SSBLOG SECTION

Copyright ©2000, Hitachi, Ltd.

Contents

19.1 Introduction SSBLOG01-10
19.2 Classification of Internal SSB SSBLOG02-10
19.3 Common information description SSBLOG03-10
19.4 Host SSB information and internal SSB format-depended information description SSBLOG04-10
19.4.1 24-byte type SSB SSBLOG04-10
19.4.2 32-byte type SSB SSBLOG04-40
19.4.3 SCSI host report format SSB SSBLOG04-60
19.5 Format-dependent information description SSBLOG05-10
- Byte27 = 0X (X≠ 8/A:System/program Check) SSBLOG05-20
- Byte27 = 08 (Reset Notification) SSBLOG05-50
- Byte27 = 0A (Bus out parity check/Overrun on LCP interface (Byte3A:b4 = 1)) SSBLOG05-70
- Byte27 = 10 (Intervention required) SSBLOG05-80
- Byte27 = 1X (Drive report error) SSBLOG05-100
- Byte27 = 3F (Reset Allegiance) SSBLOG05-120
- Byte27 = 4X (Data check) SSBLOG05-140
- Byte27 = 6X (Statistics) SSBLOG05-170
- Byte27 = 74 (FPC report error) SSBLOG05-180
- Byte27 = 79 (SCSI bus parity error) SSBLOG05-200
- Byte27 = 81 & Byte34:b4-7 = 0 (Shared Memory Failure) SSBLOG05-220
- Byte27 = 81 & Byte34:b4-7 = 3 (CHK3 Reset) SSBLOG05-410
- Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 01 (LCP Failure:CHK-2/ADP I/F Error) SSBLOG05-430
- Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 02 (LCP Failure:Link Recieve Error) SSBLOG05-450
- Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 0C (LCP Failure:Long Write Data) SSBLOG05-470
- Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 0E (LCP Failure:Timeout) SSBLOG05-490
- Byte27 = 88 & Byte34:b4-7 = A & Byte28≠ 01/02/0C/0E (LCP Failure:Others) SSBLOG05-510
- Byte27 = 88 & Byte34:b4-7 = B & Byte28 = 01 (MCP Failure:CHK2/ADP I/F ERR/BO P-ERR) SSBLOG05-530
- Byte27 = 88 & Byte34:b4-7 = B & Byte28 = 0E (MCP Failure:Timeout) SSBLOG05-560
- Byte27 = 88 & Byte34:b4-7 = B & Byte28 = 80 (MCP Failure:Burst Failed) SSBLOG05-590
- Byte27 = 89 (CHA CHK2) SSBLOG05-620
- Byte27 = 8A (FCA CHK2) SSBLOG05-870
- Byte27 = 8B (DRR CHK2) SSBLOG05-1250
- Byte27 = 8C (SVP Failure) SSBLOG05-1500
- Byte27 = 8D (Power Failure) SSBLOG05-1590
- Byte27 = 8E & Byte34 = X0 & Byte28 = 0X/10-13/15-17/2X/30-33/35-36/FE (CHK1A/WCHK1) SSBLOG05-1630
- Byte27 = 8E & Byte34 = X0 & Byte28 = 14/34 (CHK1A/WCHK1) SSBLOG05-2080
- Byte27 = 8E & Byte34 = X0 & Byte28 = 44 (CHA CHK1B) SSBLOG05-2150
- Byte27 = 8E & Byte34 = X0 & Byte28 = 42-43/52 (CHA CHK1B) SSBLOG05-2210
- Byte27 = 8E & Byte34 = X0 & Byte28 = 48-49/58-5B/FF (CHK1B) SSBLOG05-2290
- Byte27 = 8E & Byte34 = X0 & Byte28 = 4A (CHA CHK1B) SSBLOG05-2410
- Byte27 = 8E & Byte34 = X0 & Byte28 = 60-63/70/73 (DKA CHK1B) SSBLOG05-2470
- Byte27 = 8E & Byte34 = X0 & Byte28 = 68-69/79/7B (DKA CHK1B) SSBLOG05-2600
- Byte27 = 8E & Byte34 = X0 & Byte28 = 6A (DKA CHK1B) SSBLOG05-2710
- Byte27 = 8E & Byte34 = X0 & Byte28 = 64-65/74/75 (DKA CHK1B) SSBLOG05-2770
- Byte27 = 8E & Byte34 = X0 & Byte28 = F0 (Microprogram detected WCHK1) SSBLOG05-2860
- Byte27 = 8E & Byte34 = X0 & Byte28 = F1 (Microprogram CHK1A) SSBLOG05-2960
- Byte27 = 8E & Byte34:bit4-7 = 1 (Selective Reset) SSBLOG05-2980
- Byte27 = 8E & Byte34:bit4-7 = 3 (Wait SENSE Timeout) SSBLOG05-3010
- Byte27 = 8E & Byte34:bit4-7 = 5 (CHK1B Reset) SSBLOG05-3030
- Byte27 = 8E & Byte34:bit4-7 = 6 (DKC Internal Reset) SSBLOG05-3050
- Byte27 = 8E & Byte34:bit4-7 = 7 (LCP Internal Reset) SSBLOG05-3070
- Byte27 = 8E & Byte34:bit4-7 = 8 (Force Reset) SSBLOG05-3090
- Byte27 = 8E & Byte34:bit4-7 = 9 (Logical Inconsistency Reset) SSBLOG05-3110
- Byte27 = 8F (Logical Inconsistency) SSBLOG05-3130
- Byte27 = 9F (Trace data/Log data) SSBLOG05-3150

Copyright ©2000, Hitachi, Ltd.

- Byte27 = EC (Environment Monitor Detected DKC Failure) SSBLOG05-3170
- Byte27 = EE (Environment Monitor Detected DKU Failure) SSBLOG05-3200
- Byte27 = F0 (Opearation terminated) SSBLOG05-3230
- Byte27 = F1 (Micro-program Detected Cacher Failure) SSBLOG05-3250
- Byte27 = F2 (CACHE CHK2) SSBLOG05-3270
- Byte27 = F6 (CFW Access not Authorized) SSBLOG05-3470
- Byte27 = FA (NVS Terminated) SSBLOG05-3490
- Byte27 = FB (HRC/HODM Pair suspend) SSBLOG05-3510
- Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error/Warning) SSBLOG05-3530
- Byte0F:Bit1 = 1 & Byte36-37 = 08C1 (Machine Condition Exception) SSBLOG05-3950
- Byte0F:Bit1 = 1 & Byte36-37 = 0212 (Command Sequence Exception:Incomplete Domain) SSBLOG05-3970
- Byte0F:Bit1 = 1 & Byte36-37 = 4XXX (Data exception) SSBLOG05-3990
- Byte36 = 6F (Subsystem Information) SSBLOG05-4020
- Byte36:Bit0-3 = D & Byte27:bit0-2 = 7 (FPC Detected Failure) SSBLOG05-4030
- Byte36:Bit0-3 = D & Byte27:bit0-2 = 0 (Drive Detected Failure) SSBLOG05-4080
- Byte36:Bit0-3 = E & Byte2C:bit0-7≠ 5X/6X (Drive Detected Failure) SSBLOG05-4100
- Byte36 = E0 & Byte2C = 5X/6X & Byte20:b3 =1 (LDEV blockade/Pin VOL detected/Write inhibited) SSBLOG05-4220
- Byte36-37 = E210 & Byte2C = 5X/6X & Byte20:b1 = 1 (Intervention requested:LDEV not ready) SSBLOG05-4240
- Byte26:b4-7 = F & Byte3C = F1 (DKC SIM) SSBLOG05-4260
- Byte26:b4-7 = F & Byte3C = F2 (CACHE SIM) SSBLOG05-4290
- Byte26:b4-7 = F & Byte3C = FE (Device SIM) SSBLOG05-4320
- Byte26:b4-7 = F & Byte3C = FF (Media SIM) SSBLOG05-4340
- SIM Reference Codes Detected by the Processor SSBLOG05-4360
- SIM Reference Codes Detected by the SVP SSBLOG05-4580

Copyright ©2000, Hitachi, Ltd.

1 Introduction

The internal SSB (SSB Log) information is presented as either 24-byte compatibi-lity SSB format or ECKD 32-byte SSB format. The 24-byte SSB is used for DKC and the 32-byte SSB is used for DKU.

The internal SSB is devided the following sections:

- Internal SSB common information
  This information is used for SSB management, and same for all formats.

- External SSB information presented to host.
  This is 32 bytes sense information presented to host as SSB.

- Format-dependent information
  This is auxiliary information for error analysis.

See Fig.1-1 and Fig.1-2.

Note : The byte offset in SSB logs is described by hexadecimal number.
This section is correspondind to SSB log on SVP.
If you want to know about SSB which was reported to host, you should see SSB section.

Copyright ©2000, Hitachi, Ltd.

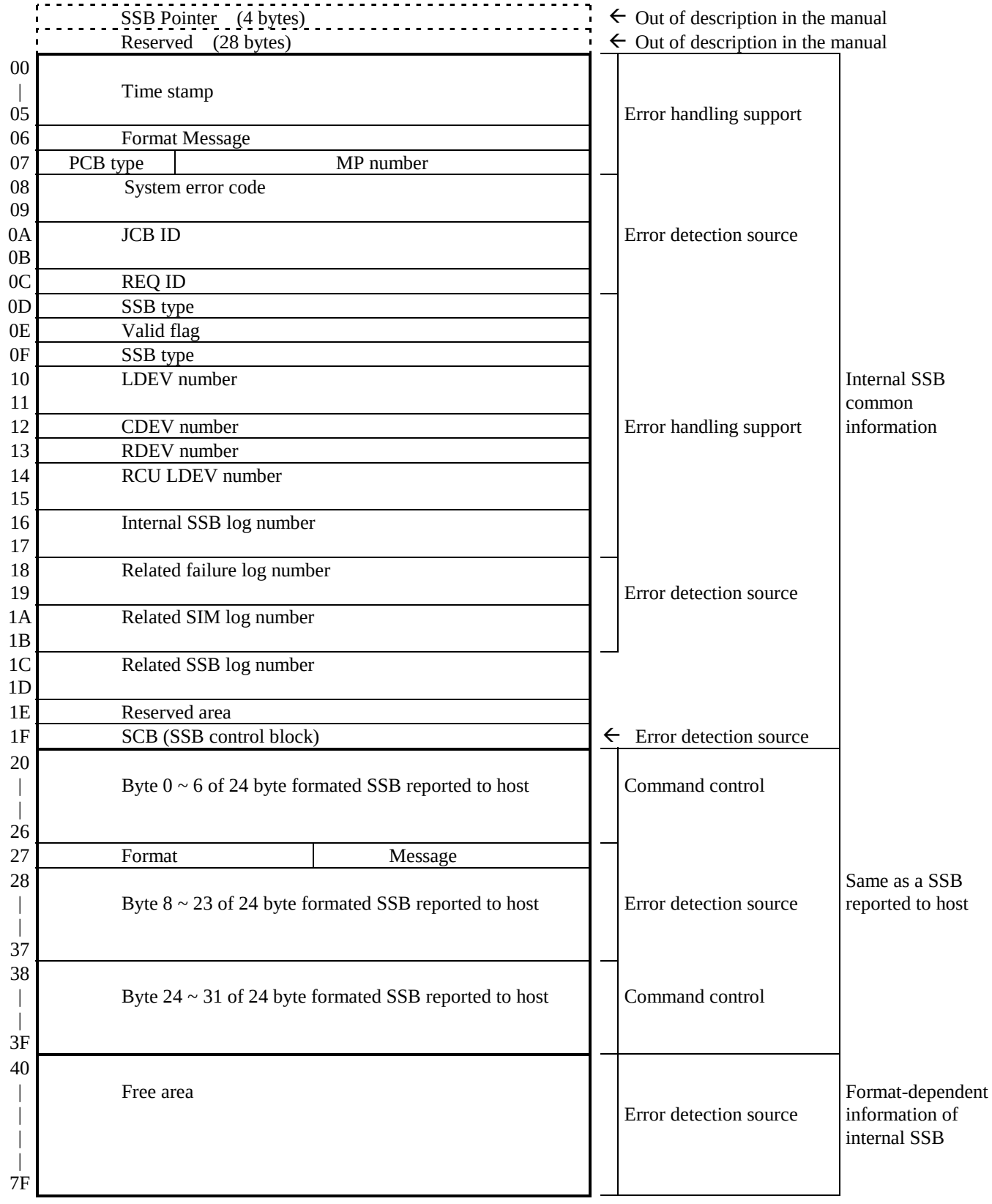


Fig.1-1 Outline of 24-byte Format Internal SSB

Copyright ©2000, Hitachi, Ltd.

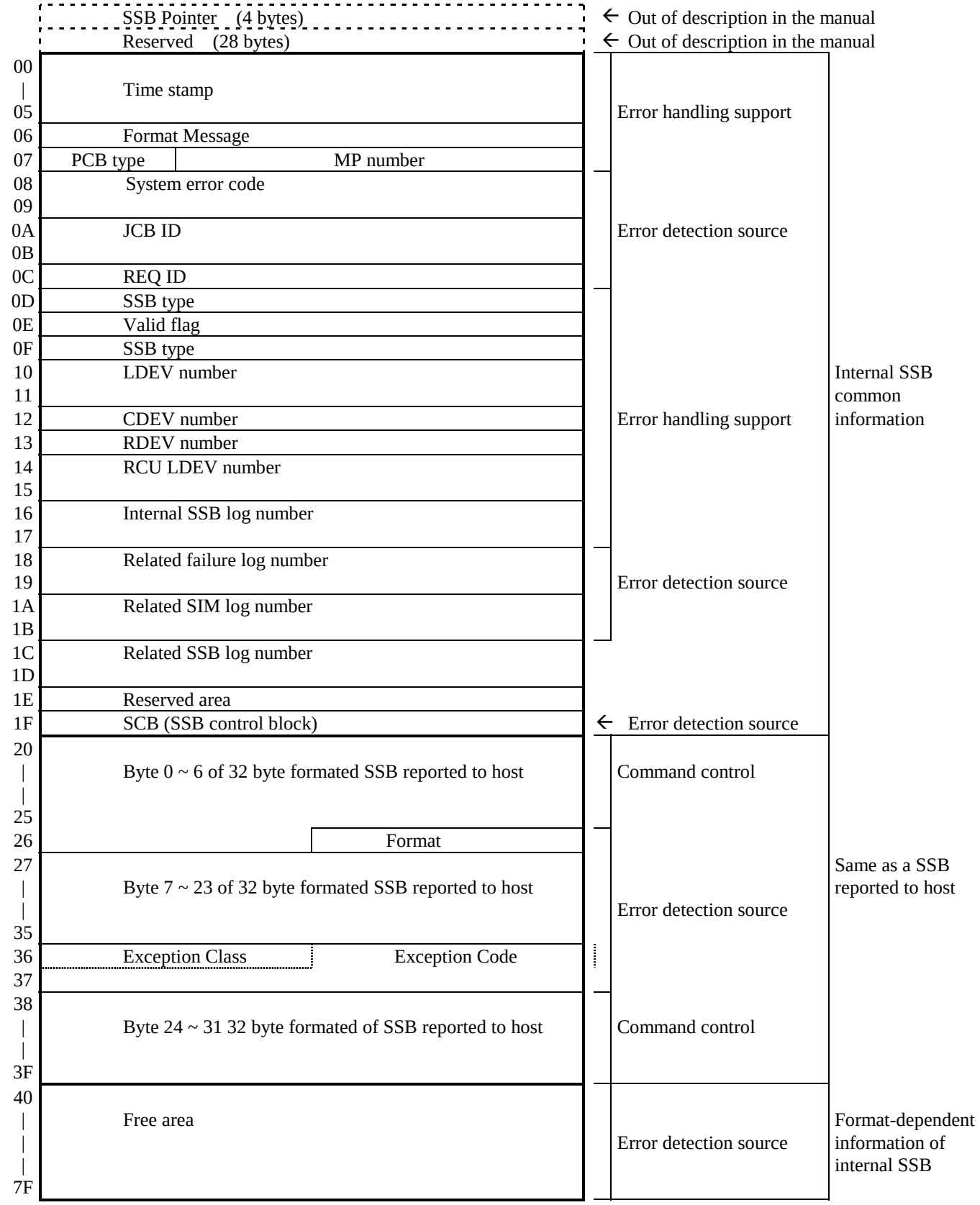


Fig.1-2 Outline of 32-byte Format Internal SSB

Copyright ©2000, Hitachi, Ltd.

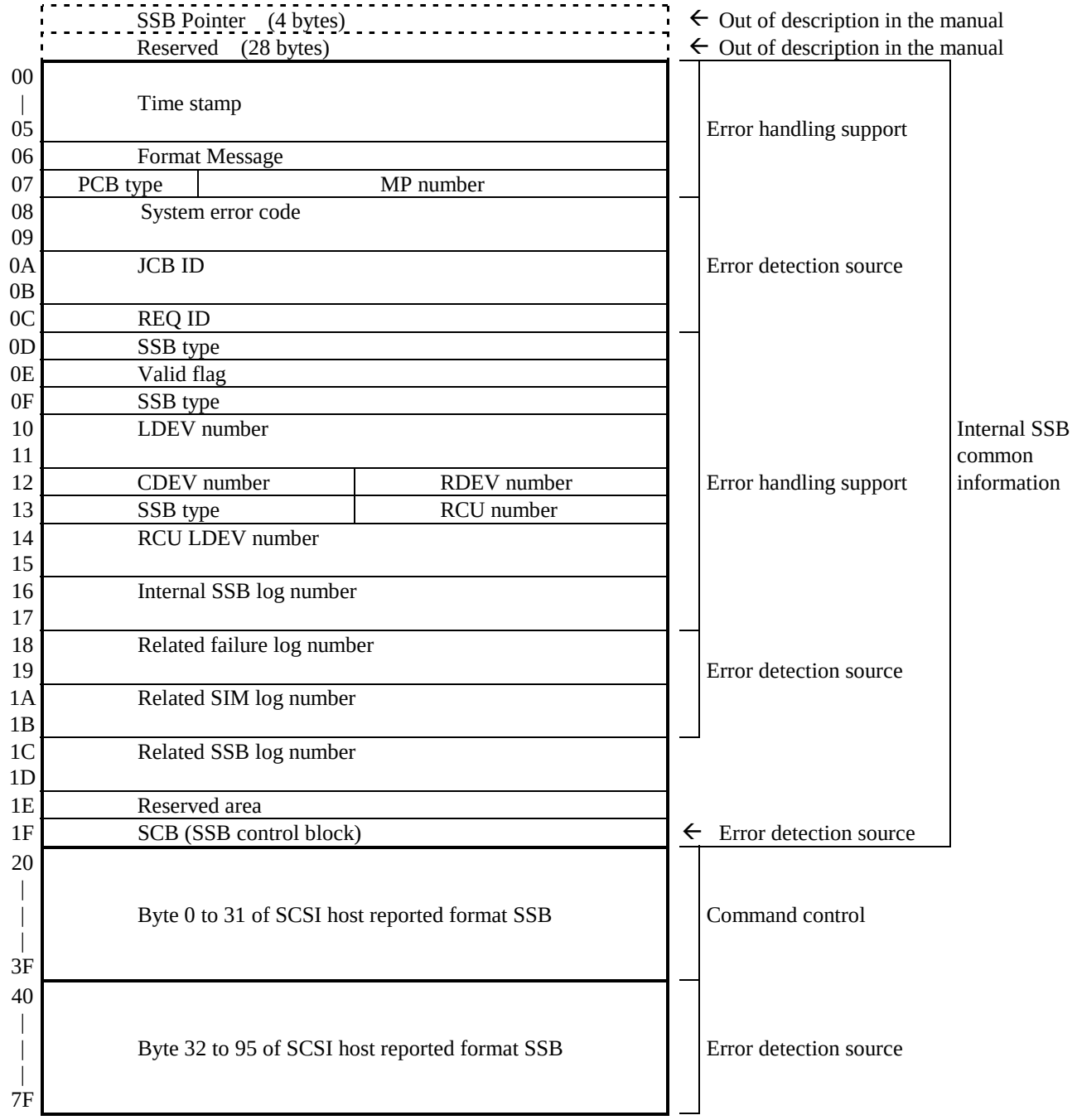
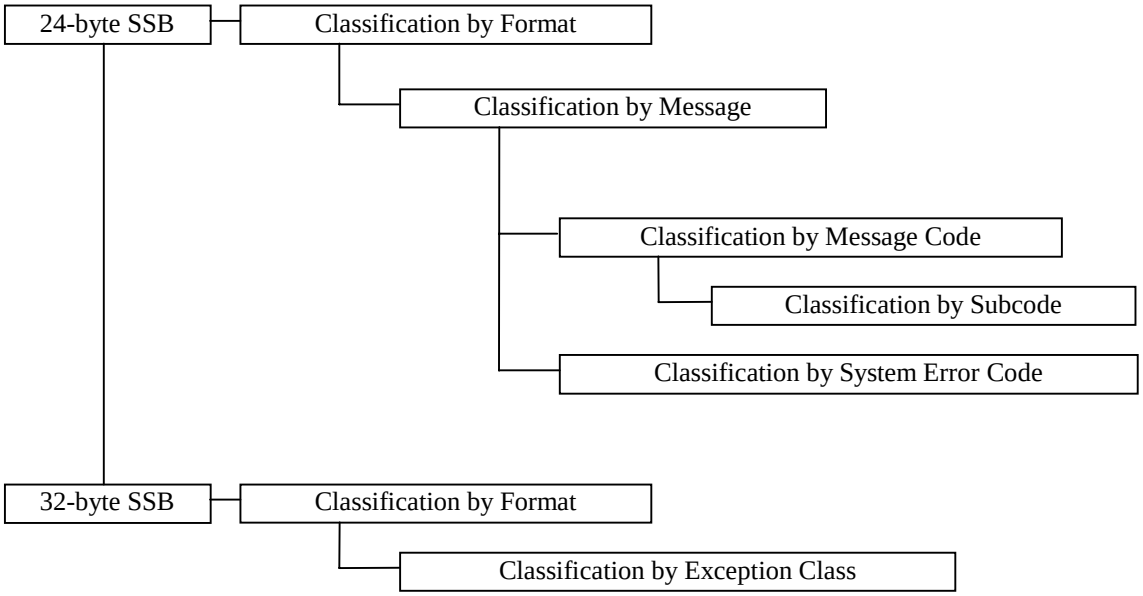


Fig.1-3 Overview of SCSI Host Report Format Internal SSB

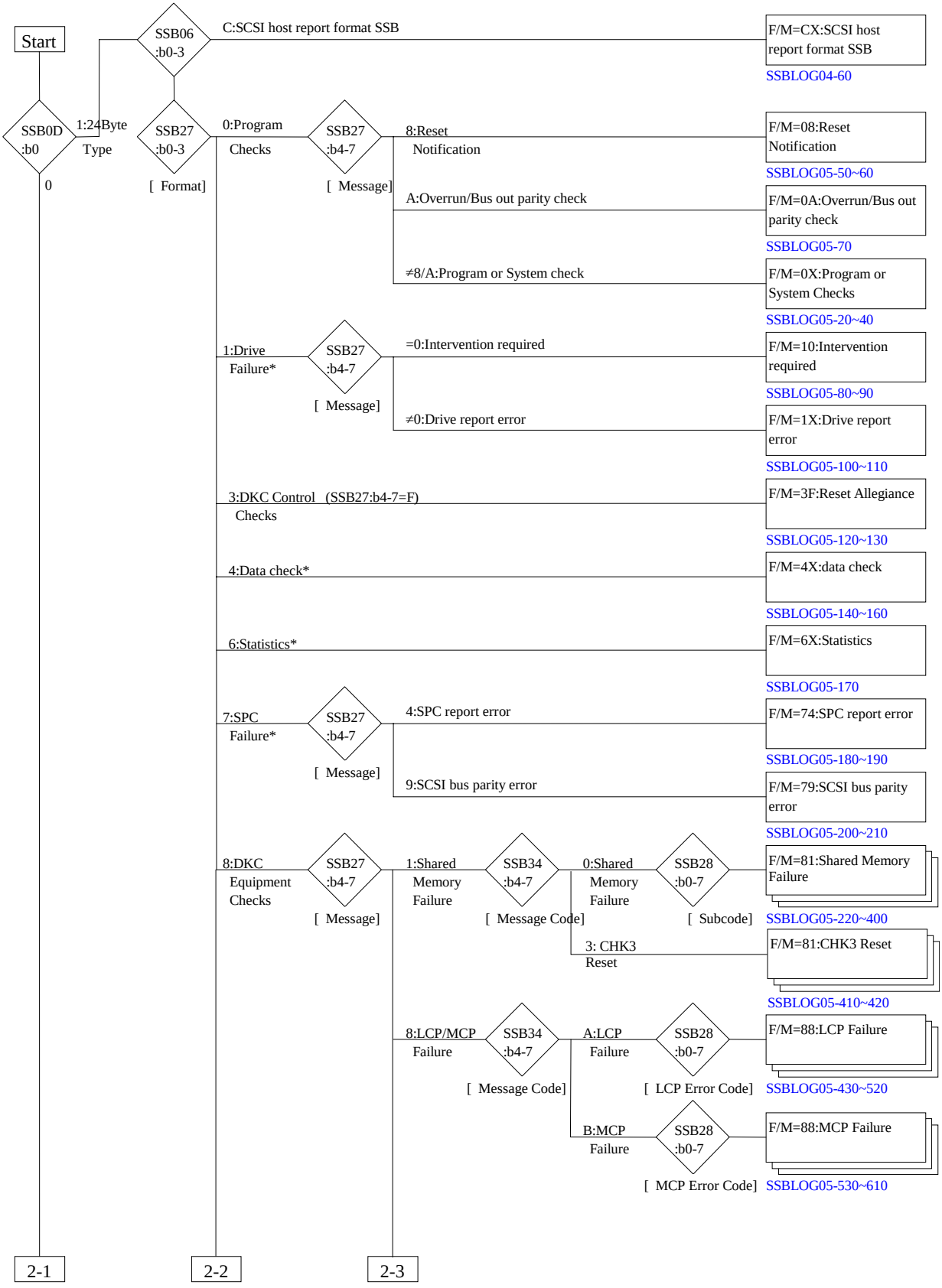
Copyright ©2000, Hitachi, Ltd.

2 Classification of Internal SSB

The internal SSB is classfied as the following figure, and Fig.2-1 for detail.



Copyright ©2000, Hitachi, Ltd.



* : For DKU86I (IBM 3380 emulation mode) only.

Fig.2-1 Search method for SSB tables (1/5)

Copyright ©2000, Hitachi, Ltd.

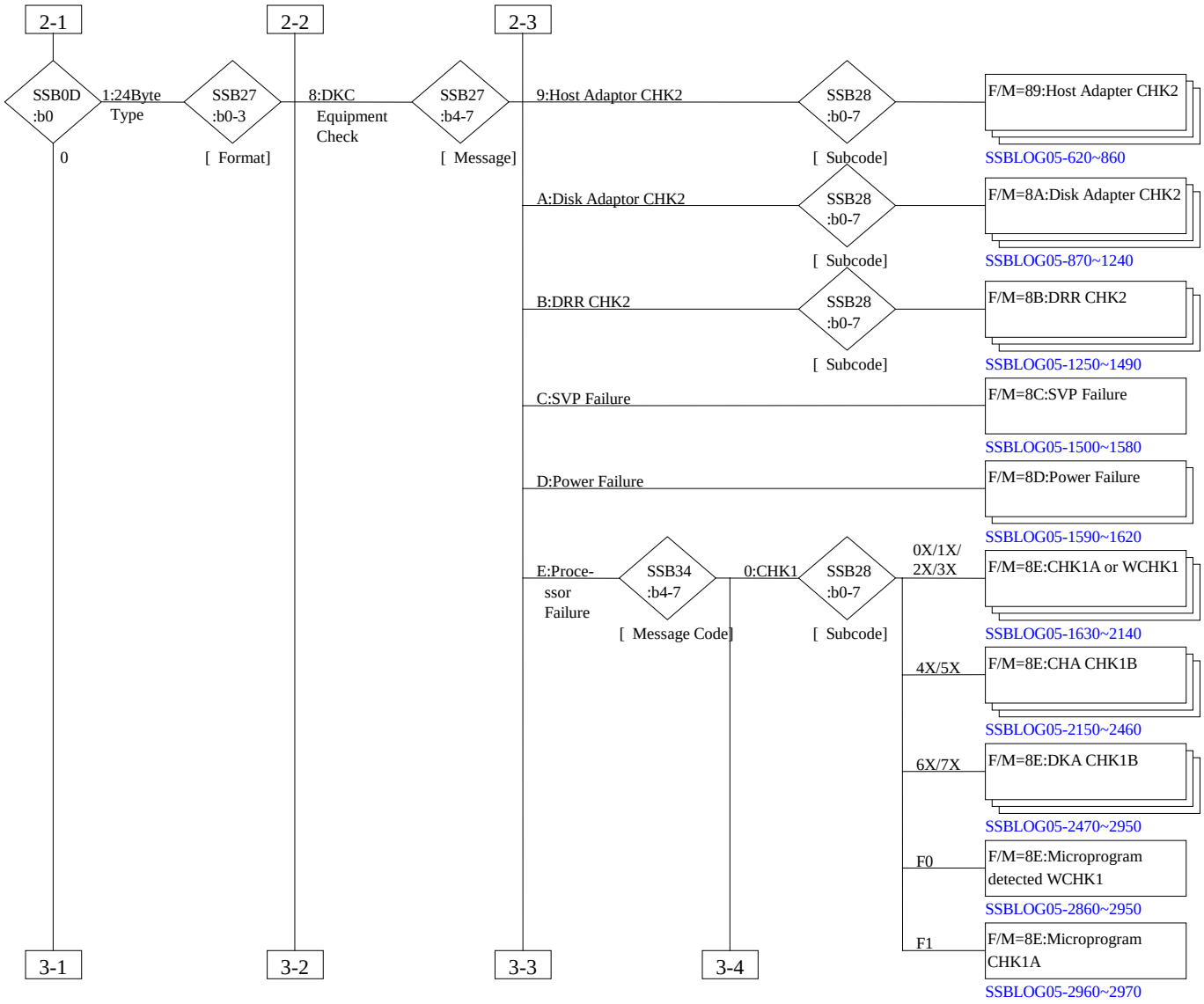


Fig.2-1 Search method for SSB tables (2/5)

Copyright ©2000, Hitachi, Ltd.

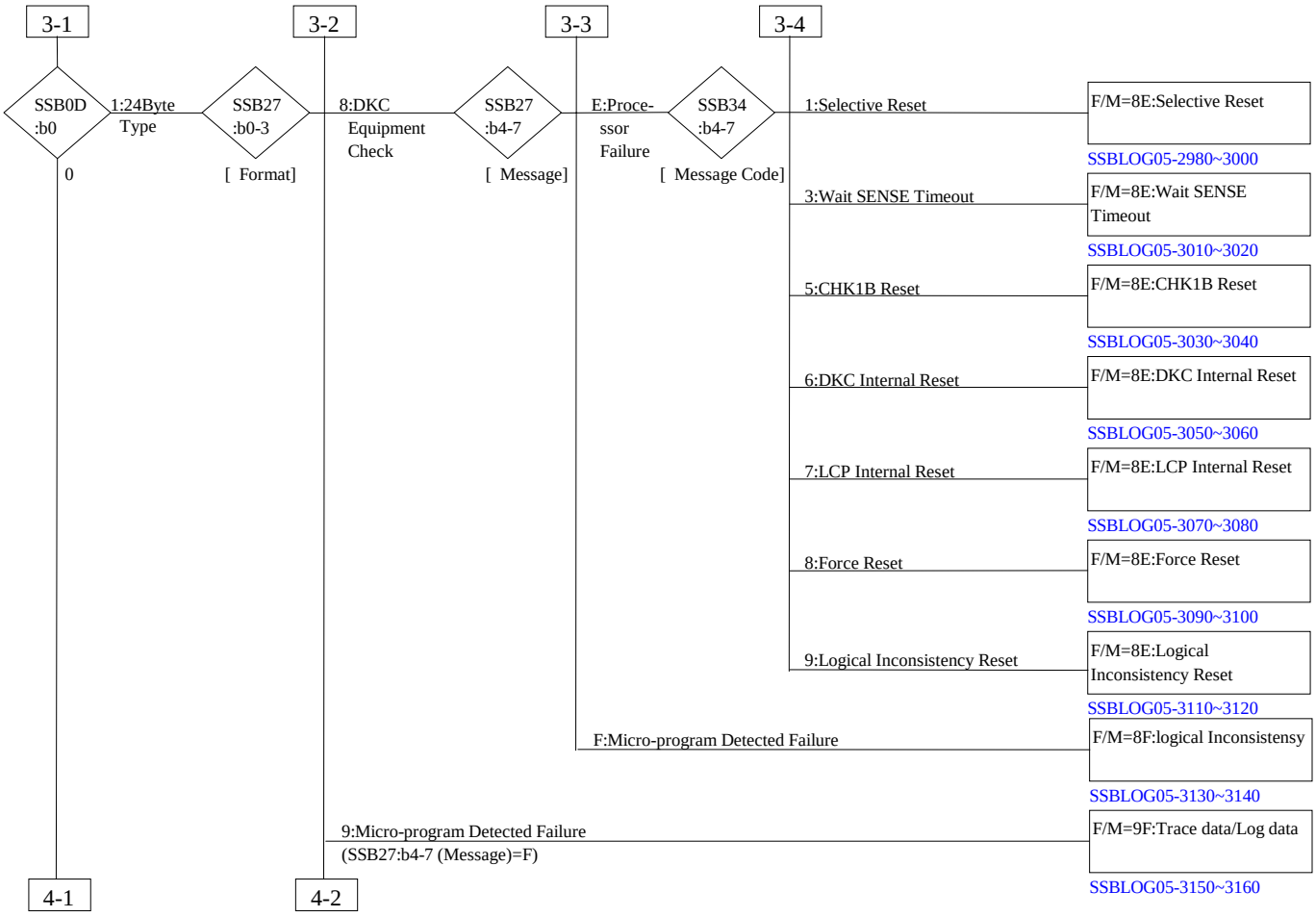


Fig.2-1 Search method for SSB tables (3/5)

Copyright ©2000, Hitachi, Ltd.

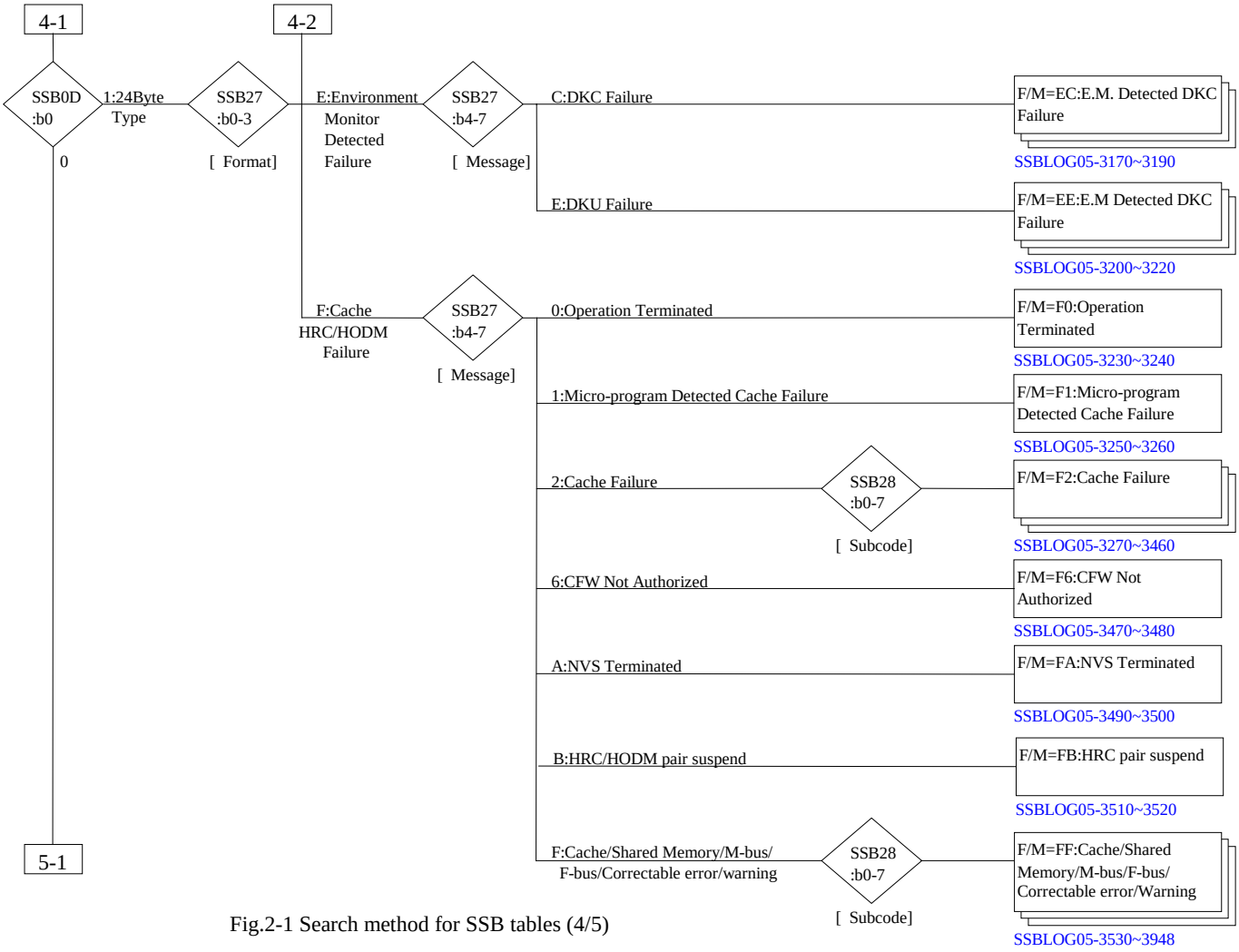


Fig.2-1 Search method for SSB tables (4/5)

Copyright ©2000, Hitachi, Ltd.

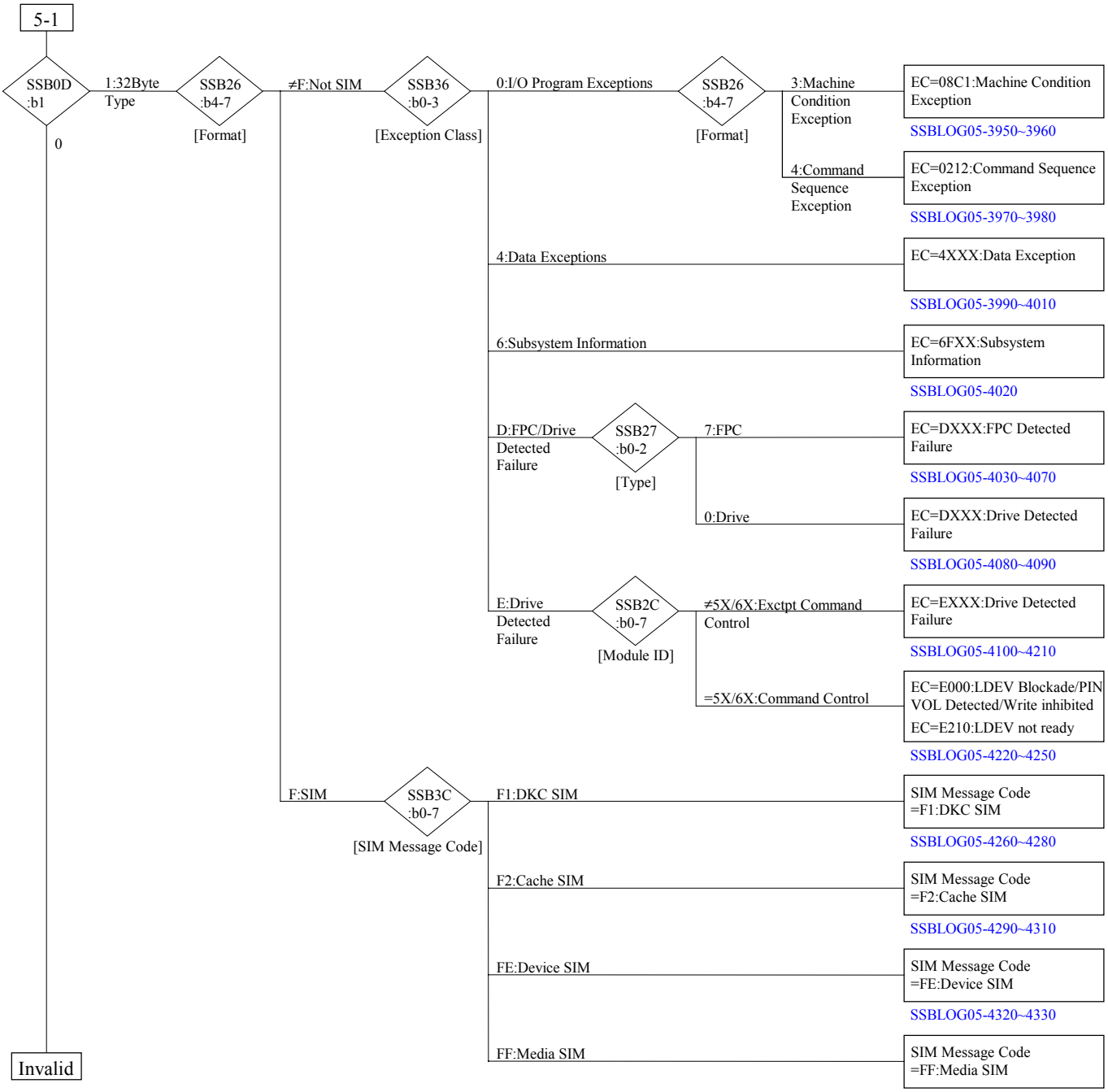


Fig.2-1 Search method for SSB tables (5/5)

Copyright ©2000,2003, Hitachi, Ltd.

3 Common information description

	0	1	2	3	4	5	6	7
00	Time Stamp							
01								
02								
03								
04								
05								
06	Format Message							
07	PCB Type		Processor ID					
08	System Error Code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host RSP	SVP RSP	Force Log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Rerserved							
1F	SCB (SSB Control Block)							
20	Host SSB Information							
⋮								
3F								
40	Internal SSB Format-Dependent Information							
⋮								
7F								

Copyright ©2000, Hitachi, Ltd.

Common Information (1/2)

Byte	Bit	Meanning	Setting	Remarks
00 - 05		Time stamp The time error occured	Error handling support	
06		Format Message	Error handling support	
07		Information of the processor detected this error	Error handling support	
	0 - 1	PCB type x'1' : CHA x'2' : DKA x'3' : CHS		
	2 - 7	Processor number (Internal ID) x'00' - x'07' : CHA0 - CHA7 x'08' - x'0F' : DKA0 - DKA7		
08 - 09		System error code	Error detection source	
	0 - 7	Module ID See " Module ID" table.		
	8 - 15	Routine ID		
0A - 0B		JCB ID	Error detection source	
0C		REQ ID	Error detection source	
0D		Valid flag	Error handling support	
	0	24Byte type flag 0:Invalid 1:24Byte type SSB		
	1	32Byte type flag 0:Invalid 1:32Byte type SSB		
	2	Flag for SCSI host processor detected the error 0:SSB detected by CHA and DKA 1:SSB detected by CHS		
	3	Remote copy flag 0:Invalid 1:Remote copy valid		
	4	Separately stored log flag 0:General log 1:Separately stored log		
	5	Host report flag 0:Pending 1:Reported		
	6	SVP report flag 0:Pending 1:Reported		
	7	Forcible log flag 0:Normal 1:Forcibly ejected log		

Copyright ©2000, Hitachi, Ltd.

Common Information (2/2)

Byte	Bit	Meanning		
0E		Valid flag	Error handling support	
	0	LDEV number valid or invalid 0:Invalid 1:Valid		
	1	PDEV number valid or invalid 0:Invalid 1:Valid		
	2	SSB number valid or invalid 0:Invalid 1:Valid		
	3	Related failure log number valid or invalid 0:Invalid 1:Valid		
	4	Related SIM log number valid or invalid 0:Invalid 1:Valid		
	5	Related SSB log number valid or invalid 0:Invalid 1:Valid		
	6 - 7	Reserved		
0F		Valid flag	Error handling support	
	0	SIM reception flag 0:First log / Log after the host reported 1:Log after SIM was received		
	1 - 7	Reserved		
10 - 11		LDEV number	Error handling support	
12		PDEV number	Error handling support	
	0 - 3	CDEV number		
	4 - 7	RDEV number		
13		HRC information	Error handling support	
	0	Reserved		
	1	RCU SIM flag 0:Invalid 1:RCU SIM valid		
	2 - 3	Reserved		
	4 - 7	RCU number		
14 - 15		RCU LDEV number		
16 - 17		Internal SSB log number		
18 - 19		Related Failure log number		
1A - 1B		Related SIM log number		
1C - 1D		Related SSB log number		
1E		Reserved area		
1F		SSB control block Use when assemble BASIC SSB of Host SSB. See " SSB Key Code" table.		

Copyright ©2000, Hitachi, Ltd.

Module ID (1/3)

Module ID	Module Name		Remarks
00	Initializer		
01	Power Off Process		
02	CUDG		
10	Job Management		
11	Synchronous Management		
12	Processor Communication		
13	Cache Control		
14	Resource Management		
15	Configuration Control		
16	Reset		
17	SVP Management		
18	Configuration Control(RAID)		
19	Configuration Control(Drive Recovery)		
30	Standard Function		
31	SVP Function		
32	Error Procedure Aid		
34	Error Procedure Aid		
35	Error Procedure Aid		
40	CHA Kernel	CHA Monitor	
41		CHA Initiator	
42		CHA Terminator	
43		CHA Common Function	
50	Command Control	Command Chain Initiate(Command Main)	
51		Command Chain Terminate(Command Main)	
52		Command Execution Status Analyze	
53		Command Execution Channel Interface Control	
54		Channel Server Common Process 1	
55		Channel Server Common Process 2	
56		Channel Server Common Process 3	
57		Channel Server Common Process 4	
58		Channel Server Transfer Process 1	
59		Channel Server Transfer Process 2	
5A		Read/Write Common Process	
5B		Substem Command Common Process	
5C		Channel Server Nonsynchronous Control 1	
5D		Channel Server Nonsynchronous Control 2	
5E		Channel Server Command Queuing Control	
5F		Channel Server Job FRR	
60		Read Command Process 1	
61		Read Command Process 2	
62		Read Command Process 3	
63		Read Command Process 4	
64		Read Command Process 5	
65		Read Command Process 6	
66		Write Command Process 1	
67		Write Command Process 2	
68		Write Command Process 3	
69		Write Command Process 4	
6A		Write Command Process 5	
6B		Write Command Process 6	
6D		Control Command Process 1	
6E		Control Command Process 2	
6F		Search Command Process	

Copyright ©2000, Hitachi, Ltd.

Module ID (2/3)

Module ID	Module Name		Remarks
70	Command Control	Path Control Command Process	
71		Sense & Miscellaneous Command Process	
72		Diagnostic Command Process	
73		Subsystem Command Process 1	
74		Subsystem Command Process 2	
75		Subsystem Command Process 3	
78		Channel Interface Link Level Frame Control	
79		Channel Interface Device Level Frame Control	
7A		Channel Interface Control Common	
7B		LDEV Format	
7C		Concurrent Copy Process	
7D		Concurrent Copy Process	
7E		Concurrent Copy Process	
7F		Channel Server WDCP/DUMP(M specified)	
80	DKA Kernel	DKA Monitor	
81		DKA Initiator	
82		DKA Terminator	
90	Staging Destaging	Staging	
91		LDEV Destaging	
92		PDEV Destaging	
93	Drive Recovery		
94	Offline Monitor		
95	Physical Device Maintenance		
98	RAID Synchrinous Type		
99	RAID LDEV Destaging		
9A	RAID PDEV Destaging		
9B	RAID Drive Recovery		
9C	RAID external provided		
9D	RAID 0 Destaging		
9E	RAID 0 Error/Merge		
9F	RAID Slot Falure Status Operation		
A0	SCSI Control		
A1	DRR Control		
A2	SVP Command Execution Process		
A3	Test Initiator		
A4	SCSI Control		
A5	Offline Monitor		
A6	Physical Drive Maintenance		
A7	SCSI Control		
A8	DRR Control		
AE	SCSI Control		
C0	HRC/HODM CHL/SVP I/F		
C1	HRC/HODM Remote copy monitor		
C2	HRC/HODM Configuration control		
C3	HRC/HODM Common copy procedure		
C4	HRC Remote copy procedure		
C5	HODM Migration copy procedure		
C6	HRC/HODM channel server procedure		
C7	HRC/HODM Remote I/O manager		
C8	HRC/HODM Remote I/O 1		
C9	HRC/HODM Remote I/O 2		
CA	HRC/HODM path control		
CF	HRC/HODM Service SIM log		

Copyright ©2000, Hitachi, Ltd.

Module ID (3/3)

Module ID	Module Name		Remarks
D0	Multiplatform Comand Control	Command Main	
D1		Transfer Process/SSB Function	
D2		Read/Write Command	
D3		Read/Write Common Process	
D4		Control/Diagnostic Command	
D8	Multiplatform SCP Control	SCP Control 1	
D9		SCP Control 2	
DA		SCP Control 3	
DC	Multiplatform Kernel	Command Queuing Procedure	
DD		CHS Scan	
DE		CHS Initiator	
DF		CHS Terminator	
E0	RCP initialize / Reset / Sequence control		
E1	RCP idle scan / Starting process		
E2	RCP link level process		
E3	RCP device level process		
E4	RCP error process / Received frame check / physical service		
E5	Communication between RCP and CHP / Path control / Clock timer control / Frame transmission and reception		
E6	RCP sequence process / Device level process		

Copyright ©2000, Hitachi, Ltd.

SSB Key Code (1/2)

Code	Basic SSB	Meanning	Remarks
00	000000	Dummy SSB	
01	800000	Command reject (A program error or invalid link between BAD and ALT)	
02	400000	Intervention required (An addressed device is offline or not connect)	
03	200000	Bus out check (Channel bus out parity error)	
04	100000	Equipment check (Equipment check in subsystem)	
05	080000	Data check (Uncorrectable:retry failed or retry inhibited)	
06	040000	Overrun (command retry failed when service overrun occured)	
07	004000	Invalid track format (Track capacity over or track format error)	
08	002000	End of cylinder (A multi track operation outside LOCATE domain)	
09	000800	No record found	
0A	000400	File protected (A seek or multi track operation violates the file mask or extent)	
0B	100200	Equipment check and write inhibited (A write command on the write inhibited path by a DIAG CTL command)	
0C	080040	Data check and correctable (The retry succeeded for data check in PCI fetch mode)	
0D	000020	First log mode error	Not used
0E	800400	Command rejected and file protected (A multi track operation outside primary track)	
0F	800200	Command reject and write inhibited	Not used
10	108000	Equipment check and permanent error) (A retry failed for the equipment check)	
11	088000	Data check and permanent error) (A retry failed for the data check)	
12	009010	SIM (DKC SIM or Cache SIM)	
13	000000	Reserved	
14	000104	Imprecise ending (This error is for a previousry completed CCW)	
15	800104	Command reject and imprecise ending	
16	400104	Intervention required and imprecise ending	
17	200104	Bus out check and imprecise ending	
18	100104	Equipment check and imprecise ending	
19	080104	Data check and imprecise ending	
1A	040104	Overrun and imprecise ending	
1B	004104	Invalid track format and imprecise ending	
1C	002104	End of cylinder and imprecise ending	
1D	000904	No record found and imprecise ending	
1E	000504	File protected and imprecise ending	
1F	100304	Equipment check and write inhibited and imprecise ending	

Copyright ©2000, Hitachi, Ltd.

SSB Key Code (2/2)

Code	Basic SSB	Meanning	Remarks
20	080144	Equipment check and correctable and imprecise ending	
21	000124	First log mode error and imprecise ending	Not used
22	800504	Command reject and file protected and imprecise ending	
23	800304	Command reject and write inhibited and imprecise ending	
24	108104	Equipment check and permanent error and imprecise ending	
25	088104	Data check and permanent error and imprecise ending	
26	009114	SIM and imprecise ending	Not used
27	000000	Reserved	
28	808000	Command reject and permanent error	
29	00C000	Permanent error and invalid track format	
2A	008800	Permanent error and request inhibit write	
2B	088200	Data check and permanent error and write protected	
2C	000000	Reserved	
2D	000000	Reserved	
2E	000000	Reserved	
2F	000000	Reserved	
30	000000	Reserved	
31	000000	Reserved	
32	010000	Incomplete domain (Received commands < LOCATE command prameter)	
33	804000	Command reject and invalid track format (A TLF unmatch in CKD conversion mode)	
34	000000	Reserved	
35	100010	Equipment check and environmental data present (Status change pending)	
36	800010	Command reject and environmental data present	
37	000000	Reserved	
38	000000	Reserved	
39	000000	Reserved	
3A	000000	Reserved	
3B	000000	Reserved	
3C	000000	Reserved	
3D	000000	Reserved	
3E	000000	Reserved	
3F	000000	Reserved	

Copyright ©2000, Hitachi, Ltd.

4 Host SSB information and internal SSB format-depended information description

4.1 24-byte type SSB

	0	1	2	3	4	5	6	7	
00	Internal SSB common Information								
1F									
20	Command reject	Intervention REQ	Bus out check	Equipment check	Data check	Overrun	Unused	Incomplete domain	Basic SSB
21	Permanent error	Invalid track FMT	End of cylinder	Operator message	No Record found	File protect	Write inhibit	Imprecise ending	
22	Write INH reques	Correctable	1st log mode ERR	Environmen-tal DAT	Unused	Imprecise ending	Not used	Not used	
23	Count								
24	Device address								
25	Cylinder address(low)								
26	Cylinder address(high)				Head address				
27	Format (See next page)				Message (See next page)				
28	Host SSB Format-depended Information								
37									
38	Log and message control								
39	Program action code								
3A	Dual frame	EDCC mode (1)	Duplex pair (0)	S-volume ERR (0)	Nonsync operation	Serial channel	Report output	Permanent path ERR	*
3B	24Byte SSB (1)	DEV ADR valid	TRK ADR valid	Not used	3380 TRK COMPT(0)	Not used	Storage path number		
3C	Not used								
3D	Cylinder address								
3E									
3F	Head address								
40	Internal SSB Format-depended Information								
7F									

*:Configuration information

**:Byte 20-27 and byte 38-3F are not certain until DKC reports SSB to Host. So if you want to know the detail, please refer to SSB section.

Copyright ©2000, Hitachi, Ltd.

Format and Message

(1/2)

Format	Message	Meanning	
0	0	No message	
	1	Invalid command	
	2	Invalid sequence	
	3	Data short	
	4	Invalid data	
	5	Violate file mask	
	6	Channel disconnect retry.	
	7	Invalid retry command	
	8	System reset	
	9	Not used	
	A	Bus of parity check/Overrun	
	B	Invalid link between bad track and alternate track.	
	C	Not used	
	D	Not used	
	E	Invalid command to secondary volume	
	F	Invalid status	
1	0	Intervention required	For DKU86I (IBM 3380 emulation mode) only
	1	Not used	
	2	Drive not ready	
	3	Not used	
	4	Drive report error	
	5~F	Not used	
3	0~E	Not used	
	F	Reset allegiance	
4	0	Data check in HA field	For DKU86I (IBM 3380 emulation mode) only
	1	Data check in C field	
	2	Data check in K field	
	3	Data check in D field	
	4	Not used	
	5	PA error	
	6~F	Not used	
6	0~7	Statistics	
	8~F	Not used	
7	0~3	Not used	
	4	SPC report error	
	5~8	Not used	
	9	SCSI bus parity error	
	A~F	Not used	
8	0	Not used	
	1	Shared memory failure	
	2~7	Not used	
	8	LCP failure or MCP failure	
	9	Host adaptor CHK2	
	A	Disk adaptor CHK2	
	B	DRR failure	
	C	SVP failure	
	D	Power failure	
	E	Processor failure	
	F	Micro-program detected error (Logical Inconsistency)	
9	0~E	Not used	
	F	Micro-program detected error (Trace data/Log data)	
E	0~B	Not used	
	C	Environmental monitor detected DKC failure	
	D	Not used	
	E	Environmental monitor detected DKU failure	
	F	Not used	

Copyright ©2000, Hitachi, Ltd.

Format and Message

(2/2)

Format	Message	Meanning
F	0	Operation Terminated
	1	Microprogram detected cache failure
	2	Cache failure
	3	Not used
	4	Not used
	5	Not used
	6	CFW not authorized
	7~9	Not used
	A	NVS terminated
	B	HRC/HODM Pair suspend
	C~E	Not used
	F	Cache/Shared memory/M-bus/F-bus/J-bus warning

Copyright ©2000, Hitachi, Ltd.

4.2 32-byte type SSB

	0	1	2	3	4	5	6	7	
00	Internal SSB common Information								
1F									
20	Command reject	Intervention REQ	Not used	Equipment check	Data check	Not used	Not used	Incomplete domain	Basic SSB
21	Permanent error	Invalid TRK FMT	End of cylinder	Operator message	Not used	File protect	Write inhibit	Imprecice ending	
22	EC=0/1/2/3/F:Environmental data present								
	EC=4/6/D/E :Strage control type (x' 06' :Cache DKC)								
23	Count / Command overrun threshold is exceede.								
24	Device address								
25	Device type (x' 24' :DKU871-3)								
26	SSB2/SSB5 valid	SSB4 valid	SSB29-31 valid	Not used	Format				
27	Host SSB Format-depended Information								
37									
38	Log and message control								
39	Program action code								
3A	Dual frame	EDCC mode (1)	Duplex pair (0)	S-Volume ERR (0)	Nonsync operation	Serial channed	Report output	Permanent path ERR	*
3B	32Byte SSB (0)	Not used	Not used	Not used	3380 TRK COMPT(0)	Not used	Storage path number		
3C	Message code								
3D	Cylinder address								
3E									
3F	Heas address								
40	Internal SSB Format-depended Information								
7F									

*:Configuration information

**:Byte 20-26 and byte 38-3F are not certain until DKC reports SSB to Host. So if you want to know the detail, please refer to SSB section.

Copyright ©2000, Hitachi, Ltd.

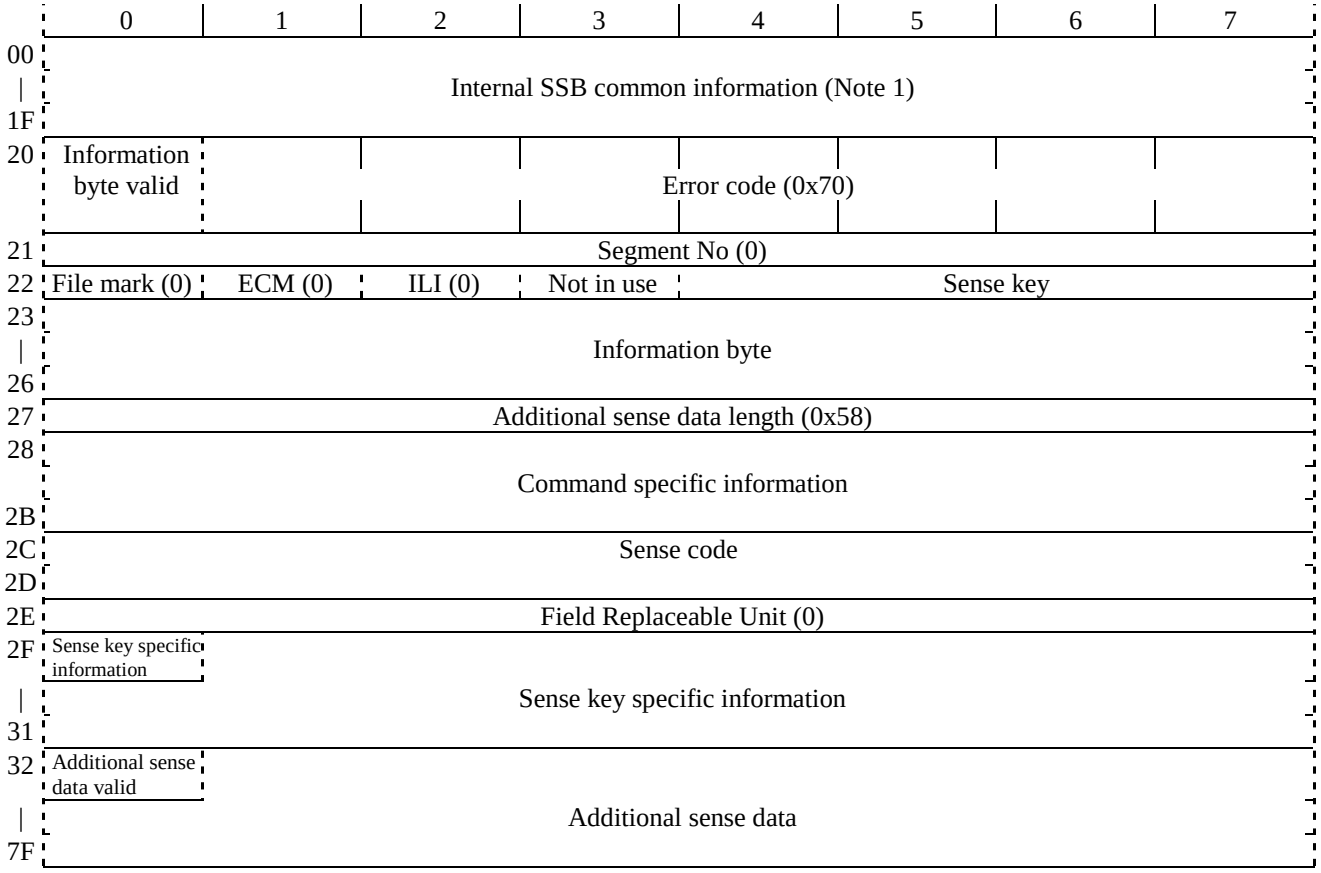
Exception Class (Byte36:bit0-3) and Format (Byte26:bit4-7)

Exception Class	Format	Meanning
0	0~2	Not used
	3	Machine condition exception
	4	I/O Program exception (incomplete Domain)
	5~F	Not used
2	0~E	Not used
	F	DKC SIM
3	0~E	Not used
	F	DKC SIM
4	0	Not used
	1	Data exception (PCI,Permanent)*
	2~E	Not used
	F	Dedia SIM
5	0~E	Not used
	F	Device SIM/Media SIM
6	0	Not used
	1	Statistics*
	2~F	Not used
C	0~E	Not used
	F	DKC SIM
D	0	Drive detected failure*
	1	SPC detected failure*
	0~E	Not used
	F	DKC SIM
E	0	Drive detected failure/LDEV blockade/PIN VOL detected/LDEV not ready/Write inhibited*
	1~E	Not used
	F	Device SIM
F	0~E	Not used
	F	DKC SIM/Cache SIM

* : For DKU87I (IBM 3390 emulation mode) only.

Copyright ©2000, Hitachi, Ltd.

4.3 SCSI host report format SSB



(Note 1) 0xCX (X=sense key) is set to byte 7 (log type low-order byte). SSB on SVP is indicated as F/M=CX.

Copyright ©2000, Hitachi, Ltd.

Details of SCSI host report format SSB information

Byte	Bit	Description	Setting	Remarks
20	0	Information byte valid/invalid 0:Invalid 1:Valid	CHS command control	
	1 ~ 7	Error code (0x7): Indicates an I/O process error.		
21		Segment No. (0)		
22	0	File mark (0)		
	1	ECM (0)		
	2	ILI (0)		
	3	Not in use		
	4 ~ 7	Sense key: For more details, see “ sense keys list”.		
23 ~ 26		Information bytes: LBA related to sense key if information byte is valid.		
27		Additional sense data length (0x58): Indicates sense data length after byte 8 or latter.		
28 ~ 2B		Command specific information		
2C ~ 2D		Sense codes: For more details, see “ sense codes list”.		
2E		Field Replaceable Unit (0)		
2F ~ 31	0	Sense key specific information valid/invalid 0:Invalid 1:Valid		
	1 ~ 17	Sense key specific information		
32 ~ 7E	0	Additional sense data valid/invalid 0:Invalid 1:Valid	Error detection source	
	1 ~ END	Additional sense data		

Copyright ©2000, Hitachi, Ltd.

Sense Keys List

Sense key	Description
0	NO SENSE
1	RECOVERED ERROR
2	NOT READY
3	MEDIUM ERROR
4	HARDWARE ERROR
5	ILLEGAL REQUEST
6	UNIT ATTENTION
7	DATA PROTECT
8	BLANK CHECK (Not in use)
9	VENDOR UNIQUE
A	COPY ABORTED
B	ABORTED COMMAND
C	EQUAL (Not in use)
D	VOLUME OVERFLOW
E	MISCOMPARE
F	(RESERVED)

Copyright ©2000,2002, Hitachi, Ltd.

Refer to SSB04-180 ~ SSB04-190 about Sense Codes.

Copyright ©2000,2003, Hitachi, Ltd.

Blank Sheet

Copyright ©2000,2003, Hitachi, Ltd.

Blank Sheet

Copyright ©2000,2003, Hitachi, Ltd.

Blank Sheet

Copyright ©2000,2003, Hitachi, Ltd.

Blank Sheet

Copyright ©2000,2003, Hitachi, Ltd.

Blank Sheet

Copyright ©2000,2003, Hitachi, Ltd.

Blank Sheet

Copyright ©2000,2003, Hitachi, Ltd.

Blank Sheet

Copyright ©2000,2003, Hitachi, Ltd.

Blank Sheet

Copyright ©2000,2003, Hitachi, Ltd.

Blank Sheet

Copyright ©2000,2003, Hitachi, Ltd.

5 Format-depended information description

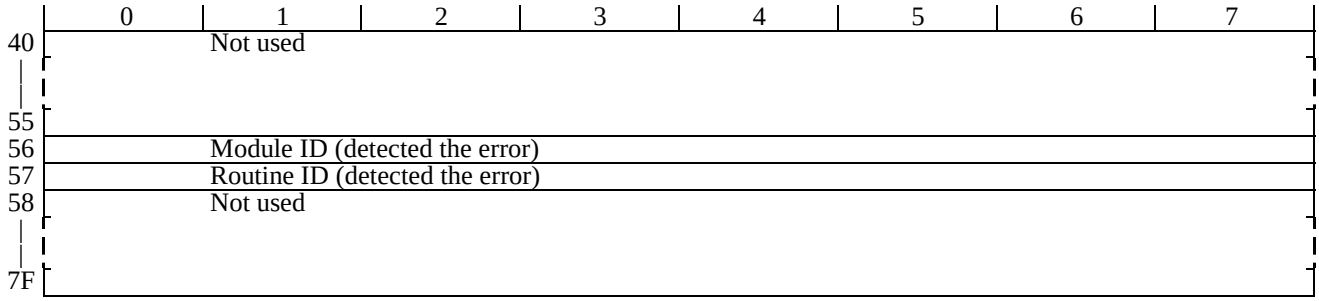
Copyright ©2000, Hitachi, Ltd.

Byte27 = 0X (X ≠ 8/A:System/Program Check) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘0’)				Message (x‘X’:X ≠ 8/A)			
28	Command code (for F/M ≠ F)/Reason code (for F/M=F) (Note 1)							
29	Detail failure information 1 (Note 2)							
2A								
2B								
2C								
2D	SSID of mate subsystem (x‘0000’ for EDCC)							
2E								
2F	Maker code & Manufacture code (x‘00’)							
30	Module ID (Note 4)							
31	Routine ID (Note 4)							
32	PCB number							
33	Detail failure information 2 (Note 3)							
34	SSID of self subsystem							
35								
36	Symptom code (x‘0F0X’)							
37	X=Message code (x‘2F00’ for dummy SENSE)							
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000,2003, Hitachi, Ltd.

Byte27 = 0X (X ≠ 8/A:System/Program Check) (2/3)



(Note 1)

F/M = 0F:Byte08 Reason code

Code	Reason
00	No message
01	Trying to make cache available and cache status is pending.
02	Not used
03	Trying to make cache force unavailable and cache status is not pending with destage complete.
04	Trying to activate CFW and CFW status is pending.
05	Trying to activate caching (device) and cache status is pending.
06	Trying to destage (track) and NVS is failed.
07	Trying to make NVS unavailable and NVS is initializing.
08	Trying to deactivete caching , DFW or DISCARD (device) , and DFW status is failed.
09	Trying to force deactivate DFW (device) and status is not as follows. • EDFW status is pending or failed. • ENVS is failed and the data exists in NVS, but not in cache.
0A	Trying to make NVS available and DFW status (device) is pending or failed.
0B	Trying to make NVS available and NVS status is pending.
0C	When NVS is failed, trying to stop caching or DFW (device) and the data exists in NVS, but not in cache.
0D	Command requires NVS and NVS is unavailable.
0E	Command requires cache and cache is unavailable.
0F	Not used
10 ~ 28	Not used
29	PFS command (Set Special Interrupt Condition) is issued on an interface on which path group is not established.
2A	Trying to make path group include parallel channel and serial channel.
2B	Message buffer is full.
2C ~ 34	Not used
35	A Set Guaranteed Path subcommand is issued on a fenced path.
36 ~ 3E	Not used
3F	A Make NVS Avail for Subsystem subcommand is issued, but NVS is disable. ('Disable NVS Capability' is set to disable in VPD.)
40	Not used
41	A normal command is issued to a device reserved by maintenance.
42 ~ 7F	Not used
80	A special command is issued on an interface that was disabled by the PFS command with Set Special Intercept Condition order.
81	An attention report on an interface that was disabled by the PFS command with Set Special Intercept Condition order.
82 ~ FF	Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 0X (X ≠ 8/A:System/Program Check) (3/3)

(Note 2) (1) Issued command information when F/M=02

B∴b	0	1	2	3	4	5	6	7
29	SCH ID	SCH KEY	Locate, LC EXT	SK, SK CYL	RD IPL	RECAL	SUSP MPR	RD C
2A	DIAG CTL	DIAG CTL (LOC DOM)	DEF EXT	SET FM	SET SUB MODE	SP C	WR CKD	WR R0
2B	SET INTF ID	DIAG CTL (PRE REM)	0	Other command	RD C chainning	All byte match	LC domain	Erase execute
2C	Pseud through	0	0	Allow WR KD	Allow WR D	Allow WR CKD	Allow WR R0	Allow WR HA

(2) Short byte flag when F/M=03
x‘0040 0000’

(3) Mask information when F/M=05

Byte 29: Mask for write control
- x‘00’: Allow all write operation except WR HA, WR R0.
- x‘40’: Inhibit all write operation.
- x‘80’: Allow update write operation.
- x‘C0’: Allow all write operation.

Byte 2A: Mask for seek control
- x‘00’: Allow all seek commands and RECAL.
- x‘08’: Allow SK CYL and SK HD only.
- x‘10’: Allow SK HD only.
- x‘18’: Inhibit all seek command and multi operation.

Byte 2B: Mask for access
- x‘00’: Allow normal access.
- x‘02’: Allow device support.
- x‘04’: Allow diagnostic access.
- x‘06’: Allow device support inhibit data check correction and retry.

Byte 2C: Not used

(4) Record address when other F/M
Byte 29 and 2A : Clinder address
Byte 2B : Head address
Byte 2C : Record number

(Note 3) Bit 4-7 of byte 32: Type of byte 33
- x‘08’: Byte 33 is cylinder address (high).
- x‘09’: Byte 33 is cylinder address (low).
- x‘0A’: Byte 33 is head address (high).
- x‘0B’: Byte 33 is head address (low).
- x‘0C’: Byte 33 is record number.

Byte 33: One byte of CCHHR.

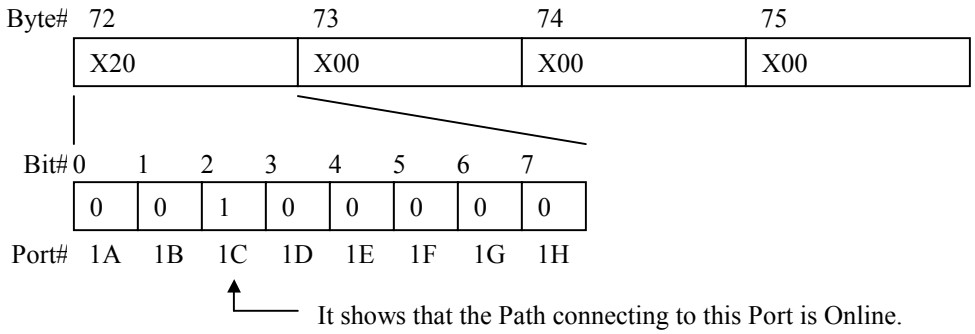
Copyright ©2000, Hitachi, Ltd.

(Note4) The details information of every Module ID & Routine ID

•Module ID & Routine ID=0xC0CA ; The Specified R-VOL of HRC is still Online from the HOST.
(Add Pair operation from the Remote Console was rejected)
Check the SSB.LOG on SVP of the specified RCU. SSB containing EC=C0CA on the specified R-VOL number should be logged.

•Module ID & Routine ID=0xC0A6 ; The M-VOL of HODM is Online from the HOST.
Check the SSB.LOG on SVP of the MCU. SSB containing EC=C0A6 on the specified M-VOL should be logged.

(1) Analyze the SSB.LOG
Both SSB are same format, from SSB byte72(0x48) though byte75(0x4B) show the Bit Map of Port indicating Online from the HOST. Each one bit corresponds to each port. It indicates the LCP Port on which the valid Path Group is established for this device.



(2) Run DSF/ANALYZE-ALLCHPID to trace the Path Group ID of the Online route.
(2.1) In case that DKC Emulation Type is 3990-6/3990-6E or 2105.
Run DSF/ANALYZE with ALLCHPID. The output shows the Path Group ID which is Online to the subsystem.

LOGICAL PATH		SYSTEM ADAPTER ID	FULL ESCON LINK ADDRESS	SP FENCE 0 1 2 3	HOST PATH GROUP ID		
NUMBER	type				CPU SERIAL#	CPU TYPE	CPU TIME STAMP
1	E	00	0101		XXXXXXX	YYYY	ZZZZZZZZ
2-32	N/E	00-01					
33	E	02	0200		XXXXXXX	YYYY	ZZZZZZZZ

"SYSTEM ADAPTER ID" corresponds to the number of the CHL adapter port.
(Ex; Port#1C is "02".)
Trace the Path Group ID indicated the SYSTEM ADAPTER ID corresponding to the value on SSB LOG of EC=C0CA or C0A6.

Note; Reference of Port ID & SAID

CL1								CL2							
CHA-1P		CHA-1Q		CHA-1R		CHA-1S		CHA-2V		CHA-2W		CHA-2X		CHA-2Y	
Port	SAID	Port	SAID	Port	SAID	Port	SAID	Port	SAID	Port	SAID	Port	SAID	Port	SAID
A	00	E	04	J	08	N	0c	A	10	E	14	J	18	N	1c
B	01	F	05	K	09	P	0d	B	11	F	15	K	19	P	1d
C	02	G	06	L	0a	Q	0e	C	12	G	16	L	1a	Q	1e
D	03	H	07	M	0b	R	0f	D	13	H	17	M	1b	R	1f

(2.2) In case that DKC Emulation Type is 3990-3 DSF/ANALYZE-ALLCHPID is not available for 3990-3. Therefore, trace the Path Online Route of the LCP.

Copyright ©2003, Hitachi, Ltd.

Byte27 = 08 (Reset Notification) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘0’)				Message (x‘8’)			
28	Not used (x‘00’)							
29	Not used (x‘00’)							
2A	Not used (x‘00’)							
2B	Hardware level (Note 1)							
2C								
2D	SSID of mate subsystem (x‘0000’ for EDCC)							
2E								
2F	Maker code & Manufacture code (x‘00’)							
30	Module ID							
31	Routine ID							
32	PCB number				Not used (x‘0’)			
33	Not used (x‘00’)							
34	SSID of self subsystem							
35								
36	Symptom code (x‘2FFF’)							
37								
38	Log & message control (x‘00’)							
39	Program action code (x‘16’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 08 (Reset Notification) (2/2)

	0	1	2	3	4	5	6	7
40		Not used						
7F								

(Note 1) Hardware Level

Bit0 : Serial Channel or Parallel Channel

Bit0=0(Parallel channel)

- Bit 1 : Not used
- Bit 2~3 : Strage Path Number
- Bit 4~5 : Channels Per Cluster
  - 00 : 4
  - 01 : 8
  - 10 : Unused
  - 11 : Unused
- Bit 6 : NVS
  - 0 : without NVS
  - 1 : with NVS
- Bit 7 : Unused
- Bit 8~10 : Cache size
  - 000 : none Cache
  - 001 : 256MB
  - 010 : 512MB
  - 011 : 768MB
  - 100 : 1024MB
  - 101 : 1280MB
  - 110 : 1536MB
  - 111 : over 1536MB
- Bit 11~13 : Cluster hardware level
- Bit 14~15 : Cache/NVS hardware level

Bit0=1(Serial Channel)

- Bit 1 : Not used
- Bit 2~3 : Strage Path Number
- Bit 4~7 : Channels Per Cluster
  - 0000 : Parallel=4, Serial=0
  - 0001 : Parallel=8, Serial=0
  - 0010 : Parallel=4, Serial=2
  - 0100 : Parallel=4, Serial=4
  - 0110 : Parallel=0, Serial=2
  - 1000 : Parallel=0, Serial=4
  - 1010 : Parallel=0, Serial=8
  - 1100 : Parallel=0, Serial=6
- Bit 8 : Dual Frame
  - 0 : Dual Frame
  - 1 : Modular Power
- Bit 9~11 : Cache size
  - 000 : none Cache
  - 001 : 256MB
  - 010 : 512MB
  - 011 : 768MB
  - 100 : 1024MB
  - 101 : 1280MB
  - 110 : 1536MB
  - 111 : over 1536MB
- Bit 12~13 : Cluster hardware level
- Bit 14~15 : Cache/NVS hardware level

Copyright ©2000, Hitachi, Ltd.

Byte27 = 0A (Bus out parity check/Overrun on LCP interface (Byte3A:b4 = 1)) (1/1)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘0’)				Message (x‘A’)			
28	Command code							
29	Cylinder address							
2A								
2B	Head address							
2C	Record number							
2D	SSID of mate subsystem (x‘0000’ for EDCC)							
2E								
2F	Maker code & Manufacture code (x‘00’)							
30	Module ID							
31	Routine ID							
32	PCB number				BBF OVR	PND OVR	STOP	OVER
33	Not used							
34	SSID of self subsystem							
35								
36	Symptom code (x‘0F0A’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							
40 -7F	Not used							

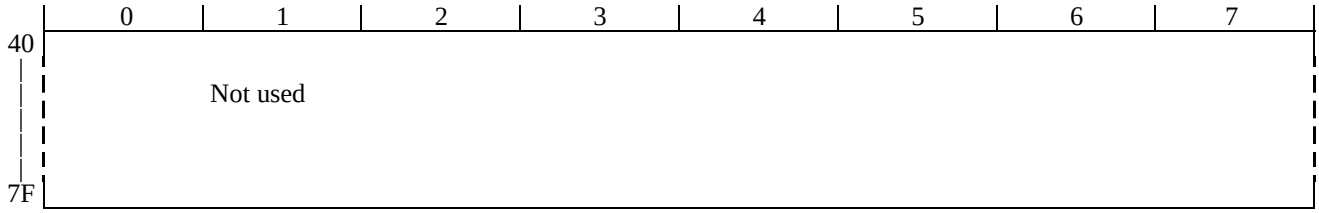
Copyright ©2000, Hitachi, Ltd.

Byte27 = 10 (Intervention required) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘1’)				Message (x‘0’)			
28	Ready	Enable	SSB PEND		Not used (‘00000’)			
29	Not used (x‘00’)							
2A	M.M. RSV	PIN VOL	Not used (‘000000’)					
2B	Host type	DKC type	Not used (‘00’)		DKU type			
2C	Module ID (x‘50’)							
2D	Routine ID (x‘1C’)							
2E	Command code							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							
31	Not used (x‘00’)							
32	PCB number				Not used (x‘0’)			
33	Not used							
34	SSID of self subsystem							
35								
36	Symptom code (x‘9F10’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 10 (Intervention required) (2/2)



Copyright ©2000, Hitachi, Ltd.

Byte27 = 1X (Drive report error) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘1’)				Message (x‘2/4’)			
28	Additional sense code (Note 2)							
29	Additional sense code qualifier (Note 2)							
2A	SCSI Command (Note 3)							
2B	Threshold type (Note 4)							
2C	Module ID							
2D	Routine ID							
2E	Not used (x‘0’)				DKA#			
2F	CDEV#				RDEV#			
30	Type code (‘000’)			0	Sense key (Note 1)			
31	Not used (x‘00’)							
32	Not used (x‘00’)							
33	Not used (x‘00’)							
34	SSID of self subsystem							
35								
36	Symptom code (x‘9F1X’ X:Message)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 1X (Drive report error) (2/2)

	0	1	2	3	4	5	6	7
40		Status byte						
41		Message						
42		CDB						
4B								
4C		SPC status register						
4D		SPC nexus status register						
4E		SPC data block register						
4F								
50		SPC data byte register						
51								
52								
53		SPC SCSI control signal status register						
54		SCSI extended sense data						
73								
74		Not used						
7F								

(Note 1) Sense key
- x‘0’ : No sense
- x‘1’ : Recoverd error
- x‘2’ : Not ready
- x‘3’ : Medium error
- x‘4’ : Hardware error
- x‘5’ : Illigal request
- x‘6’ : Unit attention
- x‘7’ : Data protect
- x‘8’ : Blank check (Not used)
- x‘9’ : Vender unique (Not used)
- x‘A’ : Copy aborted (Not used)
- x‘B’ : Aborted command
- x‘C’ : Equal (Not used)
- x‘D’ : Volume overflow (Not used)
- x‘E’ : Miscompare
- x‘F’ : (Reserved)

(Note 2) See EC = E SSB log.

(Note 3) SCSI command
- x‘00’ : Test unit ready
- x‘03’ : Request sense
- x‘04’ : Format unit
- x‘07’ : Reassign blocks
- x‘12’ : Inquiry
- x‘15’ : Mode serect
- x‘1A’ : Mode sense
- x‘1B’ : Start/stop unit
- x‘1C’ : Recieve diagnostic result
- x‘1D’ : Send diagnostic
- x‘28’ : Read (extend)
- x‘2A’ : Write (extend)
- x‘2E’ : Write and verify
- x‘3B’ : Write buffer

(Note 4) See EC = E SSB log.

Copyright ©2000, Hitachi, Ltd.

Byte27=3F (Reset Allegiance) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x'3')				Message (x'F')			
28	Not used							
29	Logical path number							
2A	DCN status (Note 1)							
2B								
2C	Command code							
2D	SSID of mate subsystem (x'0000' for EDCC)							
2E								
2F	Maker code & Manufacture code (x'00')							
30	Module ID							
31	Routine ID							
32	PCB number							
33	Not used (x'00')							
34	SSID of self subsystem							
35								
36	Symptom code (x'3F3F')							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not used (x'00')							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27=3F (Reset Allegiance) (2/2)

	0	1	2	3	4	5	6	7
40	Not used							
7F								

(Note 1)

	0	1	2	3	4	5	6	7
28	Device busy	ECI	Command chainning	Path reserve	Stack status	Wait SENSE	Long busy	Processor connect
29	Single path mode	Guarant path mode	MCB chainning	0	Block switch	0	0	0

Copyright ©2000, Hitachi, Ltd.

Byte27 = 4X (Data check) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘4’)				Message (x‘X’)			
28	Cylinder address (Note 1)							
29								
2A	Head address (Note 1)							
2B								
2C	Record number (Note 1)							
2D	Sector number (Note 1)							
2E	Controller ID							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							
31	Not used (x‘00’)							
32	PCB number				Not used (x‘0’)			
33	Not used							
34	Command code							
35	SSID (low) of self subsystem							
36	Symptom code (x‘4XYY’) (X:Note 2) (YY:Note 3)							
37								
38	Log and message control (x‘08’)							
39	Program action code (x‘91’)							
3A	Configuration information							
3B								
3C	Not usde (x‘01’)							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 4X (Data check) (2/3)

	0	1	2	3	4	5	6	7
40		Causal Key code						
41		Causal Format/Message						
42		Causal Module ID						
43		Causal Routine ID						
44		LDEV number, slot number						
45								
46								
47								
48		Slot status						
49								
4A								
4B								
4C		staging bit map/Dirty bit map						
4D								
4E								
4F								
50		Current subblock number						
51		EXIT falg (Note 4)						
52		Slot failure information (Note 5)						
53		Obtained information flat (Note 6)						
54		Head subblock number for HIT/MISS decision + Remain subblock count						
55		(when byte36 is x‘40/41/42/43’)/PACC in CBUF (when byte36 is x‘45’)						
56		Not used (when byte36 is x‘40/41/42/43’)/						
57		PAHF in CBUF (when byte36 is x‘45’)						
58		Not used (when byte36 is x‘40/41/42/43’)/						
59		Current CC in JCB (when byte36 is x‘45’)						
5A		Not used (when byte36 is x‘40/41/42/43’)/						
5B		Current HH in JCB (when byte36 is x‘45’)						
5C								
		Reserved						
7F								

(Note 1) Not determined for occurrence in HA or RO

(Note 2) Contents of message

x‘0’ : Data check in HA field
x‘1’ : Data check in C field
x‘2’ : Data check in K field
x‘3’ : Data check in D field
x‘4’ : Missing SYNC byte in HA field
x‘5’ : Missing SYNC byte in C field (PA error)
x‘6’ : Missing SYNC byte in K field
x‘7’ : Missing SYNC byte in D field
x‘8’ : Not used
x‘9’ : Missing AM during retry
x‘A’to x‘F’ : Not used

(Note 3) Contents of correctionflag

Bits 0 and 1 : ECC correction bit
10 : Correctable (Recoverd)
11 : Uncorrectable
Bit 2 : offset activ
Bits 3 to 7 : Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 4X (Data check) (3/3)

(Note 4) EXIT flag

x‘08’ : CHL I/F CHK2 timeover
x‘0D’ : EOF
x‘0E’ : DSB=0E requested
x‘0F’ : Logical error
x‘1E’ : Make sense only
x‘1F’ : Logical error (make sense only)
x‘30’ : Selective reset requested
x‘40’ : ‘Staging’ requested
x‘41’ : ‘Waiting free segment’ requested
x‘42’ : ‘Timeover of waiting for staging’ requested
x‘43’ : ‘Staging for PA unmatch’ requested
x‘45’ : ‘Destaging’ requested
x‘46’ : ‘High priority destaging’ requested
x‘47’ : ‘Pseud-through process’ requested
x‘4B’ : ‘DSB=4E retry’ requested (data transfer)
x‘4E’ : ‘DSB=4E retry’ requested (DSB = 4E retry)
x‘4F’ :STG requested (Read or STG in progress)

(Note 5) Slot failure

x‘80’ : Sector write error
x‘40’ : Sector read error
x‘20’ : ECC/LRC error
x‘10’ : Incomplete data
x‘08’ : No decision

(Note 6) Obtained information flag

bit0-1 : Block type
- 00 : Data block
- 01 : HA/RO block
- 10 : Bit map block

bit2-3 : Side
- 00 : Cache write side
- 01 : NVS write side
- 10 : Cache read side

bit4 : Segment
- 0 :No segment
- 1 :Segment exist

bit5-7 : Reserved

Copyright ©2000, Hitachi, Ltd.

Byte27 = 6X (Statistics) (1/1)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Controller ID							
24	Device address							
25	Command overrun threshold exceeded							
26	Data overrun threshold exceeded							
27	Format (x‘6’)				Message (x‘X’)			
28	Read/search byte count							
29								
2A								
2B								
2C	Seek count							
2D								
2E	Not used (x‘00’)							
2F	Manufacture code (‘000000’)						Factory code (‘00’)	
30	Not used (x‘00’)							
31	DKC serial number							
32								
33								
34	SSID of self SSID							
35								
36	Sympton code (x‘6FXY’ X:0: Statistics/RRBL command, 2: Channel data overrun							
37	Y:CHL# (parallel CHL)/LCP# (serial CHL))							
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00000000’)							
3D								
3E								
3F								
40 -7F	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 74 (SPC report error) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘7’)				Message (x‘4’)			
28	SPC interuption status register (See EC = D SSB log)							
29	SPC comand step register (See EC = D SSB log)							
2A	SCSI command code (See EC = D SSB log)							
2B	Threshold type (See EC = D SSB log)							
2C	Module ID							
2D	Routine ID							
2E	Not used (x‘0’)				DKA number			
2F	CDEV number				RDEV number			
30	Type code (‘111’)		0		Not used (x‘0’)			
31	Not used (x‘00’)							
32	Not used (x‘00’)							
33	Not used (x‘00’)							
34	SSID of self subsystem							
35								
36	Symptom code (x‘DF74’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 74 (SPC report error) (2/2)

	0	1	2	3	4	5	6	7
40		Status by						
41		Message						
42		CDB						
43								
44								
45								
46								
47								
48								
49								
4A								
4B								
4C		SPC status register						
4D		SPC nexus status register						
4E		SPC data block register						
4F								
50		SPC data byte register						
51								
52								
53		SPC SCSI control signal status register						
54		SCA SFC						
55								
56		SCA SFS0						
57								
58		SCA XFS1						
59								
5A		SCA INT						
5B								
5C		SCA SCHK1						
5D								
5E		SCA SCHK20						
5F								
60		SCA SCHK21						
61								
62		SCA SCHK22						
63								
64		SCA SCHK23						
65								
66		SCA SCHK24						
67								
68		SCA SCHK25						
69								
6A		SCA SCACHK2						
6B								
6C		SCA BSACHK2						
6D								
6E		SCA XFS2						
6F								
70		SCA XFS3						
71								
72		Not used						
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = 79 (SCSI bus parity error) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘7’)				Message (x‘9’)			
28	Additional sense code (Note 2)							
29	Additional sense code qualifier (Note 2)							
2A	SCSI Command (Note 3)							
2B	Threshold type (Note 4)							
2C	Module ID							
2D	Routine ID							
2E	Not used (x‘0’)				DKA#			
2F	CDEV#				RDEV#			
30	Type code (‘000’)		0		Sense key (Note 1)			
31	Not used (x‘00’)							
32	Not used (x‘00’)							
33	Not used (x‘00’)							
34	SSID of self subsystem							
35								
36	Symptom code (x‘DF79’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 79 (SCSI bus parity error) (2/2)

	0	1	2	3	4	5	6	7
40		Status byte						
41		Message						
42		CDB						
4B								
4C		SPC status register						
4D		SPC nexus status register						
4E		SPC data block register						
4F								
50		SPC data byte register						
51								
52								
53		SPC SCSI control signal status register						
54		SCSI extended sense data						
73								
74		Not used						
7F								

(Note 1) Sense key
- x‘0’ : No sense
- x‘1’ : Recoverd error
- x‘2’ : Not ready
- x‘3’ : Medium error
- x‘4’ : Hardware error
- x‘5’ : Illigal request
- x‘6’ : Unit attention
- x‘7’ : Data protect
- x‘8’ : Blank check (Not used)
- x‘9’ : Vender unique (Not used)
- x‘A’ : Copy aborted (Not used)
- x‘B’ : Aborted command
- x‘C’ : Equal (Not used)
- x‘D’ : Volume overflow (Not used)
- x‘E’ : Miscompare
- x‘F’ : (Reserved)

(Note 2) See EC = E SSB log.

(Note 3) SCSI command
- x‘00’ : Test unit ready
- x‘03’ : Request sense
- x‘04’ : Format unit
- x‘07’ : Reassign blocks
- x‘12’ : Inquiry
- x‘15’ : Mode serect
- x‘1A’ : Mode sense
- x‘1B’ : Start/stop unit
- x‘1C’ : Recieve diagnostic result
- x‘1D’ : Send diagnostic
- x‘28’ : Read (extend)
- x‘2A’ : Write (extend)
- x‘2E’ : Write and verify
- x‘3B’ : Write buffer

(Note 4) See EC = E SSB log.

Copyright ©2000, Hitachi, Ltd.

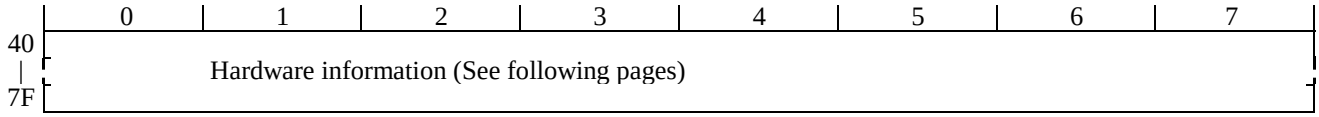
Byte27 = 81 & Byte34:b4-7 = 0 (Shared Memery Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘8’)				Message (x‘1’)			
28	Subcode			(See following pages)				
29	Hardware information			(See following pages)				
2A								
2B								
2C								
2D								
2E								
2F								
30								
31								
32	Not used (x‘00’)							
33	Not used (x‘00’)							
34	PCB number				Message code (x‘0’)			
35	SSID of self subsystem							
36	Symptom code (x‘FF81’ : LDEV type = DKU87I/x‘EF81’ : LDEV type = DKU86I)*							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Copyright ©2000, Hitachi, Ltd.

Byte27 = 81 & Byte34:b4-7 = 0 (Shared Memory Failure) (2/2)



Copyright ©2000, Hitachi, Ltd.

Byte27 = 81 (Shared Memory Failure) Byte28-31 Detail

(1) Byte34, Bit4 to Bit7 = 0: Shared Memory Failure

	0	1	2	3	4	5	6	7
28	Subcode							
	Micro error	MPA error	Shared memory Side A error	Shared memory Side B error	A0 path error	A1 path error	B0 path error	B1 path error
29	Format No.							
	Format No. : x'01': X0A access micro error & MPA internal error x'02': X1A access micro error & MPA internal error x'03': X0A access shared memory error x'04': X1A access shared memory error x'05': X0A access SHSN error x'06': X1A access SHSN error x'07': others error							
2A	MPA:ACSMODE:8200 0650(b00-07)							
	Reserved	Reserved	Reserved	execute face	Reserved	Reserved	Use path 0:use A0 1:use A1	Use path 0:use B0 1:use B1
2B	MPA:ACSMODE:8200 0650(b10-17)							
	Access mode 1	Access mode 2	Access mode 3	Access mode 4	Access mode 5	Access mode 6	Access mode 7	Access mode 8
2C	MPA:CHK3STS:8200 0108(b00-07)							
	XR send parity error	XR recv parity error	MPID unmatch	Access error	compare error	Resource lock mode/ queue error	XR timeout	XR SEQ error
2D	MPA: CHK3STS:8200 0108(b10-17)							
	A0 collect ANYERR	A1 collect ANYERR	B0 collect ANYERR	B1 collect ANYERR	A0 path error	A1 path error	B0 path error	B1 path error
2E	MPA: CHK3STS:8200 0108(b20-27)							
	A0 path timer error	A1 path timer error	B0 path timer error	B1 path timer error	A0 path send parity error	A1 path send parity error	B0 path send parity error	B1 path send parity error
2F	MPA: CHK3STS:8200 0108(b30-37)							
	A0 path recv parity error	A1 path recv parity error	B0 path recv parity error	B1 path recv parity error	A0 path no response	A1 path no response	B0 path no response	B1 path no response
30	MPA:ACSMODE:8200 0650(b20-27)							
	Access mode 9	Access mode 10	Reserved	Reserved	Access patarn 1 SM read	Access patarn 2 SM write	Access patarn 3 SM read (atomic)	Access patarn 4 SM write (atomic)
31	MPA:ACSMODE:8200 0650(b30-37)							
	Access patarn 5 resource lock	Access patarn 6 I/O read	Access patarn 7 I/O write	Access patarn 8 Bcast read	Access patarn 9 Bcast write	Access patarn 10 scan read	Access patarn 11 scan write	Reserved

Copyright ©2000, Hitachi, Ltd.

Byte27 = 81 Byte40-7F (X0A ACCESS MICRO ERROR, X1A ACCESS MICRO ERROR, MPA INTERNAL ERROR)

(Byte29=x'01'|x'02') (1/4)

	0	1	2	3	4	5	6	7
40	MPA :HIN :82000050 (b30 - 37)							
	SMDA majority decision result	SMDA input signal status			SMDB majority decision result	SMDB input signal status		
41	MPA :HOUT :82000054 (b30 - 37)							
	SMDA output result	SMDA individual signal output			SMDB output result	SMDB individual signal output		
42	MPA:RXAER:82000210(b20 - 27)							
	Reserved	Reserved	SHSN_A LRC error	SHSN_A LDT byte parity error	PER_RXER0	PER_RXER1	PER_RXER2	PER_RXER3
					SHSN_A EDT byte parity error			
43	MPA:RXAER:82000210(b30 - 37)							
	Reserved	Reserved	Reserved	SHSN_A SDT byte parity error	PER_RXRD0	PER_RXRD1	PER_RXRD2	PER_RXRD3
					SHSN_A R/W CUDG			
44	MPA:RXBER:82000214(b20 - 27)							
	Reserved	Reserved	SHSN_B LRC error	SHSN_B LDT byte parity error	PER_RXER0	PER_RXER1	PER_RXER2	PER_RXER3
					SHSN_B EDT byte parity error			
45	MPA:RXBER:82000214(b30 - 37)							
	Reserved	Reserved	Reserved	SHSN_B SDT byte parity error	PER_RXRD0	PER_RXRD1	PER_RXRD2	PER_RXRD3
					SHSN_B R/W CUDG			
46	MPA:RXAER1:82000218(b30 - 37)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SHSN_A MPID unmatch
47	MPA:RXBER1:8200021C(b30 - 37)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SHSN_B MPID unmatch
48	MPA:LNEWER : 82000234(b30 - 37)							
	L0LD byte parity error				LNEW byte parity error			
49	MPA:LNEWER1 : 8200023C(b30 - 37)							
	Reserved	Reserved	Reserved	Reserved	LNEW lock byte error	LNEW QUE error 1	LNEW QUE error 2	LNEW QUE error all
4A	MPA:LCTLER:82000230(b30 - 37)							
	Reserved	Reserved	Reserved	Reserved	LCTL byte parity error			
4B	MPA: LCTLER1: 82000238(b30 - 37)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LCTL mode set error	LCTL QUE set error
4C	MPA:SQ0ER:82000260(b30 - 37)							
	XR_IF SEQ#0 SEQ log parity error				Reserved	SEQ divergency error	Reserved	SEQ parity error
4D	MPA:SQ1ER:82000264(b30 - 37)							
	XR_IF SEQ#1 SEQ log parity error				Reserved	SEQ divergency error	Reserved	SEQ parity error
4E	MPA:SQ2ER:82000268(b30 -37)							
	XR_IF SEQ#2 SEQ log parity error				Reserved	SEQ divergency error	Reserved	SEQ parity error
4F	MPA:X1AP:82000614(b30 - 37)							
	Reserved	Reserved	X1LOCK exec face #0 XR log	X1WT exec face #0 XR log	X1AP exec face #0 XR address log byte parity bit			

Copyright ©2000, Hitachi, Ltd.

Byte27 = 81 Byte40-7F(X0A ACCESS MICRO ERROR, X1A ACCESS MICRO ERROR, MPA INTERNAL ERROR)

(Byte29=x'01'|x'02') (2/4)

	0	1	2	3	4	5	6	7
50	MPA:X1A 82000610(b00 - 07)							
	X1A00	X1A01	X1A02	X1A03	X1A04	X1A05	X1A06	X1A07
	X1A = exec face #1 XR address log byte							
51	MPA:X1A 82000610(b10 - 17)							
	X1A10	X1A11	X1A12	X1A13	X1A14	X1A15	X1A16	X1A17
	X1A = exec face #1 XR address log byte							
52	MPA:X1A 82000610(b20 - 27)							
	X1A20	X1A21	X1A22	X1A23	X1A24	X1A25	X1A26	X1A27
	X1A = exec face #1 XR address log byte							
53	MPA:X1A 82000610(b30 - 37)							
	X1A30	X1A31	X1A32	X1A33	X1A34	X1A35	X1A36	X1A37
	X1A = exec face #1 XR address log byte							
54	MPA:ACSER 82000220(b30 -37)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Access pattern error	Access mode error	Access hot line error
55	MPA:TIME0ER 82000250(b30 - 37)							
	Reserved	Reserved	Reserved	Reserved	TIM #0 byte parity error			
56	MPA:A0TXER 8214j000 (b34 - 37)				MPA:A1TXER 8215j000 (b34 - 37)			
	Reserved	Reserved	Send data parity error	Send data LRC error	Reserved	Reserved	Send data parity error	Send data LRC error
57	MPA:B0TXER 8216j000 (b34 - 37)				MPA:B1TXER 8217j000 (b34 - 37)			
	Reserved	Reserved	Send data parity error	Send data LRC error	Reserved	Reserved	Send data parity error	Send data LRC error
58	MPA:MPASTS 82000100 (b30 - 37)							
	MPA interrupt status bit	Master CHK3 status bit	Slave CHK3 status bit	Reserved	PROM_IF CHK1B status bit	COM_IF CHK1B status bit	XR_IF CHK1B status bit	MP interrupt status bit
59	MPA:BMD 82000024 (b30 - 37)							
	Reserved	SM copy mode enable	SM disable side A	SM disable side B	A0 path disable	A1 path disable	B0 path disable	B1 path disable
5A	MPA:X0AP 82000604 (b30 - 37)							
	Reserved	Reserved	X0LOCK exec face#0 XR log	X0WT exec face#0 XR log	X0AP exec face #0 XR address log byte parity bit			
5B	MPA:X0WDP 8200060C (b34 - 37)				MPA:X1WDP 8200061C (b34 - 37)			
	X0WDP exec face #0 XR write-data log byte parity bit				X1WDP exec face #0 XR write-data log byte parity bit			
5C	MPA:X0A 82000600(b00 - 07)							
	X0A00	X0A01	X0A02	X0A03	X0A04	X0A05	X0A06	X0A07
	X0A = exec face #0 XR address log byte							
5D	MPA:X0A 82000600(b10 - 17)							
	X0A10	X0A11	X0A12	X0A13	X0A14	X0A15	X0A16	X0A17
	X0A = exec face #0 XR address log byte							
5E	MPA:X0A 82000600(b20 - 27)							
	X0A20	X0A21	X0A22	X0A23	X0A24	X0A25	X0A26	X0A27
	X0A = exec face #0 XR address log byte							
5F	MPA:X0A 82000600(b30 - 37)							
	X0A30	X0A31	X0A32	X0A33	X0A34	X0A35	X0A36	X0A37
	X0A = exec face #0 XR address log byte							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 81 Byte40-7F(X0A ACCESS MICRO ERROR, X1A ACCESS MICRO ERROR, MPA INTERNAL ERROR)

(Byte29=x'01'|x'02') (3/4)

	0	1	2	3	4	5	6	7
60	MPA:X0WD:82000608 (b00 - 07)							
	X0WD00	X0WD01	X0WD02	X0WD03	X0WD04	X0WD05	X0WD06	X0WD07
	X0WD = exec face #0 XR write-data log byte							
61	MPA:X0WD:82000608 (b10 - 17)							
	X0WD10	X0WD11	X0WD12	X0WD13	X0WD14	X0WD15	X0WD16	X0WD17
	X0WD = exec face #0 XR write-data log byte							
62	MPA:X0WD:82000608 (b20 - 27)							
	X0WD20	X0WD21	X0WD22	X0WD23	X0WD24	X0WD25	X0WD26	X0WD27
	X0WD = exec face #0 XR write-data log byte							
63	MPA:X0WD:82000608 (b30 - 37)							
	X0WD30	X0WD31	X0WD32	X0WD33	X0WD34	X0WD35	X0WD36	X0WD37
	X0WD = exec face #0 XR write-data log byte							
64	MPA:X0WD:82000618 (b00 - 07)							
	X1WD00	X1WD01	X1WD02	X1WD03	X1WD04	X1WD05	X1WD06	X1WD07
	X1WD = exec face #0 XR write-data log byte							
65	MPA:X0WD:82000618 (b10 - 17)							
	X1WD10	X1WD11	X1WD12	X1WD13	X1WD14	X1WD15	X1WD16	X1WD17
	X1WD = exec face #0 XR write-data log byte							
66	MPA:X0WD:82000618 (b20 - 27)							
	X1WD20	X1WD21	X1WD22	X1WD23	X1WD24	X1WD25	X1WD26	X1WD27
	X1WD = exec face #0 XR write-data log byte							
67	MPA:X0WD:82000618 (b30 - 37)							
	X1WD30	X1WD31	X1WD32	X1WD33	X1WD34	X1WD35	X1WD36	X1WD37
	X1WD = exec face #0 XR write-data log byte							
68	MPA:RXA_EDT:82000624 (b00 - 07)							
	MP Status read INT	MP Status read STS flg	MP Status read Valid flg	MP Status read TOV	SCAN INT	SCAN read Data flg	SCAN STS flg	SCAN TOV
69	MPA:RXA_EDT:82000624 (b10 - 17)							
	All lock busy	Memory not Ready	Back up busy	All lock error	Memory disconnect busy	Illegal address error	DIMM Invalid error	Illegal lock error
6A	MPA:RXA_EDT:82000624 (b20 - 27)							
	Request timeout	PRB timeout	Lock wait timeout	Lock off timeout	PRB parity error	Check code error	Path any error	Path board error
6B	MPA:RXA_EDT:82000624 (b30 - 37)							
	Correctable error	Uncorrectable error	I/O register parity error	Reserved	Reserved	SM PS down error	Memory control signal error	Common board error
6C	MPA:A0_path TM0ERR:8214j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6D	MPA:A1_path TM0ERR:8215j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6E	MPA:B0_path TM0ERR:8216j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6F	MPA:B1_path TM0ERR:8217j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1

Copyright ©2000, Hitachi, Ltd.

Byte27 = 81 Byte40-7F(X0A ACCESS MICRO ERROR, X1A ACCESS MICRO ERROR, MPA INTERNAL ERROR)

(Byte29=x'01'|x'02') (4/4)

	0	1	2	3	4	5	6	7
70	MPA:X0ER :82000208 (b20 - 27)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MPID register parity error	LCTL register parity error
71	MPA:X0ER :82000208 (b30 - 37)							
	Input address parity error				Input data parity error			
72	MPA:X1ER :8200020C(b20 - 27)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MPID register parity error	LCTL register parity error
73	MPA:X1ER :8200020C(b30 -37)							
	Input address parity error				Input data parity error			
74	MPA:RXB_EDT:82000634 (b00 - 07)							
	MP Status read INT	MP Status read STS flg	MP Status read Valid flg	MP Status read TOV	SCAN INT	SCAN read Data flg	SCAN STS flg	SCAN TOV
75	MPA:RXB_EDT:82000624 (b10 - 17)							
	All lock busy	Memory not Ready	Back up busy	All lock error	Memory disconnect busy	Illegal address error	DIMM Invalid error	Illegal lock error
76	MPA:RXB_EDT:82000624 (b20 - 27)							
	Request timeout	PRB timeout	Lock wait timeout	Lock off timeout	PRB parity error	Check code error	Path any error	Path board error
77	MPA:RXB_EDT:82000624 (b30 - 37)							
	Correctable error	Uncorrectable error	I/O register parity error	Reserved	Reserved	SM PS down error	Memory control signal error	Common board error
78	MPA :ACSMODE :82000650 (b00 -07)							
	Reserved	Reserved	Reserved	XR access exec face #	Reserved	Reserved	Access path A side	Access path B side
79	MPA :ACSMODE :82000650 (b10 -17)							
	Access mode 1	Access mode 2	Access mode 3	Access mode 4	Access mode 5	Access mode 6	Access mode 7	Access mode 8
7A	MPA :ACSMODE :82000650 (b20 -27)							
	Access mode 9	Access mode 10	Reserved	Reserved	Accesspatarn SM read	Access patarn SM write	Access patarn SM read (atomic)	Access patarn SM write (atomic)
7B	MPA :ACSMODE :82000650 (b30 -37)							
	Access patarn resource lock	Access patarn IO read	Access patarn IO write	Access patarn BCAST read	Access patarn BCAST write	Access patarn SCAN read	Access patarn Scan write	Reserved
7C	MPA :ACSPATH :82000654 (b00 - 07)							
	1st access read access	1st access write access	1st access lock acquire access	1st access lock termination access	1st access use A0 path	1st access use A1 path	1st access use B0 path	1st access use B1 path
7D	MPA :ACSPATH :82000654 (b10 - 17)							
	2nd access read access	2nd access write access	2nd access lock acquire access	2nd access lock termination access	2nd access use A0 path	2nd access use A1 path	2nd access use B0 path	2nd access use B1 path
7E	MPA :ACSPATH :82000654 (b20 - 27)							
	3rd access read access	3rd access write access	3rd access lock acquire access	3rd access lock termination access	3rd access use A0 path	3rd access use A1 path	3rd access use B0 path	3rd access use B1 path
7F	MPA :ACSPATH :82000654 (b30 - 37)							
	4th access read access	4th access write access	4th access lock acquire access	4th access lock termination access	4th access use A0 path	4th access use A1 path	4th access use B0 path	4th access use B1 path

Copyright ©2000, Hitachi, Ltd.

Byte27 = 81 Byte40-7F (X0A ACCESS SM ERROR, X1A ACCESS SM ERROR) (Byte29=x'03'|x'04') (1/4)

	0	1	2	3	4	5	6	7
40	SMA ASIDE:SMA_STS :8280001C (b10 - 17)							
	Reserved	Reserved	Reserved	Reserved	CACHE PK slot signal bit '01' : A side '10' : B side		SM disconnect status bit	SM power down status bit
41	SMA ASIDE:SMA_STS :8280001C (b20 - 27)							
	disconnect request bit	SM self-refresh status bit	SM voltage status bit	LSI voltage status bit	System timer enable status bit	SMA alllock status bit	SM ready status bit	SM LSI blockade status bit
42	SMA ASIDE:SMA_STS :8280001C (b30 - 37)							
	CACHE PK version bit				SMA LSI version bit			
43	SMA ASIDE:PATH0_ERR_DET :82800104(b14 -17)				SMA ASIDE:PATH1_ERR_DET :82800114(b14 -17)			
	Slave_dual lock access error	Double lock error	Lock access counter over error	Reserved	Slave_dual lock access error	Double lock error	Lock access counter over error	Reserved
44	SMA ASIDE: BOARD_ERR_STS : 82800120 (b00 - 07)							
	MCB parity error	MAB parity error	MWB parity error	DIMM select parity error	Path select parity error	RDT latch nothing error	ICB parity error	IAB parity error
45	SMA ASIDE: BOARD _ERR_STS : 82800120 (b10 - 17)							
	IWB parity error	IO path select parity error	PD address output error	Lock address buffer parity error	Lock wait time over	Lock protcol error	Answer PATH ID unmatch error	CACHE slot ID parity error
46	SMA ASIDE: BOARD _ERR_STS : 82800120 (b20 - 27)							
	Clock error	Refresh error	Timer error	Arbiter error	Write sequencer parity error	Read sequencer parity error	Memory sequencer parity error	IO sequencer parity error
47	SMA ASIDE: BOARD _ERR_STS : 82800120 (b30 - 37)							
	ECC generator error	SM data output error	Bus switch error	Valid counter parity error	Scan timeout counter parity error	Scan sequencer error	BCINT output error	SCINT output error
48	SMA ASIDE: BOARD _ERR_DET : 82800124 (b20 - 27)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Memory Arbiter compare error	Lock Arbiter compare error	I/O Arbiter compareerror
49	SMA ASIDE: BOARD _ERR_DET : 82800124 (b30 - 37)							
	Reserved	System clock error	Timer clock error	Clock frequency error	Reserved	Memory initialize parity error	Refresh counter parity error	No refresh action detected
4A	SMA ASIDE :DIMM_SIG_ERR_DIMM : 8280012C(b30 - 37)							
	DIMM 0	DIMM 1	DIMM 2	DIMM 3	DIMM 4	DIMM 5	Reserved	Reserved
	DIMM error status bit when DIMM controll error detected							
4B	SMA ASIDE :UNCOR_ERR_DIMM : 82800130(b30 - 37)							
	DIMM 0	DIMM 1	DIMM 2	DIMM 3	DIMM 4	DIMM 5	Reserved	Reserved
	DIMM error status bit when uncorrectable error detected							
4C	SMA BSIDE :SMA_STS :82A0001C (b10 - 17)							
	Reserved	Reserved	Reserved	Reserved	CACHE PK slot signal bit '01' : A side '10' : B side		SM disconnect status bit	SM power down status bit
4D	SMA BSIDE :SMA_STS : 82A 0001C (b20 - 27)							
	disconnect request bit	SM self-refresh status bit	SM voltage status bit	LSI voltage status bit	System timer enable status bit	SMA alllock status bit	SM ready status bit	SM LSI blockade status bit
4E	SMA BSIDE :SMA_STS : 82A 0001C (b30 - 37)							
	CACHE PK version bit				SMA LSI version bit			
4F	SMA BSIDE :PATH0 ERR_DET : 82A 00104 (b14 - 17)				SMA BSIDE :PATH1 ERR_DET : 82A 00114 (b14 - 17)			
	Slave_dual lock access error	Double lock error	Lock access counter over error	Reserved	Slave_dual lock access error	Double lock error	Lock access counter over error	Reserved

Copyright ©2000, Hitachi, Ltd.

Byte27 = 81 Byte40-7F (X0A ACCESS SM ERROR, X1A ACCESS SM ERROR) (Byte29=x'03'|x'04') (2/4)

	0	1	2	3	4	5	6	7
50	SMA BSIDE: BOARD_ERR_STS :82A00120 (b00 - 07)							
	MCB parity error	MAB parity error	MWB parity error	DIMM select parity error	Path select parity error	RDT latch nothing error	ICB parity error	IAB parity error
51	SMA BSIDE: BOARD_ERR_STS :82A00120 (b10 - 17)							
	IWB parity error	IO path select parity error	PD address output error	Lock address buffer parity error	Lock wait time over	Lock protcol error	Answer PATH ID unmatch error	CACHE slot ID parity error
52	SMA BSIDE: BOARD_ERR_STS :82A00120 (b20 - 27)							
	Clock error	Refresh error	Timer error	Arbiter error	Write sequencer parity error	Read sequencer parity error	Memory sequencer parity error	IO sequencer parity error
53	SMA BSIDE: BOARD_ERR_STS :82A00120 (b30 - 37)							
	ECC generator error	SM data output error	Bus switch error	Valid counter parity error	Scan timeout counter parity error	Scan sequencer error	BCINT output error	SCINT output error
54	SMA BSIDE: BOARD_ERR_DET :82A00124 (b20 - 27)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Arbiter compare error	Arbiter compare error	Arbiter compareerror
55	SMA BSIDE: BOARD_ERR_DET :82A00124 (b30 - 37)							
	Reserved	System clock error	Timer clock error	Clock frequency error	Reserved	Memory Arbiter compare error	Lock Arbiter compare error	I/O Arbiter compareerror
56	SMA BSIDE :DIMM_SIG_ERR_DIMM :82A0012C(b30 - 37)							
	DIMM 0	DIMM 1	DIMM 2	DIMM 3	DIMM 4	DIMM 5	Reserved	Reserved
	DIMM error status bit when DIMM controll error detected							
57	SMA BSIDE :UNCOR_ERR_DIMM :82A00130(b30 - 37)							
	DIMM 0	DIMM 1	DIMM 2	DIMM 3	DIMM 4	DIMM 5	Reserved	Reserved
	DIMM error status bit when uncorrectable error detected							
58	MPA:MPASTS 82000100 (b30 - 37)							
	MPA interrupt status bit	Master CHK3 status bit	Slave CHK3 status bit	Reserved	PROM_IF CHK1B status bit	COM_IF CHK1B status bit	XR_IF CHK1B status bit	MP interrupt status bit
59	MPA:BMD 82000024 (b30 - 37)							
	Reserved	SM copy mode enable	SM disable side A	SM disable side B	A0 path disable	A1 path disable	B0 path disable	B1 path disable
5A	MPA:X0AP 82000604 (b30 - 37)/X1AP 82000614 (b30-37)							
	Reserved	Reserved	X0/1LOCK exec face#0 XR log	X0/1WT exec face#0 XR log	X0AP exec face #0/ X1AP exec face #0 XR address log byte parity bit			
5B	MPA:X0WDP 8200060C (b34 - 37) / MPA:X1WDP 8200061C (b34 - 37)				MPA:TIMEOUT 82000240 (b34 - 37)			
	X0WDP exec face #0 or X1WDP exec face #0 XR write-data log byte parity bit				Reserved	Reserved	Reserved	time out
5C	MPA:X0A 82000600(b00 - 07)/ X1A 82000610(b00 - 07) or MPA:LADR 82000044(b00 - 07)							
	X0A00	X0A01	X0A02	X0A03	X0A04	X0A05	X0A06	X0A07
	X0A = exec face #0 XR address log byte							
5D	MPA:X0A 82000600(b10 - 17)/ X1A 82000610(b10 - 17) or MPA:LADR 82000044(b10 - 17)							
	X0A10	X0A11	X0A12	X0A13	X0A14	X0A15	X0A16	X0A17
	X0A = exec face #0 XR address log byte							
5E	MPA:X0A 82000600(b20 - 27)/ X1A 82000610(b20 - 27) or MPA:LADR 82000044(b20 - 27)							
	X0A20	X0A21	X0A22	X0A23	X0A24	X0A25	X0A26	X0A27
	X0A = exec face #0 XR address log byte							
5F	MPA:X0A 82000600(b30 - 37)/ X1A 82000610(b30 - 37) or MPA:LADR 82000044(b30 - 37)							
	X0A30	X0A31	X0A32	X0A33	X0A34	X0A35	X0A36	X0A37
	X0A = exec face #0 XR address log byte							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 81 Byte40-7F (,w0,` ACCESS SM ERROR, X1A ACCESS SM ERROR) (Byte29=x'03'|x'04') (3/4)

	0	1	2	3	4	5	6	7
60	MPA:X0WD 82000608(b00 - 07)/ X1WD 82000618(b00 - 07) or MPA:LNEW 8200004C(b00 - 07)							
	X0WD00	X0WD01	X0WD02	X0WD03	X0WD04	X0WD05	X0WD06	X0WD07
	X0WD = exec face #0 XR write-data log byte							
61	MPA:X0WD 82000608(b10 - 17)/ X1WD 82000618(b10 - 17) or MPA:LNEW 8200004C(b10 - 17)							
	X0WD10	X0WD11	X0WD12	X0WD13	X0WD14	X0WD15	X0WD16	X0WD17
	X0WD = exec face #0 XR write-data log byte							
62	MPA:X0WD 82000608(b20 - 27)/ X1WD 82000618(b20 - 27) or MPA:LNEW 8200004C(b20 - 27)							
	X0WD20	X0WD21	X0WD22	X0WD23	X0WD24	X0WD25	X0WD26	X0WD27
	X0WD = exec face #0 XR write-data log byte							
63	MPA:X0WD 82000608(b30 - 37)/ X1WD 82000618(b30 - 37) or MPA:LNEW 8200004C(b30 - 37)							
	X0WD30	X0WD31	X0WD32	X0WD33	X0WD34	X0WD35	X0WD36	X0WD37
	X0WD = exec face #0 XR write-data log byte							
64	MPA:RXA_RDT:82000620 (b00 - 07)							
	RXA_RD00	RXA_RD01	RXA_RD02	RXA_RD03	RXA_RD04	RXA_RD05	RXA_RD06	RXA_RD07
	SHSN_A recv-data log read data byte							
65	MPA:RXA_RDT:82000620 (b10 - 17)							
	RXA_RD10	RXA_RD11	RXA_RD12	RXA_RD13	RXA_RD14	RXA_RD15	RXA_RD16	RXA_RD17
	SHSN_A recv-data log read data byte							
66	MPA:RXA_RDT:82000620 (b20 - 27)							
	RXA_RD20	RXA_RD21	RXA_RD22	RXA_RD23	RXA_RD24	RXA_RD25	RXA_RD26	RXA_RD27
	SHSN_A recv-data log read data byte							
67	MPA:RXA_RDT:82000620 (b30 - 37)							
	RXA_RD30	RXA_RD31	RXA_RD32	RXA_RD33	RXA_RD34	RXA_RD35	RXA_RD36	RXA_RD37
	SHSN_A recv-data log read data byte							
68	MPA:RXA_EDT:82000624 (b00 - 07)							
	MP Status read INT	MP Status read STS flg	MP Status read Valid flg	MP Status read TOV	SCAN INT	SCAN read Data flg	SCAN STS flg	SCAN TOV
69	MPA:RXA_EDT:82000624 (b10 - 17)							
	All lock busy	Memory not Ready	Back up busy	All lock error	Memory disconnect busy	Illegal address error	DIMM Invalid error	Illegal lock error
6A	MPA:RXA_EDT:82000624 (b20 - 27)							
	Request timeout	PRB timeout	Lock wait timeout	Lock off timeout	PRB parity error	Check code error	Path any error	Path board error
6B	MPA:RXA_EDT:82000624 (b30 - 37)							
	Correctable error	Uncorrectable error	I/O register parity error	Reserved	Reserved	SM PS down error	Memory control signal error	Common board error
6C	MPA:A0_Path TM0ERR:8214j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6D	MPA:A1_Path TM0ERR:8215j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6E	MPA:B0_Path TM0ERR:8216j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6F	MPA:B1_Path TM0ERR:8217j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1

Copyright ©2000, Hitachi, Ltd.

Byte27 = 81 Byte40-7F (X0A ACCESS SM ERROR, X1A ACCESS SM ERROR) (Byte29=x'03'|x'04') (4/4)

	0	1	2	3	4	5	6	7
70	MPA: RXB_RDT :82000630 (b00 - 07)							
	RXB_RD00	RXB_RD01	RXB_RD02	RXB_RD03	RXB_RD04	RXB_RD05	RXB_RD06	RXB_RD07
	SHSN_B recv-data log read data byte							
71	MPA: RXB_RDT :82000630 (b10 - 17)							
	RXB_RD10	RXB_RD11	RXB_RD12	RXB_RD13	RXB_RD14	RXB_RD15	RXB_RD16	RXB_RD17
	SHSN_B recv-data log read data byte							
72	MPA: RXB_RDT :82000630 (b20 - 27)							
	RXB_RD20	RXB_RD21	RXB_RD22	RXB_RD23	RXB_RD24	RXB_RD25	RXB_RD26	RXB_RD27
	SHSN_B recv-data log read data byte							
73	MPA: RXB_RDT :82000630 (b30 - 37)							
	RXB_RD30	RXB_RD31	RXB_RD32	RXB_RD33	RXB_RD34	RXB_RD35	RXB_RD36	RXB_RD37
	SHSN_B recv-data log read data byte							
74	MPA:RXB_EDT:82000634 (b00 - 07)							
	MP Status read INT	MP Status read STS flg	MP Status read Valid flg	MP Status read TOV	SCAN INT	SCAN read Data flg	SCAN STS flg	SCAN TOV
75	MPA:RXB_EDT:82000634 (b10 - 17)							
	All lock busy	Memory not Ready	Back up busy	All lock error	Memory disconnect busy	Illegal address error	DIMM Invalid error	Illegal lock error
76	MPA:RXB_EDT:82000634 (b20 - 27)							
	Request timeout	PRB timeout	Lock wait timeout	Lock off timeout	PRB parity error	Check code error	Path any error	Path board error
77	MPA:RXB_EDT:82000634 (b30 - 37)							
	Correctable error	Uncorrectable error	I/O register parity error	Reserved	Reserved	SM PS down error	Memory control signal error	Common board error
78	MPA :ACSMODE :82000650 (b00 -07)							
	Reserved	Reserved	Reserved	XR access exec face #	Reserved	Reserved	Access path A side	Access path B side
79	MPA :ACSMODE :82000650 (b10 -17)							
	Access mode 1	Access mode 2	Access mode 3	Access mode 4	Access mode 5	Access mode 6	Access mode 7	Access mode 8
7A	MPA :ACSMODE :82000650 (b20 -27)							
	Access mode 9	Access mode 10	Reserved	Reserved	Accesspattern SM read	Accesspattern SM write	Accesspattern SM read (atomic)	Accesspattern SM write (atomic)
7B	MPA :ACSMODE :82000650 (b30 -37)							
	Accesspattern resource lock	Accesspattern IO read	Accesspattern IO write	Accesspattern BCAST read	Accesspattern BCAST write	Accesspattern SCAN read	Accesspattern Scan write	Reserved
7C	MPA :ACSPATH :82000654 (b00 - 07)							
	1st access read access	1st access write access	1st access lock acquire access	1st access lock termination access	1st access use A0 path	1st access use A1 path	1st access use B0 path	1st access use B1 path
7D	MPA :ACSPATH :82000654 (b10 - 17)							
	2nd access read access	2nd access write access	2nd access lock acquire access	2nd access lock termination access	2nd access use A0 path	2nd access use A1 path	2nd access use B0 path	2nd access use B1 path
7E	MPA :ACSPATH :82000654 (b20 - 27)							
	3rd access read access	3rd access write access	3rd access lock acquire access	3rd access lock termination access	3rd access use A0 path	3rd access use A1 path	3rd access use B0 path	3rd access use B1 path
7F	MPA :ACSPATH :82000654 (b30 - 37)							
	4th access read access	4th access write access	4th access lock acquire access	4th access lock termination access	4th access use A0 path	4th access use A1 path	4th access use B0 path	4th access use B1 path

Copyright ©2000, Hitachi, Ltd.

Byte27 = 81 Byte40-7F (X0A ACCESS HSN ERROR, X1A ACCESS HSN ERROR) (Byte29=x'05'|x'06') (1/4)

	0	1	2	3	4	5	6	7
40	SMA ASIDE:SMA_STS :8280001C (b10 - 17)							
	Reserved	Reserved	Reserved	Reserved	CACHE PK slot signal bit '01' : A side '10' : B side		SM disconnect status bit	SM power down status bit
41	SMA ASIDE:SMA_STS :8280001C (b20 - 27)							
	disconnect request bit	SM self-refresh status bit	SM voltage status bit	LSI voltage status bit	System timer enable status bit	SMA alllock status bit	SM ready status bit	SM LSI blockade status bit
42	SMA ASIDE:SMA_STS :8280001C (b30 - 37)							
	CACHE PK version bit				SMA LSI version bit			
43								
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
44	SMA ASIDE: PATH0_ERR_DET :82800104 (b00 - 07)							
	HSN recv command parity error	HSN recv address parity error	HSN recv write data parity error	Reserved	HSN recv sync0 under run error	HSN recv sync1 under run error	HSN recv sync0 over run error	HSN recv sync1 over run error
45	SMA ASIDE: PATH0_ERR_DET :82800104 (b10 - 17)							
	Recv data LRC error	LRC byte check inconsist	Command lock/unlock '0' or '1'	Command read/write bit '0' or '1'	Slave-dual lock access error	Double lock error	Lock access count over error	Reserved
46	SMA ASIDE: PATH0_ERR_DET :82800104 (b20 - 27)							
	Command bit parity generator error	Address bit parity generator error	Data bit parity generator error	Path command buffer parity error	Path address buffer parity error	Path write data buffer parity error	Path command lock/unlock bit ON	Path command read/write bit ON
47	SMA ASIDE: PATH0_ERR_DET :82800104 (b30 - 37)							
	Reserved	Reserved	lock under no lock request	common path self-path compare error	Reserved	Path sequencer parity error	Request tineout count parity error	Lock timeout count parity error
48	SMA ASIDE: PATH1_ERR_DET :82800114 (b00 - 07)							
	HSN recv command parity error	HSN recv address parity error	HSN recv write data parity error	Reserved	HSN recv sync0 under run error	HSN recv sync1 under run error	HSN recv sync0 over run error	HSN recv sync1 over run error
49	SMA ASIDE: PATH1_ERR_DET :82800114 (b10 - 17)							
	Recv data LRC	LRC byte check inconsist	Command lock/unlock '0' or '1'	Command read/write bit '0' or '1'	Slave-dual lock access error	Double lock error	Lock access count over error	Reserved
4A	SMA ASIDE :PATH1_ERR_DET :82800114 (b20 - 27)							
	Command bit parity generator error	Address bit parity generator error	Data bit parity generator error	Path command buffer parity error	Path address buffer parity error	Path write data buffer parity error	Path command lock/unlock bit ON	Path command read/write bit ON
4B	SMA ASIDE :PATH1_ERR_DET :82800114 (b30 - 37))							
	Reserved	Reserved	lock under no lock request	common path self-path compare error	Reserved	Path sequencer parity error	Request tineout count parity error	Lock timeout count parity error
4C	SMA BSIDE :SMA_STS :82A0001C (b10 - 17)							
	Reserved	Reserved	Reserved	Reserved	CACHE PK slot signal bit '01' : A side '10' : B side		SM disconnect status bit	SM power down status bit
4D	SMA BSIDE :SMA_STS :82A0001C (b20 - 27)							
	disconnect request bit	SM self-refresh status bit	SM voltage status bit	LSI voltage status bit	System timer enable status bit	SMA alllock status bit	SM ready status bit	SM LSI blockade status bit
4E	SMA BSIDE :SMA_STS :82A0001C (b30 - 37)							
	CACHE PK version bit				SMA LSI version bit			
4F								
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Copyright ©2000, Hitachi, Ltd.

Byte27 = 81 Byte40-7F (X0A ACCESS HSN ERROR, X1A ACCESS HSN ERROR) (Byte29=x'05'|x'06') (2/4)

	0	1	2	3	4	5	6	7
50	SMA BSIDE: PATH0_ERR_DET :82A00104 (b00 - 07)							
	HSN recv command parity error	HSN recv address parity error	HSN recv write data parity error	Reserved	HSN recv sync0 under run error	HSN recv sync1under run error	HSN recv sync0 over run error	HSN recv sync1over run error
51	SMA BSIDE: PATH0_ERR_DET :82A00104 (b10 - 17)							
	Recv data LRC	LRC byte check inconsist	Command lock/unlock '0' or '1'	Command read/write bit '0' or '1'	Slave-dual lock access error	Double lock error	Lock access count over error	Reserved
52	SMA BSIDE: PATH0_ERR_DET :82A00104 (b20 - 27)							
	Command bit parity generator error	Address bit parity generator error	Data bit parity generator error	Path command buffer parity error	Path address buffer parity error	Path write data buffer parity error	Path command lock/unlock bit ON	Path command read/write bit ON
53	SMA BSIDE: PATH0_ERR_DET :82A00104 (b30 - 37)							
	Reserved	Reserved	lock under no lock request	common path self path compare err	Reserved	Path sequencer parity error	Request tineout count parity error	Lock timeout count parity error
54	SMA BSIDE: PATH1_ERR_DET :82A00114 (b00 - 07)							
	HSN recv command parity error	HSN recv address parity error	HSN recv write data parity error	Reserved	HSN recv sync0 under run error	HSN recv sync1under run error	HSN recv sync0 over run error	HSN recv sync1over run error
55	SMA BSIDE: PATH1_ERR_DET :82A00114 (b10 - 17)							
	Recv data LRC	LRC byte check inconsist	Command lock/unlock '0' or '1'	Command read/write bit '0' or '1'	Slave-dual lock access error	Double lock error	Lock access count over error	Reserved
56	SMA BSIDE :PATH1_ERR_DET :82A00114(b20 - 27)							
	Command bit parity generator error	Address bit parity generator error	Data bit parity generator error	Path command buffer parity error	Path address buffer parity error	Path write data buffer parity error	Path command lock/unlock bit ON	Path command read/write bit ON
57	SMA BSIDE :PATH1_ERR_DET :82A00114(b30 - 37)							
	Reserved	Reserved	lock under no lock request	common path self path compare err	Reserved	Path sequencer parity error	Request tineout count parity error	Lock timeout count parity error
58	MPA:MPASTS 82000100 (b30 - 37)							
	MPA interrupt status bit	Master CHK3 status bit	Slave CHK3 status bit	Reserved	PROM_IF CHK1B status bit	COM_IF CHK1B status bit	XR_IF CHK1B status bit	MP interrupt status bit
59	MPA:BMD 82000024 (b30 - 37)							
	Reserved	SM copy mode enable	SM disable side A	SM disable side B	A0 path disable	A1 path disable	B0 path disable	B1 path disable
5A	MPA:X0AP 82000604 (b30 - 37)/ MPA:X1AP 82000614 (b30 - 37)							
	Reserved	Reserved	X0/1LOCK exec face#0	X0/1WT exec face#0	X0AP exec face #0/ X1AP exec face #0 XR address log byte parity bit			
5B	MPA:X0WDP 8200060C (b34 - 37) / MPA:X1WDP 8200061C (b34 - 37)				MPA:TIMEOUT 82000240 (b34 - 37)			
	X0WDP exec face #0 /X1WDP exec face #0 XR write-data log byte parity bit				Reserved	Reserved	Reserved	time out
5C	MPA:X0A 82000600(b00 - 07)/ X1A 82000610(b00 - 07) or MPA:LADR 82000044(b00 - 07)							
	X0A00	X0A01	X0A02	X0A03	X0A04	X0A05	X0A06	X0A07
	X0A = exec face #0 XR address log byte							
5D	MPA:X0A 82000600(b10 - 17)/ X1A 82000610(b10 - 17) or MPA:LADR 82000044(b10 - 17)							
	X0A10	X0A11	X0A12	X0A13	X0A14	X0A15	X0A16	X0A17
	X0A = exec face #0 XR address log byte							
5E	MPA:X0A 82000600(b20 - 27)/ X1A 82000610(b20 - 27) or MPA:LADR 82000044(b20 - 27)							
	X0A20	X0A21	X0A22	X0A23	X0A24	X0A25	X0A26	X0A27
	X0A = exec face #0 XR address log byte							
5F	MPA:X0A 82000600(b30 - 37)/ X1A 82000610(b30 - 37) or MPA:LADR 82000044(b30 - 47)							
	X0A30	X0A31	X0A32	X0A33	X0A34	X0A35	X0A36	X0A37
	X0A = exec face #0 XR address log byte							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 81 Byte40-7F (X0A ACCESS HSN ERROR, X1A ACCESS HSN ERROR) (Byte29=x'05'|x'06') (3/4)

	0	1	2	3	4	5	6	7
60	MPA:X0WD 82000608(b00 - 07)/ X1WD 82000618(b00 - 07) or MPA:LNEW 8200004C(b00 - 07)							
	X0WD00	X0WD01	X0WD02	X0WD03	X0WD04	X0WD05	X0WD06	X0WD07
	X0WD = exec face #0 XR write-data log byte							
61	MPA:X0WD 82000608(b10 - 17)/ X1WD 82000618(b10 - 17) or MPA:LNEW 8200004C(b10 - 17)							
	X0WD10	X0WD11	X0WD12	X0WD13	X0WD14	X0WD15	X0WD16	X0WD17
	X0WD = exec face #0 XR write-data log byte							
62	MPA:X0WD 82000608(b20 - 27)/ X1WD 82000618(b20 - 27) or MPA:LNEW 8200004C(b20 - 27)							
	X0WD20	X0WD21	X0WD22	X0WD23	X0WD24	X0WD25	X0WD26	X0WD27
	X0WD = exec face #0 XR write-data log byte							
63	MPA:X0WD 82000608(b30 - 37)/ X1WD 82000618(b30 - 37) or MPA:LNEW 8200004C(b30 - 37)							
	X0WD30	X0WD31	X0WD32	X0WD33	X0WD34	X0WD35	X0WD36	X0WD37
	X0WD = exec face #0 XR write-data log byte							
64	MPA:RXA_RDT:82000620 (b00 - 07)							
	RXA_RD00	RXA_RD01	RXA_RD02	RXA_RD03	RXA_RD04	RXA_RD05	RXA_RD06	RXA_RD07
	SHSN_A recv-data log read data byte							
65	MPA:RXA_RDT:82000620 (b10 - 17)							
	RXA_RD10	RXA_RD11	RXA_RD12	RXA_RD13	RXA_RD14	RXA_RD15	RXA_RD16	RXA_RD17
	SHSN_A recv-data log read data byte							
66	MPA:RXA_RDT:82000620 (b20 - 27)							
	RXA_RD20	RXA_RD21	RXA_RD22	RXA_RD23	RXA_RD24	RXA_RD25	RXA_RD26	RXA_RD27
	SHSN_A recv-data log read data byte							
67	MPA:RXA_RDT:82000620 (b30 - 37)							
	RXA_RD30	RXA_RD31	RXA_RD32	RXA_RD33	RXA_RD34	RXA_RD35	RXA_RD36	RXA_RD37
	SHSN_A recv-data log read data byte							
68	MPA:RXA_EDT:82000624 (b00 - 07)							
	MP Status read INT	MP Status read STS flg	MP Status read Valid flg	MP Status read TOV	SCAN INT	SCAN read Data flg	SCAN STS flg	SCAN TOV
69	MPA:RXA_EDT:82000624 (b10 - 17)							
	All lock busy	Memory not Ready	Back up busy	All lock error	Memory disconnect busy	Illegal address error	DIMM Invalid error	Illegal lock error
6A	MPA:RXA_EDT:82000624 (b20 - 27)							
	Request timeout	PRB timeout	Lock wait timeout	Lock off timeout	PRB parity error	Check code error	Path any error	Path board error
6B	MPA:RXA_EDT:82000624 (b30 - 37)							
	Correctable error	Uncorrectable error	I/O register parity error	Reserved	Reserved	SM PS down error	Memory control signal error	Common board error
6C	MPA:A0_Path TM0ERR:8214j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6D	MPA:A1_Path TM0ERR:8215j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6E	MPA:B0_Path TM0ERR:8216j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6F	MPA:B1_Path TM0ERR:8217j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1

Copyright ©2000, Hitachi, Ltd.

Byte27 = 81 Byte40-7F (X0A ACCESS HSN ERROR, X1A ACCESS HSN ERROR) (Byte29=x'05'|x'06') (4/4)

	0	1	2	3	4	5	6	7
70	MPA: RXB_RDT :82000630 (b00 - 07)							
	RXB_RD00	RXB_RD01	RXB_RD02	RXB_RD03	RXB_RD04	RXB_RD05	RXB_RD06	RXB_RD07
	SHSN_B recv-data log read data byte							
71	MPA: RXB_RDT :82000630 (b10 - 17)							
	RXB_RD10	RXB_RD11	RXB_RD12	RXB_RD13	RXB_RD14	RXB_RD15	RXB_RD16	RXB_RD17
	SHSN_B recv-data log read data byte							
72	MPA: RXB_RDT :82000630 (b20 - 27)							
	RXB_RD20	RXB_RD21	RXB_RD22	RXB_RD23	RXB_RD24	RXB_RD25	RXB_RD26	RXB_RD27
	SHSN_B recv-data log read data byte							
73	MPA: RXB_RDT :82000630 (b30 - 37)							
	RXB_RD30	RXB_RD31	RXB_RD32	RXB_RD33	RXB_RD34	RXB_RD35	RXB_RD36	RXB_RD37
	SHSN_B recv-data log read data byte							
74	MPA:RXB_EDT:82000634 (b00 - 07)							
	MP Status read INT	MP Status read STS flg	MP Status read Valid flg	MP Status read TOV	SCAN INT	SCAN read Data flg	SCAN STS flg	SCAN TOV
75	MPA:RXB_EDT:82000634 (b10 - 17)							
	All lock busy	Memory not Ready	Back up busy	All lock error	Memory disconnect busy	Illegal address error	DIMM Invalid error	Illegal lock error
76	MPA:RXB_EDT:82000634 (b20 - 27)							
	Request timeout	PRB timeout	Lock wait timeout	Lock off timeout	PRB parity error	Check code error	Path any error	Path board error
77	MPA:RXB_EDT:82000634 (b30 - 37)							
	Correctable error	Uncorrectable error	I/O register parity error	Reserved	Reserved	SM PS down error	Memory control signal error	Common board error
78	MPA :ACSMODE :82000650 (b00 -07)							
	Reserved	Reserved	Reserved	XR access exec face #	Reserved	Reserved	Access path A side	Access path B side
79	MPA :ACSMODE :82000650 (b10 -17)							
	Access mode 1	Access mode 2	Access mode 3	Access mode 4	Access mode 5	Access mode 6	Access mode 7	Access mode 8
7A	MPA :ACSMODE :82000650 (b20 -27)							
	Access mode 9	Access mode 10	Reserved	Reserved	Accesspatarn SM read	Access patarn SM write	Access patarn SM read (atomic)	Access patarn SM write (atomic)
7B	MPA :ACSMODE :82000650 (b30 -37)							
	Access patarn resource lock	Access patarn IO read	Access patarn IO write	Access patarn BCAST read	Access patarn BCAST write	Access patarn SCAN read	Access patarn Scan write	Reserved
7C	MPA :ACSPATH :82000654 (b00 - 07)							
	1st access read access	1st access write access	1st access lock acquire access	1st access lock termination access	1st access use A0 path	1st access use A1 path	1st access use B0 path	1st access use B1 path
7D	MPA :ACSPATH :82000654 (b10 - 17)							
	2nd access read access	2nd access write access	2nd access lock acquire access	2nd access lock termination access	2nd access use A0 path	2nd access use A1 path	2nd access use B0 path	2nd access use B1 path
7E	MPA :ACSPATH :82000654 (b20 - 27)							
	3rd access read access	3rd access write access	3rd access lock acquire access	3rd access lock termination access	3rd access use A0 path	3rd access use A1 path	3rd access use B0 path	3rd access use B1 path
7F	MPA :ACSPATH :82000654 (b30 - 37)							
	4th access read access	4th access write access	4th access lock acquire access	4th access lock termination access	4th access use A0 path	4th access use A1 path	4th access use B0 path	4th access use B1 path

Copyright ©2000, Hitachi, Ltd.

Byte27 = 81 Byte40-7F (OTHER ERROR) (Byte29=x'07') (1/4)

	0	1	2	3	4	5	6	7
40	SMA ASIDE:SMA_STS :8280001C (b10 - 17)							
	Reserved	Reserved	Reserved	Reserved	CACHE PK slot signal bit '01' : A side '10' : B side		SM disconnect status bit	SM power down status bit
41	SMA ASIDE:SMA_STS :8280001C (b20 - 27)							
	disconnect request bit	SM self-refresh status bit	SM voltage status bit	LSI voltage status bit	System timer enable status bit	SMA all lock status bit	SM ready status bit	SM LSI blockade status bit
42	SMA ASIDE:SMA_STS :8280001C (b30 - 37)							
	CACHE PK version bit				SMA LSI version bit			
43	SMA ASIDE: UNCOR_ERR_DIMM:82800130 (b30 - 37)							
	DIMM00	DIMM01	DIMM02	DIMM03	DIMM04	DIMM05	Reserved	Reserved
	DIMM error status bit when uncorrectable error detected							
44	SMA ASIDE: PATH0_ERR_DET :82800104 (b00 - 07)							
	HSN recv command parity error	HSN recv address parity error	HSN recv write data parity error	Reserved	HSN recv sync0 under run error	HSN recv sync1under run error	HSN recv sync0 over run error	HSN recv sync1over run error
45	SMA ASIDE: PATH0_ERR_DET :82800104 (b10 - 17)							
	Recv data LRC	LRC byte check inconsist	Command lock/unlock '0' or '1'	Command read/write bit '0' or '1'	Slave-dual lock access error	Double lock error	Lock access count over error	Reserved
46	SMA ASIDE: PATH0_ERR_DET :82800104 (b20 - 27)							
	Command bit parity generator error	Address bit parity generator error	Data bit parity generator error	Path command buffer parity error	Path address buffer parity error	Path write data buffer parity error	Path command lock/unlock bit ON	Path command read/write bit ON
47	SMA ASIDE: PATH0_ERR_DET :82800104 (b30 - 37)							
	Reserved	Reserved	lock under no lock request	common path self path compare error	Reserved	Path sequencer parity error	Request tineout count parity error	Lock timeout count parity error
48	SMA ASIDE: PATH1_ERR_DET :82800114 (b00 - 07)							
	HSN recv command parity error	HSN recv address parity error	HSN recv write data parity error	Reserved	HSN recv sync0 under run error	HSN recv sync1under run error	HSN recv sync0 over run error	HSN recv sync1over run error
49	SMA ASIDE: PATH1_ERR_DET :82800114 (b10 - 17)							
	Recv data LRC	LRC byte check inconsist	Command lock/unlock '0' or '1'	Command read/write bit '0' or '1'	Slave-dual lock access error	Double lock error	Lock access count over error	Reserved
4A	SMA ASIDE :PATH1_ERR_DET :82800114 (b20 - 27)							
	Command bit parity generator error	Address bit parity generator error	Data bit parity generator error	Path command buffer parity error	Path address buffer parity error	Path write data buffer parity error	Path command lock/unlock bit ON	Path command read/write bit ON
4B	SMA ASIDE :PATH1_ERR_DET :82800114 (b30 - 37))							
	Reserved	Reserved	lock under no lock request	common path self path compare error	Reserved	Path sequencer parity error	Request tineout count parity error	Lock timeout count parity error
4C	SMA BSIDE :SMA_STS :82A0001C (b10 - 17)							
	Reserved	Reserved	Reserved	Reserved	CACHE PK slot signal bit '01' : A side '10' : B side		SM disconnect status bit	SM power down status bit
4D	SMA BSIDE :SMA_STS :82A0001C (b20 - 27)							
	disconnect request bit	SM self-refresh status bit	SM voltage status bit	LSI voltage status bit	System timer enable status bit	SMA all lock status bit	SM ready status bit	SM LSI blockade status bit
4E	SMA BSIDE :SMA_STS :82A0001C (b30 - 37)							
	CACHE PK version bit				SMA LSI version bit			
4F								
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Copyright ©2000, Hitachi, Ltd.

Byte27 = 81 Byte40-7F (OTHER ERROR) (Byte29=x'07') (2/4)

	0	1	2	3	4	5	6	7
50	SMA BSIDE: PATH0_ERR_DET : 82A00104 (b00 - 07)							
	HSN recv command parity error	HSN recv address parity error	HSN recv write data parity error	Reserved	HSN recv sync0 under run error	HSN recv sync1under run error	HSN recv sync0 over run error	HSN recv sync1 over run error
51	SMA BSIDE: PATH0_ERR_DET : 82A00104 (b10 - 17)							
	Recv data LRC	LRC byte check inconsist	Command lock/unlock '0' or '1'	Command read/write bit '0' or '1'	Slave-dual lock access error	Double lock error	Lock access count over error	Reserved
52	SMA BSIDE: PATH0_ERR_DET : 82A00104 (b20 - 27)							
	Command bit parity generator error	Address bit parity generator error	Data bit parity generator error	Path command buffer parity error	Path address buffer parity error	Path write data buffer parity error	Path command lock/unlock bit ON	Path command read/write bit ON
53	SMA BSIDE: PATH0_ERR_DET : 82A00104 (b30 - 37)							
	Reserved	Reserved	lock under no lock request	common path self path compare error	Reserved	Path sequencer parity error	Request tineout count parity error	Lock timeout count parity error
54	SMA BSIDE: PATH1_ERR_DET : 82A00114 (b00 - 07)							
	HSN recv command parity error	HSN recv address parity error	HSN recv write data parity error	Reserved	HSN recv sync0 under run error	HSN recv sync1under run error	HSN recv sync0 over run error	HSN recv sync1 over run error
55	SMA BSIDE: PATH1_ERR_DET : 82A00114 (b10 - 17)							
	Recv data LRC	LRC byte check inconsist	Command lock/unlock '0' or '1'	Command read/write bit '0' or '1'	Slave-dual lock access error	Double lock error	Lock access count over error	Reserved
56	SMA BSIDE :PATH1_ERR_DET : 82A00114(b20 - 27)							
	Command bit parity generator error	Address bit parity generator error	Data bit parity generator error	Path command buffer parity error	Path address buffer parity error	Path write data buffer parity error	Path command lock/unlock bit ON	Path command read/write bit ON
57	SMA BSIDE :PATH1_ERR_DET : 82A00114(b30 - 37)							
	Reserved	Reserved	lock under no lock request	common path self path compare error	Reserved	Path sequencer parity error	Request tineout count parity error	Lock timeout count parity error
58	MPA:MPASTS 82000100 (b30 - 37)							
	MPA interrupt status bit	Master CHK3 status bit	Slave CHK3 status bit	Reserved	PROM_IF CHK1B status bit	COM_IF CHK1B status bit	XR_IF CHK1B status bit	MP interrupt status bit
59	MPA:BMD 82000024 (b30 - 37)							
	Reserved	SM copy mode enable	SM disable side A	SM disable side B	A0 path disable	A1 path disable	B0 path disable	B1 path disable
5A	MPA:X0AP 82000604 (b30 - 37)							
	Reserved	Reserved	X0LOCK exec face#0 XR log	X0WT exec face#0 XR log	X0AP exec face #0 XR address log byte parity bit			
5B	MPA:X1AP 82000614 (b34 - 37)							
	Reserved	Reserved	X1LOCK exec face#0 XR log	X1WT exec face#0 XR log	X1AP exec face #0 XR address log byte parity bit			
5C	MPA:X1A 82000610(b00 - 07) or MPA:LADR 82000044(b00 - 07)							
	X1A00	X1A01	X1A02	X1A03	X1A04	X1A05	X1A06	X1A07
	X1A = exec face #0 XR address log byte							
5D	MPA:X1A 82000610(b10 - 17) or MPA:LADR 82000044(b10 - 17)							
	X1A10	X1A11	X1A12	X1A13	X1A14	X1A15	X1A16	X1A17
	X1A = exec face #0 XR address log byte							
5E	MPA:X1A 82000610(b20 - 27) or MPA:LADR 82000044(b20 - 27)							
	X1A20	X1A21	X1A22	X1A23	X1A24	X1A25	X1A26	X1A27
	X1A = exec face #0 XR address log byte							
5F	MPA:X1A 82000610(b30 - 37) or MPA:LADR 82000044(b30 - 37)							
	X1A30	X1A31	X1A32	X1A33	X1A34	X1A35	X1A36	X1A37
	X1A = exec face #0 XR address log byte							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 81 Byte40-7F (OTHER ERROR) (Byte29=x'07') (3/4)

	0	1	2	3	4	5	6	7
60	MPA:X0A:82000600 (b00 - 07) or MPA:LNEW 82000044(b00 - 07)							
	X0A00	X0A01	X0A02	X0A03	X0A04	X0A05	X0A06	X0A07
	X0A = exec face #0 XR address log byte							
61	MPA:X0A:82000600 (b10 - 17) or MPA:LNEW 82000044(b10 - 17)							
	X0A10	X0A11	X0A12	X0A13	X0A14	X0A15	X0A16	X0A17
	X0A = exec face #0 XR address log byte							
62	MPA:X0A:82000600 (b20 - 27) or MPA:LNEW 82000044(b20 - 27)							
	X0A20	X0A21	X0A22	X0A23	X0A24	X0A25	X0A26	X0A27
	X0A = exec face #0 XR address log byte							
63	MPA:X0A:82000600 (b30 - 37) or MPA:LNEW 82000044(b30 - 37)							
	X0A30	X0A31	X0A32	X0A33	X0A34	X0A35	X0A36	X0A37
	X0A = exec face #0 XR address log byte							
64	MPA:RXA_RDT:82000620 (b00 - 07)							
	RXA_RD00	RXA_RD01	RXA_RD02	RXA_RD03	RXA_RD04	RXA_RD05	RXA_RD06	RXA_RD07
	SHSN_A recv-data log read data byte							
65	MPA:RXA_RDT:82000620 (b10 - 17)							
	RXA_RD10	RXA_RD11	RXA_RD12	RXA_RD13	RXA_RD14	RXA_RD15	RXA_RD16	RXA_RD17
	SHSN_A recv-data log read data byte							
66	MPA:RXA_RDT:82000620 (b20 - 27)							
	RXA_RD20	RXA_RD21	RXA_RD22	RXA_RD23	RXA_RD24	RXA_RD25	RXA_RD26	RXA_RD27
	SHSN_A recv-data log read data byte							
67	MPA:RXA_RDT:82000620 (b30 - 37)							
	RXA_RD30	RXA_RD31	RXA_RD32	RXA_RD33	RXA_RD34	RXA_RD35	RXA_RD36	RXA_RD37
	SHSN_A recv-data log read data byte							
68	MPA:RXA_EDT:82000624 (b00 - 07)							
	MP Status read INT	MP Status read STS flg	MP Status read Valid flg	MP Status read TOV	SCAN INT	SCAN read Data flg	SCAN STS flg	SCAN TOV
69	MPA:RXA_EDT:82000624 (b10 - 17)							
	All lock busy	Memory not Ready	Back up busy	All lock error	Memory disconnect busy	Illegal address error	DIMM Invalid error	Illegal lock error
6A	MPA:RXA_EDT:82000624 (b20 - 27)							
	Request timeout	PRB timeout	Lock wait timeout	Lock off timeout	PRB parity error	Check code error	Path any error	Path board error
6B	MPA:RXA_EDT:82000624 (b30 - 37)							
	Correctable error	Uncorrectable error	I/O register parity error	Reserved	Reserved	SM PS down error	Memory control signal error	Common board error
6C	MPA:A0_Path TM0ERR:8214j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6D	MPA:A1_Path TM0ERR:8215j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6E	MPA:B0_ path TM0ERR:8216j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6F	MPA:B1_Path TM0ERR:8217j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1

Copyright ©2000, Hitachi, Ltd.

Byte27 = 81 Byte40-7F (OTHER ERROR) (Byte29=x'07') (4/4)

	0	1	2	3	4	5	6	7
70	MPA: RXB_RDT :82000630 (b00 - 07)							
	RXB_RD00	RXB_RD01	RXB_RD02	RXB_RD03	RXB_RD04	RXB_RD05	RXB_RD06	RXB_RD07
	SHSN_B recv-data log read data byte							
71	MPA: RXB_RDT :82000630 (b10 - 17)							
	RXB_RD10	RXB_RD11	RXB_RD12	RXB_RD13	RXB_RD14	RXB_RD15	RXB_RD16	RXB_RD17
	SHSN_B recv-data log read data byte							
72	MPA: RXB_RDT :82000630 (b20 - 27)							
	RXB_RD20	RXB_RD21	RXB_RD22	RXB_RD23	RXB_RD24	RXB_RD25	RXB_RD26	RXB_RD27
	SHSN_B recv-data log read data byte							
73	MPA: RXB_RDT :82000630 (b30 - 37)							
	RXB_RD30	RXB_RD31	RXB_RD32	RXB_RD33	RXB_RD34	RXB_RD35	RXB_RD36	RXB_RD37
	SHSN_B recv-data log read data byte							
74	MPA:RXB_EDT:82000634 (b00 - 07)							
	MP Status read INT	MP Status read STS flg	MP Status read Valid flg	MP Status read TOV	SCAN INT	SCAN read Data flg	SCAN STS flg	SCAN TOV
75	MPA:RXB_EDT:82000634 (b10 - 17)							
	All lock busy	Memory not Ready	Back up busy	All lock error	Memory disconnect busy	Illegal address error	DIMM Invalid error	Illegal lock error
76	MPA:RXB_EDT:82000634 (b20 - 27)							
	Request timeout	PRB timeout	Lock wait timeout	Lock off timeout	PRB parity error	Check code error	Path any error	Path board error
77	MPA:RXB_EDT:82000634 (b30 - 37)							
	Correctable error	Uncorrectable error	I/O register parity error	Reserved	Reserved	SM PS down error	Memory control signal error	Common board error
78	MPA :ACSMODE :82000650 (b00 -07)							
	Reserved	Reserved	Reserved	XR access exec face #	Reserved	Reserved	Access path A side	Access path B side
79	MPA :ACSMODE :82000650 (b10 -17)							
	Access mode 1	Access mode 2	Access mode 3	Access mode 4	Access mode 5	Access mode 6	Access mode 7	Access mode 8
7A	MPA :ACSMODE :82000650 (b20 -27)							
	Access mode 9	Access mode 10	Reserved	Reserved	Accesspatarn SM read	Access patarn SM write	Access patarn SM read (atomic)	Access patarn SM write (atomic)
7B	MPA :ACSMODE :82000650 (b30 -37)							
	Access patarn resource lock	Access patarn IO read	Access patarn IO write	Access patarn BCAST read	Access patarn BCAST write	Access patarn SCAN read	Access patarn Scan write	Reserved
7C	MPA :ACSPATH :82000654 (b00 - 07)							
	1st access read access	1st access write access	1st access lock acquire access	1st access lock termination access	1st access use A0 path	1st access use A1 path	1st access use B0 path	1st access use B1 path
7D	MPA :ACSPATH :82000654 (b10 - 17)							
	2nd access read access	2nd access write access	2nd access lock acquire access	2nd access lock termination access	2nd access use A0 path	2nd access use A1 path	2nd access use B0 path	2nd access use B1 path
7E	MPA :ACSPATH :82000654 (b20 - 27)							
	3rd access read access	3rd access write access	3rd access lock acquire access	3rd access lock termination access	3rd access use A0 path	3rd access use A1 path	3rd access use B0 path	3rd access use B1 path
7F	MPA :ACSPATH :82000654 (b30 - 37)							
	4th access read access	4th access write access	4th access lock acquire access	4th access lock termination access	4th access use A0 path	4th access use A1 path	4th access use B0 path	4th access use B1 path

Copyright ©2000, Hitachi, Ltd.

Byte27 = 81 & Byte34 : bit4-7 = 3 (CHK3 Reset) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘8’)				Message (x‘1’)			
28	Related internal SSB log number							
29								
2A	Not used							
2B	Not used							
2C	Old PSW							
2D								
2E								
2F								
30	Internal SSB log number (RESET)							
31								
32	Related RESET detail log number							
33								
34	PCB number				Message code (x‘3’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF81’ : LDEV type = DKU87I/x‘EF81’ : LDEV type = DKU86I)*							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not usde (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Copyright ©2000, Hitachi, Ltd.

Byte27 = 81 & Byte34 : bit4-7 = 3 (CHK3 Reset) (2/2)

	0	1	2	3	4	5	6	7
40		Not used						
41		Not used						
42		Initialize interface information						
43								
44		Reset type code						
45								
46		1st reset type code						
47		Reset SSB type code						
48		Reset type code for making SSB						
49		Self CHK1A difference code						
4A		Multi reset type code						
4B								
4C		Interrupted address						
4D								
4E								
4F								
50		Interrupted opration code						
51								
52								
53								
54		Current LDEV number						
55								
56		Current LPN number						
57								
58		Initiation cause code						
59								
5A		Command interface						
5B		DSB (from LCT)						
5C		sys status						
5D		REQ ID (from LCT)						
5E		JCB ID (form LCT)						
5F								
60		wchklmpbitmap (from LCT)						
61								
62								
63								
64		jcb id						
65								
66		req id						
67		Job type code						
68		job status						
69		Executing processor number						
6A		Initiation cause code						
6B		Initiation detail code						
6C		Command code						
6D		Channel sequence						
6E		Reserved						
6F								
70		DCN						
77								
78		Not used						
79								
7A								
7B								
7C		SLV-DCN (slvdcnr)						
7D								
7E								
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = 88 & Byte34:b4-7=A & Byte28 = 01 (LCP Failure:CHK-2/ADP I/F Error) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘8’)				Message (x‘8’)			
28	LCP error message”(x‘01’:LCP CHK-2/ADP interface error)							
29	LCP error code							
2A								
2B	XR4B(H)							
	BBF OVERRUN	PND OVERRUN	0	0	0	0	0	0
2C	XR4B(L)							
	LRCA ERR	LRCB ERR	BBFP PER	BBIP PER	BBOP PER	PND CK2	CNT PER	REQ CNT OVERRUN
2D	XR3E(H)							
	RBFA APER	RBFB APER	RBFC APER	RBF WRDER	MBFA APER	MBFB APER	MBFC APER	MBF WRDER
2E	XR3E(L)							
	FRM RCTPE	CMP DPER	XFR CHRPER	XFR SEQPER	M-CNT PER	H-CNT PER	0	0
2F	XR55(H)							
	BUSPE PA	LRCER PA	REQ ER A	ADTDT ER A	0	0	0	0
30	XR55(L)							
	BUSPE PB	LRCER PB	REQ ER B	ADTDT ER B	0	0	0	0
31								
	Control flag	0	0	STOP (XR49:bit15)	CK2 DTX (XR4A:bit0)	CK2 LIN (XR4A:bit1)	IFERA (XR51:bit12)	IFERB (XR51:bit13)

Copyright ©2000, Hitachi, Ltd.

Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 01 (LCP Failure:CHK-2/ADP I/F Error) (2/2)

	0	1	2	3	4	5	6	7
32		Module ID						
33		Routine ID						
34		PCB number			Message code (x‘A’)			
35		SSID (Low) of self subsystem						
36		Symptom code (x‘FF88’ : LDEV type = DKU87I/x‘EF88’ : LDEV type = DKU86I)						
37								
38		Log and message control (x‘00’)						
39		Program action code (x‘00’)						
3A		Configuration information						
3B								
3C		Not used						
3D		Cylinder address						
3E								
3F		Head address						
40		LCP error message (x‘01’)						
41		Key code (x‘04’)						
42		LCP error code						
43								
44		x‘00’						
45		Command code						
46		x‘00’						
47		x‘00’						
48		XR4B						
49								
4A		XR3E						
4B								
4C		XR55						
4D								
4E		Control flag						
4F		x‘00’						
50		Not used						
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 02 (LCP Failure:Link Receive Error) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘8’)				Message (x‘8’)			
28	LCP error message”(x‘02’:Link receive error)							
29	LCP error code							
2A								
2B	XR36(H)							
	L-SIG ERR0	L-SIG ERR1	CONN ERR0	CONN ERR1	CONN ERR2	0	0	0
2C	XR37(H)							
	CONN ERR3	L-SIG ERR	CODE VIOLA	SEQ ERR	CRC ERR	ABORT ERR	PROT ERR0	PROT ERR1
2D	XR37(L)							
	PROT ERR2	PROT ERR3	PROT ERR4	PROT ERR5	PROT ERR6	PROT ERR7	PROT ERR8	PROT ERR9
2E	XR33(H)							
	C-SOF ERR	P-SOF ERR	D-EOF ERR	P-EOF ERR	L-SIG ERR	CODE VIOLA	SEQ ERR	CRC ERR
2F	XR33(L)							
	0	0	0	R-CNT 0	R-CNT 1	R-CNT 2	R-CNT 3	R-CNT 4
30								
	0	0	STOP (XR49:bit15)	ABORT (XR32:bit11)	ER RCV1 (XR4A:bit3)	ER RCV2 (XR4A:bit4)	ER RCV3 (XR4A:bit5)	OTHER (XR51:bit6)
31	XR2A(L)							
	Field Information							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 02 (LCP Failure:Link Receive Error) (2/2)

	0	1	2	3	4	5	6	7
32		Module ID						
33		Routine ID						
34		PCB number			Message code (x‘A’)			
35		SSID (Low) of self subsystem						
36		Symptom code (x‘FF88’ : LDEV type = DKU87I/x‘EF88’ : LDEV type = DKU86I)						
37								
38		Log and message control (x‘00’)						
39		Program action code (x‘00’)						
3A		Configuration information						
3B								
3C		Not used (x‘00’)						
3D		Cylinder address						
3E								
3F		Head address						
40		LCP error message (x‘02’)						
41		Key code (x‘04’)						
42		LCP error code						
43								
44		x‘00’						
45		Command code						
46		x‘00’						
47		x‘00’						
48		XR36						
49								
4A		XR37						
4B								
4C		XR33						
4D								
4E		Control flag						
4F		x‘00’						
50		Not used						
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 0C (LCP Failure:Long Write Data) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘8’)				Message (x‘8’)			
28	LCP error message (x‘0C’:Long Write Data)							
29	LCP error code							
2A								
2B	Request count							
2C								
2D	Received data count							
2E								
2F	Not used (x‘00’)							
30	Not used (x‘00’)							
31	Not used (x‘00’)							
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘A’)			
35	SSID (low) of self subsystem							
36	Symptom Code (x‘FF88’ : LDEV type = DKU87I/x‘EF88’ : LDEV type = DKU86I)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 0C (LCP Failure:Long Write Data) (2/2)

	0	1	2	3	4	5	6	7
40		LCP error message (x‘0C’)						
41		Key code (x‘04’)						
42		LCP error code						
43								
44		x‘00’						
45		Command code						
46		x‘00’						
47		x‘00’						
48		Requested count						
49								
4A		Received data count						
4B								
4C		x‘00’						
4D		x‘00’						
4E		x‘00’						
4F		x‘00’						
50		Not used						
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 0E (LCP Failure:Timeout) (1/2)

	0	1	2	3	4	5	6	7
00		Time stamp						
05								
06		Format Message						
07	PCB type		Processor ID (Note)					
08		System error code						
09								
0A		JCB ID						
0B								
0C		REQ ID						
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10		LDEV number						
11								
12		CDEV#						
13		RDEV#						
12		CDEV number				RDEV number		
13	0	RCU SIM	0	0		RCV number		
14		RCU LDEV number						
15								
16		SSB log number						
17								
18		Related failure log number						
19								
1A		Related SIM log number						
1B								
1C		Related SSB log number						
1D								
1E		(Reserved)						
1F		SCB						
20		Basic SSB						
21								
22								
23		Count						
24		Device address						
25		Cylinder address (low)						
26		Cylinder address (high)				Head address		
27		Format (x‘8’)				Message (x‘8’)		
28		LCP error message (x‘0E’:Timeout)						
29		LCP error code						
2A								
2B		Reason code (Note 1)						
2C								
2D		XR49 (H)						
	ESYCN	END	RDYOK	RDYRCV	0	CMDFRM	ACPRSP	DATAXF
2E		XR49 (L)						
	XFREND	DEVEND	CNTFLG	EOF	CMPEQ	CMPGT	0	STOP
2F		XR51 (H)						
	CAL PA	CAL PB	RDY	P BSY	CALL	SELTD	CHK1	DCK1
30		XR51 (L)						
	BFBSY	ATTN	0	0	IFERA	IFERB	PA BSY	PB BSY
31		XR48 (H)						
	RUN BSY	RUN TRS	RUN ADP	DAT REQ MOD	XFSTOOP	CDFLG	CMPA	CMPB
32		Module ID						
33		Routine ID						
34		PCB number				Message code (x‘A’)		
35		SSID (low) of self subsystem						
36		Symptom code (x‘FF88’ : LDEV type = DKU87I/x‘EF88’ : LDEV type = DKU86I)						
37								

Copyright ©2000, Hitachi, Ltd.

Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 0E (LCP Failure:Timeout) (2/2)

	0	1	2	3	4	5	6	7
38		Log and message control (x‘00’)						
39		Program action code (x‘00’)						
3A		Configuration information						
3B								
3C		Not used (x‘00’)						
3D		Cylinder address						
3E								
3F		Head address						
40		LCP error message (x‘0E’)						
41		Key code (x‘04’)						
42		LCP error code						
43								
44		x‘00’						
45		Command code						
46		x‘00’						
47		x‘00’						
48		Reason code						
49								
4A		XR49(H)						
	ESYCN	END	RDYOK	RDYRCV	0	CMDFRM	ACPRSP	DATAXF
4B		XR49(L)						
	XFREND	DEVEND	CNTFLG	EOF	CMPEQ	CMPGT	0	STOP
4C		XR51(H)						
	CAL PA	CAL PB	RDY	P BSY	CALL	SELTD	CHK1	DCK1
4D		XR51(L)						
	BFBSY	ATTN	0	0	IFERA	IFERB	PA BSY	PB BSY
4E		XR48(H)						
	RUN BSY	RUN TRS	RUN ADP	DAT REQ MOD	XFSTOP	CDFLG	CMPA	CMPB
4F		XR48(L)						
	DATA XF	RD / WR (0) (1)	1st CCW	RD/WR XFR	MEFLG	BBF SWEEP	BBIP INC	BBIP INC
50		Not used						
7F								

(Note 1) Reason code

x‘FF01’ : (Read) Timeout at wating for ACP CMD RSP
x‘FF02’ : (Read) Timeout at wating for frame header
x‘FF03’ : (Read) Timeout at wating for data frame
x‘FF04’ : (Read) Timeout at wating for end of data transfer
x‘FF05’ : (Read) Timeout at wating for data frame
x‘FF06’ : (Read) Timeout at wating for end of data transfer
x‘FF07’ : (Read) Timeout at wating for command frame
x‘FF08’ : (Read) Timeout at wating for DATA REQ
x‘FF09’ : (Read) Timeout at wating for status
x‘FFF1’ : (Write) Timeout at wating for ACP CMD RSP
x‘FFF2’ : (Write) Timeout at wating for first data
x‘FFF3’ : (Write) Timeout at wating for frame header
x‘FFF4’ : (Write) Timeout at wating for frame header
x‘FFF5’ : (Write) Timeout at wating for frame header
x‘FFF6’ : (Write) Timeout at wating for command frame
x‘FFF7’ : (Write) Timeout at wating for frame header
x‘FFF8’ : (Write) Timeout at wating for end of data transfer
x‘FFF9’ : (Write) Timeout at wating for status

Copyright ©2000, Hitachi, Ltd.

Byte27 = 88 & Byte34:b4-7 = A & Byte28 ≠ 01/02/0C/0E (LCP Failure:Others) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘8’)				Message (x‘8’)			
28	LCP error message (Note 1)							
29	LCP error code							
2A								
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							
31	Not used (x‘00’)							
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘A’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF88’ : LDEV type = DKU87I/x‘EF88’ : LDEV type = DKU86I)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 88 & Byte34:b4-7 = A & Byte28 ≠ 01/02/0C/0E (LCP Failure:Others) (2/2)

	0	1	2	3	4	5	6	7
40	LCP error message (Note 1)							
41	Key code (x‘04’)							
42	LCP error code							
43								
44	x‘00’							
45	Command code							
46	x‘00’							
47	x‘00’							
48	x‘00’							
49	x‘00’							
4A	x‘00’							
4B	x‘00’							
4C	x‘00’							
4D	x‘00’							
4E	x‘00’							
4F	x‘00’							
50	Not used							
7F								

(Note 1) LCP error message

x‘00’ : No message
x‘08’ : Transmission error
x‘09’ : Protocol error
x‘0D’ : Retry abort

Copyright ©2000, Hitachi, Ltd.

Byte27 = 88 & Byte34:b4-7 = B & Byte28 = 01 (MCP Failure:CHK2/ADP I/F ERR/B0 P-ERR) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘8’)				Message (x‘8’)			
28	MCP error message (x‘01’:LCP CHK2 / ADP I/F error / Bus out parity ERR)							
29	MCP error code							
2A								
2B	XRBS(H)							
	Data transfer end	CHK2 error	ADP interface error	Channel bus out parity ER	Channel overrun	Truncation	Halt I/O	Data XFR force end
2C	XRBS(L)							
	Data XFR abnormal end	Channel data XFR end	MP data XFR end	0	0	0	0	0
2D	XRCK20(H)							
	EDCC/DCC mode unmatch	Duplicate CU ADR in DCC	CHL BIN0 parity ER:data XFR	CHL BIN1 parity ER:data XFR	MBF ¨ADP MBF ADR parity ER	ADP ¨MBF MBF ADR parity ER	ADP ¨MBF MBF data parity ER	(RSV)
2E	XRCK20(L)							
	SPC counter parity ER	CHC counter parity ER	PND counter parity ER	PND counter overrun	BBF out CBID in LRC ERR	CHL BUS IN 0 parity ER	CHL BUS IN 1 parity ER	0
2F	XRCK21(H)							
	BBF input data LRC ERR	BBF input section LRC ERR	BBF input-output LRC ERR	BBIP parity error	BBOP parity error	TAG OUT parity error	CBOB out data parity ER	CBOB in-BBF in parity ER
30	XRCK21(L)							
	TAG IN FLG MEM parity ER	FLG MEM INP PTR parity ER	FLG MEM OUT PTR parity ER	TAG OUT sequence error	TAG OUT signal narrow	TAG OUT signal duplicate	0	0

Copyright ©2000, Hitachi, Ltd.

Byte27 = 88 & Byte34:b4-7 = B & Byte28 = 01 (MCP Failure:CHK2/ADP I/F ERR/B0 P-ERR) (2/3)

	0	1	2	3	4	5	6	7
31	XRIFER							
	LCM-ADPA bus parity ER	LCM-ADPA bus LRC error	ADP I/F sequencer parity ER	ADP0 error	LCM-ADPB bus parity ER	LCM-ADPB bus LRC error	ADP I/F sequencer parity ER	ADP1 error
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x'B')			
35	SSID (low) of self subsystem							
36	Symptom code (x'FF88' : LDEV type = DKU87I/x'EF88' : LDEV type = DKU86I)							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not used (x'00')							
3D	Cylinder address							
3E								
3F	Head address							
40	MCP message code (x'01)							
41	Key code (x'04')							
42	MCP error code							
43								
44	x'00'							
45	Command code							
46	x'00'							
47	x'00'							
48	XRBS (H)							
	Data transfer end	CHK2 error	ADP interface error	Channel bus out parity ER	Channel overrun	Truncation	Halt I/O	Data XFR force end
49	XRBS (L)							
	Data XFR abnormal end	Channel data XFR end	MP data XFR end	0	0	0	0	0
4A	XRCK20 (H)							
	EDCC/DCC mode unmatch	Duplicate CU ADR in DCC	CHL BIN0 parity ER:data XFR	CHL BIN1 parity ER:data XFR	MBF→ADP MBF ADR parity ER	ADP→MBF MBF ADR parity ER	ADP→MBF MBF data parity ER	(RSV)
4B	XRCK20 (L)							
	SPC counter parity ER	CHC counter parity ER	PND counter parity ER	PND counter overrun	BBF out CBID in LRC ERR	CHL BUS IN 0 parity ER	CHL BUS IN 1 parity ER	0
4C	XRCK21 (H)							
	BBF input data LRC ERR	BBF input section LRC ERR	BBF input-output LRC ERR	BBIP parity error	BBOP parity error	TAG OUT parity error	CBOB out data parity ER	CBOB in-BBF in parity ER
4D	XRCK21 (L)							
	TAG IN FLG MEM parity ER	FLG MEM INP PTR parity ER	FLG MEM OUT PTR parity ER	TAG OUT sequence error	TAG OUT signal narrow	TAG OUT signal duplicate	0	0
4E	XRIFER							
	LCM-ADPA bus parity ER	LCM-ADPA bus LRC error	ADP I/F sequencer parity ER	ADP0 error	LCM-ADPB bus parity ER	LCM-ADPB bus LRC error	ADP I/F sequencer parity ER	ADP1 error
4F	XRBC0							
	Channel enable	Channel execute	Increment mode	Channel XFR mode 10:Read 11:Write		ADP I/F execute	Chain data flag	LRC enable

Copyright ©2000, Hitachi, Ltd.

Byte27 = 88 & Byte34:b4-7 = B & Byte28 = 01(MCP Failure:CHK2/ADP I/F ERR/B0 P-ERR) (3/3)

	0	1	2	3	4	5	6	7
50	XRCHC(H)							
	Channel data transfer count							
51	XRCHC(L)							
	Channel data transfer count							
52	XRBBIP(H)							
	BBF data input address							
53	XRBBIP(L)							
	BBF data input address							
54	XRBBOP(H)							
	BBF data output address							
55	XRBBOP(L)							
	BBF data output address							
56	XRPNDR(H)							
	Burst Buffet Output Pointer							
57	XRPNDR(L)							
	Pend Counter							
58	XRBC1(H)							
	Force channel overrun	Force data XFR stop	Suppress data valid	BBF dummy DT output	(RSV)	(RSV)	(RSV)	(RSV)
59	XRBC1(L)							
	Request suppress data	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5A	XRCC0(H)							
	DCC mode	EDCC mode	(RSV)	(RSV)	(RSV)	CHL XFR rate	010 : 4.5MB/S 000 : 3.0MB/S 100 : 6.0MB/S 001 : 4.2MB/S 110 : 9.0MB/S	
5B	XRCC0(L)							
	XRCA0,1, XRCC0 INIT end	(RSV)	(RSV)	HALT I/O→CU Busy valid	DISCON valid	SEL RST valid	SYS RST valid (OPL OUT)	SYS RST valid (SUP OUT)
5C	x‘00’							
5D	x‘00’							
5E	x‘00’							
5F	x‘00’							
60	Module ID detected error							
61	Routine ID detected error							
62	Not used							
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = 88 & Byte34:b4-7 = B & Byte28 = 0E (MCP Failure:Timeout) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘8’)				Message (x‘8’)			
28	MCP error message (x‘0E’:Timeout)							
29	LCP error code							
2A								
2B	Reason code							
2C								
2D	XRBS(H)							
	Data transfer end	CHK2 error	ADP interface error	Channel bus out parity ER	Channel overrun	Truncation	Halt I/O	Data XFR force end
2E	XRBS(L)							
	Data XFR abnormal end	Channel data XFR end	MP data XFR end	0	0	0	0	0
2F	XRASTS(H)							
	Path 0 ADP data XFR request	Path 1 ADP data XFR request	ADP path interface ready	ADP path busy	ADP path CALL M	ADP path SEL	ADP path CHK1	ADP path W-CHK1
30	XRASYS(L)							
	Receive buffer busy	Data FRM with attention	(RSV)	(RSV)	Path 0 ADP interface error	Path 1 ADP interface error	CHP 0 path busy	CHP 1 path busy
31	XRBC0(H)							
	Enable channel	Execute channel	(RSV)	Increment mode	Channel XFR mode 10:READ 11:WRITE		(RSV)	(RSV)

Copyright ©2000, Hitachi, Ltd.

Byte27 = 88 & Byte34:b4-7 = B & Byte28 = 0E (MCP Failure:Timeout) (2/3)

	0	1	2	3	4	5	6	7
32		Module ID						
33		Routine ID						
34		PCB number			Message code (x‘B’)			
35		SSID (low) of self subsystem						
36		Symptom code (x‘FF88’ : LDEV type = DKU87I/x‘EF88’ : LDEV type = DKU86I)						
37								
38		Log and message control (x‘00’)						
39		Program action code (x‘00’)						
3A		Configuration information						
3B								
3C		Not used (x‘00’)						
3D		Cylinder address						
3E								
3F		Head address						
40		MCP message code (x‘0E)						
41		Key code (x‘04’)						
42		MCP error code						
43								
44		x‘00’						
45		Command code						
46		x‘00’						
47		x‘00’						
48		Reason code						
49								
4A		XRBS (H)						
	Data transfer end	CHK2 error	ADP interface error	Channel bus out parity ER	Channel overrun	Truncation	Halt I/O	Data XFR force end
4B		XRBS (L)						
	Data XFR abnormal end	Channel data XFR end	MP data XFR end	0	0	0	0	0
4C		XRASTS (H)						
	Path 0 ADP data XFR request	Path 1 ADP data XFR request	ADP path interface ready	ADP path busy	ADP parh CALL M	ADP path SEL	ADP parh CHK1	ADP path W-CHK1
4D		XRASTS (L)						
	Receive buffer busy	Data FRM with attention	(RSV)	(RSV)	Path 0 ADP interface error	Path 1 ADP interface error	CHP 0 path busy	CHP 1 path busy
4E		XRBC0 (H)						
	Enable channel	Execute channel	(RSV)	Increment mode	Channel XFR mode 10:READ 11:WRITE		(RSV)	(RSV)
4F		XRBC0 (L)						
	ADP I/F data XFR execute	Chain data flag	LRC enable	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
50		XRCHC (H)						
		Channel data transfer count						
51		XRCHC (L)						
		Channel data transfer count						
52		XRBBIP (H)						
		BBF data input address						
53		XRBBIP (L)						
		BBF data input address						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 88 & Byte34:b4-7 = B & Byte28 = 0E (MCP Failure:Timeout) (3/3)

	0	1	2	3	4	5	6	7
54	XRBBOP(H)							
	BBF data output address							
55	XRBBOP(L)							
	BBF data output address							
56	XRPNDR(H)							
	Burst Buffet Output Pointer							
57	XRPNDR(L)							
	Pend Counter							
58	XRBC1(H)							
	Force channel overrun	Force data XFR stop	Suppress data valid	BBF dummy DT output	(RSV)	(RSV)	(RSV)	(RSV)
59	XRBC1(L)							
	Suppress data request	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5A	XRCC0(H)							
	DCC mode	EDCC mode	(RSV)	(RSV)	(RSV)	CHL XFR rate	010 : 4.5MB/S 000 : 3.0MB/S 100 : 6.0MB/S 001 : 4.2MB/S 110 : 9.0MB/S	
5B	XRCC0(L)							
	XRCA0,1, XRCC0 INIT end	(RSV)	(RSV)	HALT I/O→CU Busy valid	DISCON valid	SEL RST valid	SYS RST valid (OPL OUT)	SYS RST valid (SUP OUT)
5C	x‘00’							
5D	x‘00’							
5E	x‘00’							
5F	x‘00’							
60	Module ID detected error							
61	Routine ID detected error							
62	Not used							
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = 88 & Byte34:b4-7 = B & Byte28 = 80 (MCP Failure :Burst Failed) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘8’)				Message (x‘8’)			
28	MCP error message (x‘80’:Burst failed)							
29	MCP error code							
2A								
2B	x‘00’							
2C	x‘00’							
2D	x‘00’							
2E	x‘00’							
2F	x‘00’							
30	x‘00’							
31	x‘00’							
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘B’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF88’ : LDEV type = DKU87I/x‘EF88’ : LDEV type = DKU86I)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 88 & Byte34:b4-7 = B & Byte28 = 80 (MCP Failure:Burst Failed) (2/3)

	0	1	2	3	4	5	6	7
40		MCP message code (x‘80’)						
41		Key code (x‘04’)						
42		MCP error code						
43								
44		Not used						
4F								
50		XRCHC(H)						
		Channel data transfer count						
51		XRCHC(L)						
		Channel data transfer count						
52		XRBBIP(H)						
		BBF data input address						
53		XRBBIP(L)						
		BBF data input address						
54		XRBBOP(H)						
		BBF data output address						
55		XRBBOP(L)						
		BBF data output address						
56		XRPNDR(H)						
		Burst buffer output pointer						
57		XRPNDR(L)						
		Pend Counter						
58		XRBC1(H)						
	Force channel overrun	Force data XFR stop	Suppress data valid	BBF dummy DT output	(RSV)	(RSV)	(RSV)	(RSV)
59		XRBC1(L)						
	Suppress data request	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5A		XRCC0(H)						
	DCC mode	EDCC mode	(RSV)	(RSV)	(RSV)	CHL XFR rate 010:4.5MB/S 000:3.0MB/S 100:6.0MB/S 001:4.2MB/S 110:9.0MB/S		
5B		XRCC0(L)						
	XRCA0,1, XRCC0 INIT end	(RSV)	(RSV)	HALT I/O →CU Busy valid	DISCON valid	SEL RST valid	SYS RST valid (OPL OUT)	SYS RST valid (SUP OUT)

Copyright ©2000, Hitachi, Ltd.

Byte27 = 88 & Byte34:b4-7 = B & Byte28 = 80 (MCP Failure :Burst failed) (3/3)

	0	1	2	3	4	5	6	7
5C		Not used						
5D								
5E								
5F								
60		Module ID detected error						
61		Routine ID detected error						
62		Not used						
63								
64								
65								
66								
67								
68								
69								
6A								
6B								
6C								
6D								
6E								
6F								
70								
71								
72								
73								
74								
75								
76								
77								
78								
79								
7A								
7B								
7C								
7D								
7E								
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = 89 & Byte0D Bit2 = 0 (ESCON, FICON CHA CHK2)

	0	1	2	3	4	5	6	7
00	Time Stamp							
|								
05								
06	Format Message							
07	P/K Type		Processer ID					
08	System Error Code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	HOST Report	SVP Report	Force Log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	PORT#		RCU#			
10	LDEV#							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV#							
15								
16	Internal SSB Log Number							
17								
18	Related Failure Log Number							
19								
1A	Related SIM Log Number							
1B								
1C	Related SSB Log Number							
1D								
1E	(Reserved)							
1F	SCB							
20	BasicSSB							
21								
22								
23	Count							
24	Device Address							
25	Cylinder Address (Low)							
26	Cylinder Address (High)				Head Address			
27	Format (x‘8’)				Message (x‘9’)			
28	SubCode							
29	Detail Information (See Following Pages.)							
|								
31								
32	Module ID							
33	Routine ID							
34	P/K ID				Message Code (x‘0’)			
35	SSID for Self Subsystem							
36	Symptom Code (x‘FF89’:LDEV Type=DKU87I / x‘EF89’: LDEV Type=DKU86I)							
37								
38	Log and Message Control (x‘00’)							
39	Program Action Control (x‘00’)							
3A	Configuration Information							
3B								
3C	Not Used							
3D	Cylinder Address							
3E								
3F	Head Address							
40	Detail Information (See Following Pages.)							
|								
7F								

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 89 & Byte0D Bit2 ≠ 0 (FIBRE CHA CHK2)

	0	1	2	3	4	5	6	7
00	Time Stamp							
|								
05								
06	Format Message							
07	P/K Type		Processer ID					
08	System Error Code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	HOST Report	SVP Report	Force Log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	PORT#		RCU#			
10	LDEV#							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV#							
15								
16	Internal SSB Log Number							
17								
18	Related Failure Log Number							
19								
1A	Related SIM Log Number							
1B								
1C	Related SSB Log Number							
1D								
1E	(Reserved)							
1F	SCB							
20	Inf valid	Err Code						
21	Segment Number							
22	Filemark	ECM	ILI	Reserved	Sense Key			
23	Information bytes							
24								
25								
26								
27	Format (x‘8’)				Message (x‘9’)			
28	SubCode							
29	Detail Information (See Following Pages.)							
|								
31								
32	Reserved							
33								
34	Module ID1							
35	Routine ID1							
36	Module ID2							
37	Routine ID2							
38	Master Path Number							
39	SCSI Initiator ID							
3A	SCSI Target ID							
3B	Logical Unit Number							
3C	SCSI Command Code							
3D	Processor Number							
3E	LDEV#							
33								
40	Detail Information (See Following Pages.)							
|								
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte28-31 Detail
(1) Byte28 = 00, 1F

	0	1	2	3	4	5	6	7
28	SubCode (x'00' : ESCON I/F CHA - XFR CHK2) (x'1F' : ESCON I/F CHA - XFR TIME OUT)							
29	CHA::XFS0							
	TRANSFER END	(RSV)	(RSV)	PFC STATUS	CHK2	CHK2A	CHK2B	CHK2C
2A	CHA::XFS0							
	CHK2D	TRUNCA-TION	HALT I/O	SEARCH DASD= CPU	SEARCH DASD> CPU	SEARCH DASD< CPU	(RSV)	ABORT
2B	CHA::XFS1							
	(RSV)	(RSV)	(RSV)	(RSV)	MICRO ABORT	HARD ABORT	Force CHK1	Force CHK2
2C	CHA::XFS1							
	NEXT SEG ADR REG STATUS	(RSV)	(RSV)	(RSV)	(RSV)	NEXT SEG ADR WAIT	PFC ZERO	(RSV)
2D	CHA::PDC							
	(RSV)	(RSV)	(RSV)	ENLPLTB 0:NORMAL 1:LIST XFR	(RSV)	(RSV)	(RSV)	(RSV)
2E	CHA::XFC0							
	ENBL XFR	EXEC XFR	(RSV)	(RSV)	(RSV)	CBP PNT INC STOP	CACHE I/O MODE	SSD MODE
2F	CHA::XFC0							
	Data Tarnsfer Path: 0:ESCON=>CACHE 2:ESCON=>CBUF 3:CBUF=>ESCON 4:CACHE=>ESCON 6:CACHE=>CBUF 7:CBUF=>ESCON 8:CACHE SEARCH 9:CBUF SEARCH B:CACHE COPY				U-MODE (504B SB FORMAT)	(RSV)	(RSV)	WR FBA MODE
30	CHA::XFC1							
	(RSV)	ABORT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
31	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte28-31 Detail
(2) Byte28 = 01

	0	1	2	3	4	5	6	7
28	SubCode (x‘01’ : ESCON I/F CHA - Abnormal Cache Slot Status 1, (Note 1))							
29	Slot Status							
2A								
2B								
2C								
2D	WRITE in Progress	Make GAP	Execute ERASE	Update HA/R0	Update BM	(RSV)		
2E	SubBlock Number for Ready Response to Transfer							
2F	Start SubBlock Number for Incompletet Recode							
30	End SubBlock Number for Incompletet Recode							
31	Reserved							

(Note 1)Expect for cache ECC/LRC error has been detected in read side.
(Note2) (1) Module ID = 55 : After synchronous destage, cache slot with dirty attribute has been detected.
(2) Module ID ≠ 55 : In internal search or orientation process, incomplete subblock has been detected.

Copyright ©2000, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte28-31 Detail
(3) Byte28 = 02

	0	1	2	3	4	5	6	7
28	SubCode (x‘02’ : ESCON I/F CHA - Abnormal Cache Slot Status 2, (Note 1))							
29	Slot Status							
2A								
2B								
2C								
2D	WRITE in Progress	Make GAP	Execute ERASE	Update HA/R0	Update BM	(RSV)		
2E	SubBlock Number for Ready Response to Transfer							
2F	Start SubBlock Number for Processing Recode							
30	End SubBlock Number for Processing Recode							
31	Reserved							

(Note 1) Cache ECC/LRC error has been detected in read side.

Copyright ©2000, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte28-31 Detail
(4) Byte28 = 20, 3F

	0	1	2	3	4	5	6	7
28	SubCode (x'20' : FICON I/F CHA - XFR CHK2) (x'3F' : FICON I/F CHA - XFR TIME OUT)							
29	CHA::XFS0							
	TRANSFER END	(RSV)	(RSV)	PFC STATUS	CHK2	CHK2A	CHK2B	CHK2C
2A	CHA::XFS0							
	CHK2D	TRUNCA-TION	HALT I/O	SEARCH DASD= CPU	SEARCH DASD> CPU	SEARCH DASD< CPU	(RSV)	ABORT
2B	CHA::XFS1							
	(RSV)	(RSV)	(RSV)	(RSV)	MICRO ABORT	HARD ABORT	Force CHK1	Force CHK2
2C	CHA::XFS1							
	NEXT SEG ADR REG STATUS	(RSV)	(RSV)	(RSV)	(RSV)	NEXT SEG ADR WAIT	PFC ZERO	(RSV)
2D	CHA::PDC							
	(RSV)	DXBF XFR RUN	DXBF XFR 0:DXBF→CM 1:CM→DXBF	DXBF XFR WT ASYNC	DXBF XFR CNP	DXBF XFR CHAIN DATA	DXBF XFR COF	DXBF XFR MSW
2E	CHA::XFC0							
	ENBL XFR	EXEC XFR	(RSV)	(RSV)	(RSV)	CBP PNT INC STOP	CACHE I/O MODE	SSD MODE
2F	CHA::XFC0							
	Data Transfer Path: 0:ESCON=>CACHE 2:ESCON=>CBUF 3:CBUF=>ESCON 4:CACHE=>ESCON 6:CACHE=>CBUF 7:CBUF=>ESCON 8:CACHE SEARCH 9:CBUF SEARCH B:CACHE COPY				U-MODE (504B SB FORMAT)	(RSV)	(RSV)	WR FBA MODE
30	CHA::XFC1							
	(RSV)	ABORT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
31	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte28-31 Detail
(5) Byte28 = 28, 2F

	0	1	2	3	4	5	6	7
28	SubCode (x‘28’ : FICON I/F CHA - XFR CHK2) (x‘2F’ : FICON I/F CHA - XFR TIME OUT)							
29	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
2A	CMF::PXSTS							
	PBEND	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
2B	CMF::PXSTS							
	(RSV)	(RSV)	(RSV)	(RSV)	MICRO ABORT	HARD ABORT	Force CHK1	Force CHK2
2C	CMF::PBCTL							
	(RSV)	PRMBF RUN	PRMBF 0: READ 1: WRITE	(RSV)	PBP STOP	(RSV)	(RSV)	(RSV)
2D	CMF::PBCTL							
	PRMBF Address Pointer							
2E	CMF::PBCTL							
	PRMBF PCNT (High)							
2F	CMF::PBCTL							
	PRMBF PCNT (Low)							
30	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
31	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

Copyright ©2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte28-31 Detail
(6) Byte28 = 80, 81, 82, 83, 84, 85, 86, 87

	0	1	2	3	4	5	6	7
28	SubCode (x‘80’ - x‘87’ : FIBRE I/F CHA – DMA CHK2 (Note 1))							
29	FDTA::PnXFS							
	TRANSFER END	(RSV)	(RSV)	(RSV)	DMA CHK2B	DMA CHK2B	(RSV)	MP STOP0
2A	FDTA::PnXFS							
	MP STOP1	PCI CHK2A	PCI CHK2B0	PCI CHK2B1	PCI CHK2B2	PCI OVER RUN	(RSV)	HSN CHK2
2B	FDTA::PnXFS							
	(RSV)	P0 CHK2A	P0 CHK2B	P0 CHK2C	(RSV)	P0 CHK2A	P0 CHK2B	P0 CHK2C
2C	FDTA::PnXFS							
	(RSV)	(RSV)	(RSV)	COMMON CHK2C	(RSV)	(RSV)	(RSV)	ABORT
2D	FDTA::PnXFC							
	XFR BIT ‘00’:XFR Initialize ‘10’:XFR ABORT ‘11’:XFR START		(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	INT SEL 0:CHP SEL 1:FOP SEL
2E	FDTA::PnXFC							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	XFR SEL ‘000’:PCI DEVICE XFR ‘011’:16B - 128B CACHE ACCESS		
2F	FDTA::PnXFC							
	(RSV)	(RSV)	DATA FORMAT ‘00’:528B FORMAT ‘10’:16B-128B FORMAT		(RSV)	16 XFR CNT ‘000’:16B ACCESS ‘011’:64B ACCESS		
30	FDTA::PnXFC							
	(RSV)	(RSV)	XBF CHAIN (Transfer Chain Number :1 - 32)					
31	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

(Note 1) SubCode Bit 5: CHSN CHK2 detected
SubCode Bit 6: DMA CHK2 detected
SubCode Bit 7: PCI CHK2 detected

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte28-31 Detail
(7) Byte28 = 90, 91, 92, 93, 94, 95, 96, 97

	0	1	2	3	4	5	6	7
28	SubCode (x‘90’ - x‘97’ : FIBRE I/F CHA – PMA CHK2 (Note 1))							
29	FDTA::PnXFS							
	TRANSFER END	(RSV)	(RSV)	(RSV)	PMA CHK2B	PMA CHK2B	(RSV)	MP STOP0
2A	FDTA::PnXFS							
	MP STOP1	PCI CHK2A	PCI CHK2B0	PCI CHK2B1	PCI CHK2B2	PCI OVER RUN	(RSV)	HSN CHK2
2B	FDTA::PnXFS							
	(RSV)	P0 CHK2A	P0 CHK2B	P0 CHK2C	(RSV)	P0 CHK2A	P0 CHK2B	P0 CHK2C
2C	FDTA::PnXFS							
	(RSV)	(RSV)	(RSV)	COMMON CHK2C	(RSV)	(RSV)	(RSV)	ABORT
2D	FDTA::PnXFC							
	XFR BIT ‘00’:XFR Initialize ‘01’:XFR ABORT ‘10’:XFR START		(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	INT SEL 0:CHP SEL 1:FOP SEL
2E	FDTA::PnXFC							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	XFR SEL ‘010’: DEBUG MODE CACHE ACCESS ‘011’: 16B - 128B CACHE ACCESS		
2F	FDTA::PnXFC							
	(RSV)	(RSV)	DATA FORMAT ‘10’:NO FLRC FORMAT ‘11’:FLRC FORMAT	(RSV)	16 XFR CNT ‘000’:16B ACCESS ‘011’:64B ACCESS			
30	FDTA::PnXFC							
	(RSV)	(RSV)	XBF CHAIN (Transfer Chain Number :1 - 32)					
31	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

(Note 1) SubCode Bit 5: CHSN CHK2 detected
SubCode Bit 6: PMA CHK2 detected
SubCode Bit 7: PCI CHK2 detected

Copyright ©2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(1) Byte28 = 00/1F and Byte32 = 58/59 (1/4)

	0	1	2	3	4	5	6	7
40		CHA::CK2AST0						
	RDBF PLRC ERR	SLRC ERR	LA ERR	CBUF DT PARITY ERR	SEARCH ERR	SEARCH DT ERR	WRBF INPUT DT PARITY ERR	BYTE ALIGNME-NT ERR
41		CHA::CK2AST0						
	LCM OUTPUT DT PARITY ERR	(RSV)	LA PARITY ERR	RDBF OUTPUT DT PARITY ERR	HSN PACKET LEN PARITY ERR	(RSV)	(RSV)	(RSV)
42		CHA::CK2AST2						
	PLIST XFR SEQ PARITY ERR	XR SET XFR SEQ PARITY ERR	PLIST OUT PARITY ERR	PLIST IN PARITY ERR	CBP CNT PARITY ERR	CBUF CKDDL PARITY ERR	TBP PARITY ERR	XFR MODE ERR
43		CHA::CK2AST2						
	(RSV)	LCM CKDDL PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
44		CHA::CK2AST1						
	FBADL PARITY ERR	SGOP PARITY ERR	PFC PARITY ERR	WRBF CNT PARITY ERR	RDBF CNT PARITY ERR	PACKET SEQ PARITY ERR	UNMATCH ERR0	UNMATCH ERR1
45		CHA::CK2AST1						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
46		CHA::CK2AST1						
	SOP PARITY ERR	BOP PARITY ERR	CKDFBA CNG CKDDL PARITY ERR	CKDFBA CNG SEQ PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
47		CHA::CK2AST1						
	SLAVE1 NEXTSEG ADR PARITY ERR	SLAVE1 HSN ADR PARITY ERR	SLAVE2 NEXTSEG ADR PARITY ERR	SLAVE2 HSN ADR PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
48		CHA::CHK2ASTS						
	WRBF RD ADR PNT PARITY ERR	RDBF WT ADR PNT PARITY ERR	SC CNT PARITY ERR	LOS CNT PARITY ERR	HARD TIMER PARITY ERR	WRBF PLRC ERR	HSN ADR PARITY ERR	WRBF OUT DT PARITY ERR
49		CHA::CHK2ASTS						
	P0 Recive PARITY ERR	P1 Recive PARITY ERR	X0 Recive PARITY ERR	X1 Recive PARITY ERR	ADRM PARITY ERR	ADRS PARITY ERR	ADRP PARITY ERR	CMD PARITY ERR
4A		CHA::CHK2ASTS						
	XFR CNT PARITY ERR	ILPRM0	ILPRM1	ILPRM2	ILPRM3	ILPRM4	ILPRM5	ILPRM6
4B		CHA::CHK2ASTS						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4C		CHA::ADP_CK21						
	SR0 PARITY ERR	CMWAD PARITY ERR	CMWD PARITY ERR	TSEQ PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
4D		CHA::ADP_CK22						
	LCM-A DATA PARITY ERR	LCM-B DATA PARITY ERR	LCM-C DATA PARITY ERR	LCM-D DATA PARITY ERR	LCM-E DATA PARITY ERR	LCM-F DATA PARITY ERR	LCM-G DATA PARITY ERR	LCM-H DATA PARITY ERR
4E		CHA::CHK2DSTS						
	P0 ERR	P1 ERR	CARB	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4F		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

Copyright ©2000, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(1) Byte28 = 00/1F and Byte32 = 58/59 (2/4)

	0	1	2	3	4	5	6	7
50	CHA_CHK2CSTS							
	TIME OUT0	TIME OUT1	TIME OUT2	HSN RD PLRC ERR	STATUS0 PLRC ERR	STATUS1 PLRC ERR	HSN RD PLRC-INV ERR	STATUS0 PLRC ERR
51	CHA_CHK2CSTS							
	STATUS1 PLRC ERR	HSN RD END-CODE ERR	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	(RSV)	(RSV)	STATUS0 PKID ERR	STATUS1 PKID ERR
52	CHA_CHK2CSTS							
	STATUS0 BYTE0/1 ERR	STATUS1 BYTE0/1 ERR	ACK ERR	ERRINT	LOS	P0 Send PARITY ERR	P1 Send PARITY ERR	X0 Send PARITY ERR
53	CHA_CHK2CSTS							
	X1 Send PARITY ERR	STATUS0 CARB PARITY ERR	STATUS0 CMA PARITY ERR	STATUS1 CARB PARITY ERR	STATUS1 CMA PARITY ERR	(RSV)	(RSV)	(RSV)
54	CHA::ADP_SELP							
	LCM-A SELECT	LCM-B SELECT	LCM-C SELECT	LCM-D SELECT	LCM-E SELECT	LCM-F SELECT	LCM-G SELECT	LCM-H SELECT
55	CHA::ADP_EALT							
	LCP-A CHK1 Detected	LCP-B CHK1 Detected	LCP-C CHK1 Detected	LCP-D CHK1 Detected	LCP-E CHK1 Detected	LCP-F CHK1 Detected	LCP-G CHK1 Detected	LCP-H CHK1 Detected
56	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
57	CHA::CBP							
	CBUF Data Transfer Start Address							
58	CHA::CKDDL							
	Transfer Data Length(CKD)							
59	CHA::CKDDL							
	Transfer Data Length(CKD)							
5A	CHA::FBADL							
	Transfer Data Length(FBA)							
5B	CHA::FBADL							
	Transfer Data Length(FBA)							
5C	CHA::PDS							
	PLIST MEM FULL	(RSV)	(RSV)	(RSV)	PLHLD NE0	PLHLD EQ0	(RSV)	(RSV)
5D	CHA::PLIN							
	PLIST Setting Parameter Memory Page Pointer (BYTE0)							
5E	CHA::PLOUT							
	Parameter Decoder Processing PLIST Page Pointer (BYTE0)							
5F	CHA::PFC							
	Packet Frow Counter (Packet Number Able to Transfer)							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(1) Byte28 = 00/1F and Byte32 = 58/59 (3/4)

	0	1	2	3	4	5	6	7
60	CHA::MCSA00 Slave 1 CACHE Tranfer Address (BYTE0)							
61	CHA::MCSA00 Slave 1 CACHE Tranfer Address (BYTE1)							
62	CHA::MCSA01 Slave 1 CACHE Tranfer Address (BYTE2)							
63	CHA::MCSA01 Slave 1 CACHE Tranfer Address (BYTE3)							
64	CHA::SCSA00 Slave 2 CACHE Tranfer Address (BYTE0)							
65	CHA::SCSA00 Slave 2 CACHE Tranfer Address (BYTE1)							
66	CHA::SCSA01 Slave 2 CACHE Tranfer Address (BYTE2)							
67	CHA::SCSA01 Slave 2 CACHE Tranfer Address (BYTE3)							
68	CHA::CSPGR							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
69	CHA::CSPGR							
	Slave 1 REG Access Flag	Slave 1 CARB Access Flag	(RSV)	(RSV)	Slave 2 REG Access Flag	Slave 2 CARB Access Flag	(RSV)	(RSV)
6A	CHA::PCMD1 CACHE Transfer Command (BYTE0)							
6B	CHA::PCMD1 CACHE Transfer Command (BYTE1)							
6C	CHA::PCMD2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6D	CHA::PCMD2 CACHE Transfer Command (BYTE2)							
6E	CHA::LPEN							
	C Path#00 ENABLE	C Path#01 ENABLE	C Path#02 ENABLE	C Path#03 ENABLE	C Path#10 ENABLE	C Path#11 ENABLE	C Path#12 ENABLE	C Path#13 ENABLE
6F	CHA::IMPZREF0							
	IMP Setting Value for LSI_UP Side High-Level				IMP Setting Value for LSI_UP Side Low-Level			

Copyright ©2000, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(1) Byte28 = 00/1F and Byte32 = 58/59 (4/4)

	0	1	2	3	4	5	6	7
70	CHA::LA0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
71	CHA::LA0							
	LA Expected Value (BYTE0)							
72	CHA::LA1							
	LA Expected Value (BYTE1)							
73	CHA::LA1							
	LA Expected Value (BYTE2)							
74	CHA::LA2							
	LA Expected Value (BYTE3)							
75	CHA::LA2							
	LA Expected Value (BYTE4)							
76	CHA::SOP							
	Subblock Offset Pointer							
77	CHA::SOP							
	Subblock Offset Pointer							
78	CHA::BOP							
	Block Offset Pointer							
79	CHA::BOP							
	Block Offset Pointer							
7A	CHA::POP							
	Packet Offset Pointer							
7B	CHA::POP							
	Packet Offset Pointer							
7C	CHA::SGOP							
	Segment Offset Pointer							
7D	CHA::SGOP							
	Segment Offset Pointer							
7E	Micro Information							
	Error Devided Result Code							
7F	Micro Information							
	CHK2 Detected Counter (Low)							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail

(2) Byte28 = 00/1F/20/28/2F/3F and Byte32 ≠ 58/59 and Byte42 = 58/59

	0	1	2	3	4	5	6	7
40		Causal Key code						
41		Causal Format/Message						
42		Causal Module ID						
43		Causal Routine ID						
44		VDEV and slot number						
45								
46								
47								
48		Slot status						
49								
4A								
4B								
4C		Information of Micro Program						
4D								
4E								
4F								
50		Internal Siearch Parameter (Cylinder number)						
51								
52		Internal Siearch Parameter (Head number)						
53		Internal Siearch Parameter (Reacord number)						
54		Information of Micro Program						
55								
56								
57								
58								
59								
5A								
5B								
5C								
5D								
5E		Curent Command Code						
5F		Old Command Code						
60		Information of Micro Program						
61								
62								
63								
64								
65								
66								
67								
68								
69								
6A								
6B								
6C								
6D								
6E								
6F								
70								
71								
72								
73								
74								
75								
76								
77								
78								
79								
7A								
7B								
7C		Record number in CBUF						
7D		Key Length in CBUF						
7E		Data Length in CBUF						
7F								

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail

(3) Byte28 = 00/1F/20/28/2F/3F and Byte32 ≠ 58/59 and Byte42 ≠ 58/59

	0	1	2	3	4	5	6	7
40		Causal Key code						
41		Causal Format/Message						
42		Causal Module ID						
43		Causal Routine ID						
44		Information of Micro Program						
45								
46								
47								
48								
49								
4A								
4B								
4C								
4D								
4E								
4F								
50								
51								
52								
53								
54								
55								
56								
57								
58								
59								
5A								
5B								
5C								
5D								
5E		Curent Command Code						
5F		Old Command Code						
60		Information of Micro Program						
61								
62								
63								
64								
65								
66								
67								
68								
69								
6A								
6B								
6C								
6D								
6E								
6F								
70								
71								
72								
73								
74								
75								
76								
77								
78								
79								
7A								
7B								
7C								
7D								
7E								
7F								

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(4) Byte28 = 80 or 83 or 85 or 87 (1/4)

	0	1	2	3	4	5	6	7
40		FORMAT NO.						
		x'01'						
41		LPA::PnICNTL						
	(RSV)	(RSV)	LPDB INT ENABLE	CHK2A INT ENABLE 4	CHK2A INT ENABLE 3	CHK2A INT ENABLE 2	CHK2A INT ENABLE 1	CHK2A INT ENABLE 0
42		LPA::PnICNTL						
	PLDB31-28 ENABLE	PLDB27-24 ENABLE	PLDB23-20 ENABLE	PLDB19-16 ENABLE	OTHER INT ENABLE	PFA XFR END INT ENABLE	LPA XFR END INT ENABLE	PLDB INT ENABLE
43		LPA::PnISTAT						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	CHK2A ERR 4
44		LPA::PnISTAT						
	CHK2A ERR 3	CHK2A ERR 2	CHK2A ERR 1	CHK2A ERR 0	OTHER INT (960RD FAULT)	PFA XFR END	LPA XFR END	PLDB
45		FDTA::PCICHK2A						
	MWB8B PARITY ERR	MWB4B PARITY ERR	MWB8B PARITY GEN CHK ERR	MWB4B PARITY GEN CHK ERR	MRB0 PARITY ERR	MRB1 PARITY ERR	(RSV)	PCI IN PARITY ERR
46		FDTA::PCICHK2A						
	MWB8B PARITY GEN ERR	MWB4B PARITY GEN ERR	PCI ADR PARITY ERR	PCI ADR PARITY GEN CHK ERR	(RSV)	(RSV)	(RSV)	PCI IN SERR
47		FDTA::PCICHK2A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
48		FDTA::PCICHK2A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
49		FDTA::PCICHK2B0						
	DBF0 B0 PARITY ERR	DBF0 B1 PARITY ERR	DBF0 B2 PARITY ERR	DBF0 B3 PARITY ERR	DBF0 B4 PARITY ERR	DBF0 B5 PARITY ERR	DBF0 B6 PARITY ERR	DBF0 B7 PARITY ERR
4A		FDTA::PCICHK2B0						
	DBF1 B0 PARITY ERR	DBF1 B1 PARITY ERR	DBF1 B2 PARITY ERR	DBF1 B3 PARITY ERR	DBF1 B4 PARITY ERR	DBF1 B5 PARITY ERR	DBF1 B6 PARITY ERR	DBF1 B7 PARITY ERR
4B		FDTA::PCICHK2B0						
	DBF IN PARITY ERR 00	DBF IN PARITY ERR 01	DBF IN PARITY ERR 10	DBF IN PARITY ERR 11	(RSV)	DBF 16BI PARITY ERR	DBF 16B0 PARITY ERR	(RSV)
4C		FDTA::PCICHK2B0						
	XBF B0 PARITY ERR	XBF B1 PARITY ERR	XBF B2 PARITY ERR	XBF B3 PARITY ERR	(RSV)	(RSV)	(RSV)	XBF IN PARITY ERR
4D		FDTA::PCICHK2B1						
	PCI SEQ PARITY ERR	WTBDF SEQ PARITY ERR	WTXBF SEQ PARITY ERR	RDBDF SEQ PARITY ERR	MRB8B PARITY GEN ERR	MRB4B PARITY GEN ERR	XWB WPTR PARITY ERR	XWB SPTR PARITY ERR
4E		FDTA::PCICHK2B1						
	HWB WPTR PARITY ERR	HWB SPTR PARITY ERR	HRB WPTR PARITY ERR	HRB SPTR PARITY ERR	DLRC CMP ERR	DLRC PARITY ERR	(RSV)	PWD LRC ERR
4F		FDTA::PCICHK2B1						
	HWB PARITY ERR 00	HWB PARITY ERR 01	HWB PARITY ERR 10	HWB PARITY ERR 11	HRB PARITY ERR 00	HRB PARITY ERR 01	HRB PARITY ERR 10	HRB PARITY ERR 11

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(4) Byte28 = 80 or 83 or 85 or 87 (2/4)

	0	1	2	3	4	5	6	7
50	FDTA::PCICHK2B1							
	XWB0 PARITY ERR	XWB1 PARITY ERR	MRB0 PARITY ERR	MRB1 PARITY ERR	DWA XAD PARITY ERR	PCI XAD PARITY ERR	DBFW ADRCNT PARITY ERR	DBFR ADRCNT PARITY ERR
51	FDTA::PCICHK2B2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
52	FDTA::PCICHK2B2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
53	FDTA::PCICHK2B2							
	(RSV)	(RSV)	(RSV)	PCI OVER RUN ERR	INV MEMACS ERR	CRC POINTER ERR	DWA CMP ERR	DRA CMP ERR
54	FDTA::PCICHK2B2							
	DBF WT ACSERR	DBF RD ACSERR	DMA DSTT ERR	XFC MODE ERR	ACC WIDTH ERR	STADR ACC ERR	DBF ACC ERR	XBF ACC ERR
55	FDTA::DMACHK2BST0							
	DMA TJ0 PARITY ERR	DMA TJ1 PARITY ERR	DMA TJ2 PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
56	FDTA::DMACHK2BST0							
	CHAIN CNT PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
57	FDTA::DMACHK2CST0							
	HSN ADR CNT1 PARITY ERR0	HSN ADR CNT1 PARITY ERR1	HSN ADR CNT1 PARITY ERR2	HSN ADR CNT1 PARITY ERR3	HSN ADR CNT1 PARITY ERR4	(RSV)	(RSV)	(RSV)
58	FDTA::DMACHK2CST0							
	HSN ADR CNT2 PARITY ERR0	HSN ADR CNT2 PARITY ERR1	HSN ADR CNT2 PARITY ERR2	HSN ADR CNT2 PARITY ERR3	HSN ADR CNT2 PARITY ERR4	(RSV)	(RSV)	(RSV)
59	FDTA::DMACHK2CST0							
	SUB BLOCK PARITY ERR	SUB BLOCK CNT PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5A	FDTA::DMACHK2CST0							
	XBF CMD PARITY ERR	LA CNT PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5B	FDTA::DMACHK2CST1							
	HSN RD ADR CNT PARITY ERR	HSN WT ADR CNT PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5C	FDTA::DMACHK2CST1							
	PWB LRC PARITY ERR0	PWB LRC PARITY ERR1	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5D	FDTA::DMACHK2CST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	DMA TIME OUT
5E	FDTA::DMACHK2CST2							
	SDBF0 PARITY ERR	SDBF1 PARITY ERR	SDBF2 PARITY ERR	SDBF3 PARITY ERR	SDLRC ERR	DBF PARITY ERR	XBF BLOCKCODE ERR	XBF PARITY ERR
5F	FDTA::DMACHK2CST2							
	SLRC GEN PARITY ERR	SLRC CHK PARITY ERR	LA ERR	SLRC ERR	(RSV)	(RSV)	RAID MODE ERR	BLKBD ACSERR

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(4) Byte28 = 80 or 83 or 85 or 87 (3/4)

	0	1	2	3	4	5	6	7
60	FDTA::DMACHK2CST2							
	RD DT END-CODE ERR0	RD DT END-CODE ERR1	RD DT END-CODE ERR2	RD DT END-CODE ERR3	(RSV)	(RSV)	RD DT INV-PLRC ERR0	RD DT INV-PLRC ERR1
61	FDTA::DMACHK2CST2							
	(RSV)	(RSV)	(RSV)	(RSV)	DMA TIMER PARITY ERR	(RSV)	(RSV)	DMA SEQ PARITY ERR
62	FDTA::H0CHK2BST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 DBF PARITY ERR
63	FDTA::H0CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 PWB0 PARITY ERR
64	FDTA::H0CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 PWB1 PARITY ERR
65	FDTA::H0CHK2BST2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 SNB0 PARITY ERR	P0 SNB1 PARITY ERR
66	FDTA::H0CHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 TJ1 PARITY ERR	P0 TJ2 PARITY ERR
67	FDTA::H0CHK2CST0							
	P0 TX1 TIMER0 PARITY ERR	(RSV)	(RSV)	(RSV)	P0 TX1 PTR PARITY ERR	P0 TX1 CNT PARITY ERR	(RSV)	P0 TX1 SEQ PARITY ERR
68	FDTA::H0CHK2CST1							
	P0 TX2 TIMER0 PARITY ERR	P0 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P0 TX1 PTR PARITY ERR	(RSV)	(RSV)	P0 TX1 SEQ PARITY ERR
69	FDTA::H0CHK2CST2							
	P0 PRBPTR CMP ERR	P0 PRBPTR PARITY ERR	P0 PRBPTR CMP ERR	P0 PRBPTR PARITY ERR	P0 PRBPTR 0 CMP ERR	P0 PRBPTR 1 CMP ERR	P0 PRBPTR 0 PARITY ERR	P0 PRBPTR 1 PARITY ERR
6A	FDTA::H0CHK2CST2							
	P0 RX TIMER0 PARITY ERR	P0 RX TIMER1 PARITY ERR	(RSV)	(RSV)	P0 RX PTR PARITY ERR	P0 RX CNT PARITY ERR	(RSV)	P0 RX SEQ PARITY ERR
6B	FDTA::H1CHK2BST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 DBF PARITY ERR
6C	FDTA::H1CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 PWB0 PARITY ERR
6D	FDTA::H1CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 PWB1 PARITY ERR
6E	FDTA::H1CHK2BST2							
0	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 SNB0 PARITY ERR	P1 SNB1 PARITY ERR
6F	FDTA::H1CHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 TJ1 PARITY ERR	P1 TJ2 PARITY ERR

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(4) Byte28 = 80 or 83 or 85 or 87 (4/4)

	0	1	2	3	4	5	6	7
70	FDTA::H1CHK2CST0							
	P1 TX2 TIMER0 PARITY ERR	P1 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P1 TX1 PTR PARITY ERR	(RSV)	(RSV)	P1 TX1 SEQ PARITY ERR
71	FDTA::H1CHK2CST1							
	P1 TX2 TIMER0 PARITY ERR	P1 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P1 TX1 PTR PARITY ERR	(RSV)	(RSV)	P1 TX1 SEQ PARITY ERR
72	FDTA::H1CHK2CST2							
	P1 PRBPTR CMP ERR	P1 PRBPTR PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
73	FDTA::H1CHK2CST2							
	P1 RX TIMER0 PARITY ERR	P1 RX TIMER1 PARITY ERR	(RSV)	(RSV)	P1 RX PTR PARITY ERR	P1 RX CNT PARITY ERR	(RSV)	P1 RX SEQ PARITY ERR
74	FDTA::COMMCHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
75	FDTA::COMMCHK2CST0							
	(RSV)	(RSV)	80ns TIMER CNT PARITY ERR	60ns TIMER CNT PARITY ERR	(RSV)	ARB0 SEQ PARITY ERR	ARB1 SEQ PARITY ERR	ARB CMP ERR
76	FDTA::PnMSADR							
	(RSV)	(RSV)	(RSV)	XBF Data Transfer Parameter Address (x‘00’ - x‘1F’)				
77	FDTA::CBEN							
	C Path#00 ENABLE	C Path#01 ENABLE	C Path#02 ENABLE	C Path#03 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
78	FDTA::CBEN							
	C Path#10 ENABLE	C Path#11 ENABLE	C Path#12 ENABLE	C Path#13 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
79	FDTA::PKID							
	(RSV)	(RSV)	(RSV)	(RSV)	PKID#			
7A	FDTA::MONI							
	MPID#				LSI REV.			
7B	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7C	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7D	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7E	Micro Information							
	Error Devided Result Code							
7F	Micro Information							
	CHK2 Detected Counter (Low)							

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(5) Byte28 = 81 (1/4)

	0	1	2	3	4	5	6	7
40		FORMAT NO.						
		x‘02’						
41		LPA::PnICNTL						
	(RSV)	(RSV)	LPDB INT ENABLE	CHK2A INT ENABLE 4	CHK2A INT ENABLE 3	CHK2A INT ENABLE 2	CHK2A INT ENABLE 1	CHK2A INT ENABLE 0
42		LPA::PnICNTL						
	PLDB31-28 ENABLE	PLDB27-24 ENABLE	PLDB23-20 ENABLE	PLDB19-16 ENABLE	OTHER INT ENABLE	PFA XFR END INT ENABLE	LPA XFR END INT ENABLE	PLDB INT ENABLE
43		LPA::PnISTAT						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	CHK2A ERR 4
44		LPA::PnISTAT						
	CHK2A ERR 3	CHK2A ERR 2	CHK2A ERR 1	CHK2A ERR 0	OTHER INT (960RD FAULT)	PFA XFR END	LPA XFR END	PLDB
45		LPA::PnLCK2A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
46		LPA::PnLCK2A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
47		LPA::PnLCK2A						
	(RSV)	PCI MASTER READ PARITY ERR	PCI MASTER PERR IN	PCI MASTER PERR OUT	(RSV)	PCI TARGET READ PARITY ERR	PCI TARGET PERR IN	PCI TARGET PERR OUT
48		LPA::PnLCK2A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	LBUS TIME OVER	LBUS READ PARITY ERR	LBUS WRITE PARITY ERR
49		LPA::PnCSTA						
	DETECTED PARITY ERR	DETECTED SYSTEM ERR	RECEIVED MASTER ABORT	RECEIVED TARGET ABORT	(RSV)	DEVSEL TIMING 01:medium		DATA PARITY REPORT
4A		LPA::PnCSTA						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4B		LPA::PnCCMD						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4C		LPA::PnCCMD						
	(RSV)	ENABLE PARITY RESPONSE	(RSV)	(RSV)	(RSV)	ENABLE BUS MASTERING	ENABLE MEMORY SPACE	ENABLE I/O SPACE
4D		LPA::PnPACNF						
		PCI CNF ADDRESS (BYTE0)						
4E		LPA::PnPACNF						
		PCI CNF ADDRESS (BYTE1)						
4F		LPA::PnPACNF						
		PCI CNF ADDRESS (BYTE2)						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(5) Byte28 = 81 (2/4)

	0	1	2	3	4	5	6	7
50	LPA::PnPACNF							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	CONFIGURATION TYPE '00':TYPE0 '01':TYPE1	
51	LPA::PnPAIO							
	PCI I/O ADDRESS (BYTE0)							
52	LPA::PnPAIO							
	PCI I/O ADDRESS (BYTE1)							
53	LPA::PnPAIO							
	PCI I/O ADDRESS (BYTE2)							
54	LPA::PnPAIO							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
55	LPA::PnPAMEM							
	PCI MEMORY ADDRESS (BYTE0)							
56	LPA::PnPAMEM							
	PCI MEMORY ADDRESS (BYTE1)							
57	LPA::PnPAMEM							
	PCI MEMORY ADDRESS (BYTE2)							
58	LPA::PnPAMEM							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
59	LPA::PnPAXFR							
	PCI XFR ADDRESS (BYTE0)							
5A	LPA::PnPAXFR							
	PCI XFR ADDRESS (BYTE1)							
5B	LPA::PnPAXFR							
	PCI XFR ADDRESS (BYTE2)							
5C	LPA::PnPAXFR							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5D	LPA::PnACTRL1							
	XFR READ COMMAND				XFR WRITE COMMAND			
5E	LPA::PnACTRL1							
	MEMORY READ COMMAND				MEMORY WRITE COMMAND			
5F	LPA::PnACTRL1							
	I/O READ COMMAND				I/O WRITE COMMAND			

Copyright ©2000, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(5) Byte28 = 81 (3/4)

	0	1	2	3	4	5	6	7
60	LPA::PnACTRL1							
	CONFIGURATION READ COMMAND				CONFIGURATION WRITE COMMAND			
61	FDTA::PCICHK2A							
	MWB8B PARITY ERR	MWB4B PARITY ERR	MWB8B PARITY GEN CHK ERR	MWB4B PARITY GEN CHK ERR	MRB0 PARITY ERR	MRB1 PARITY ERR	(RSV)	PCI IN PARITY ERR
62	FDTA::PCICHK2A							
	(RSV)	(RSV)	PCI ADR PARITY ERR	PCI ADR PARITY GEN CHK ERR	(RSV)	(RSV)	(RSV)	PCI IN SERR
63	FDTA::PCICHK2A							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
64	FDTA::PCICHK2A							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
65	FDTA::PCICHK2B0							
	DBF0 B0 PARITY ERR	DBF0 B1 PARITY ERR	DBF0 B2 PARITY ERR	DBF0 B3 PARITY ERR	DBF0 B4 PARITY ERR	DBF0 B5 PARITY ERR	DBF0 B6 PARITY ERR	DBF0 B7 PARITY ERR
66	FDTA::PCICHK2B0							
	DBF1 B0 PARITY ERR	DBF1 B1 PARITY ERR	DBF1 B2 PARITY ERR	DBF1 B3 PARITY ERR	DBF1 B4 PARITY ERR	DBF1 B5 PARITY ERR	DBF1 B6 PARITY ERR	DBF1 B7 PARITY ERR
67	FDTA::PCICHK2B0							
	DBF IN PARITY ERR 00	DBF IN PARITY ERR 01	DBF IN PARITY ERR 10	DBF IN PARITY ERR 11	(RSV)	DBF 16BI PARITY ERR	DBF 16B0 PARITY ERR	(RSV)
68	FDTA::PCICHK2B0							
	XBF B0 PARITY ERR	XBF B1 PARITY ERR	XBF B2 PARITY ERR	XBF B3 PARITY ERR	(RSV)	(RSV)	(RSV)	XBF IN PARITY ERR
69	FDTA::PCICHK2B1							
	PCI SEQ PARITY ERR	WTBDF SEQ PARITY ERR	WTXBF SEQ PARITY ERR	RDBDF SEQ PARITY ERR	MRB8B PARITY GEN ERR	MRB4B PARITY GEN ERR	XWB WPTR PARITY ERR	XWB SPTR PARITY ERR
6A	FDTA::PCICHK2B1							
	HWB WPTR PARITY ERR	HWB SPTR PARITY ERR	HRB WPTR PARITY ERR	HRB SPTR PARITY ERR	DLRC CMP ERR	DLRC PARITY ERR	(RSV)	PWD LRC ERR
6B	FDTA::PCICHK2B1							
	HWB PARITY ERR 00	HWB PARITY ERR 01	HWB PARITY ERR 10	HWB PARITY ERR 11	HRB PARITY ERR 00	HRB PARITY ERR 01	HRB PARITY ERR 10	HRB PARITY ERR 11
6C	FDTA::PCICHK2B1							
	XWB0 PARITY ERR	XWB1 PARITY ERR	MRB0 PARITY ERR	MRB1 PARITY ERR	DWA XAD PARITY ERR	PCI XAD PARITY ERR	DBFW ADRCNT PARITY ERR	DBFR ADRCNT PARITY ERR
6D	FDTA::PCICHK2B2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6E	FDTA::PCICHK2B2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6F	FDTA::PCICHK2B2							
	(RSV)	(RSV)	(RSV)	PCI OVER RUN ERR	INV MEMACS ERR	CRC POINTER ERR	DWA CMP ERR	DRA CMP ERR

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(5) Byte28 = 81 (4/4)

	0	1	2	3	4	5	6	7
70	FDTA::PCICHK2B2							
	DBF WT ACSERR	DBF RD ACSERR	DMA DSTT ERR	XFC MODE ERR	ACC WIDTH ERR	STADR ACC ERR	DBF ACC ERR	XBF ACC ERR
71	FDTA::COMMCHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
72	FDTA::COMMCHK2CST0							
	(RSV)	(RSV)	80ns TIMER CNT PARITY ERR	60ns TIMER CNT PARITY ERR	(RSV)	ARB0 SEQ PARITY ERR	ARB1 SEQ PARITY ERR	ARB CMP ERR
73	FDTA::HCMD							
	CACHE Transfer Command (BYTE0)							
74	FDTA::HCMD							
	CACHE Transfer Command (BYTE1)							
75	FDTA::HCMD							
	CACHE Transfer Command (BYTE2)							
76	FDTA::PnMSADR							
	(RSV)	(RSV)	(RSV)	XBF Data Transfer Parameter Address (x‘00’ - x‘1F’)				
77	FDTA::CBEN							
	C Path#00 ENABLE	C Path#01 ENABLE	C Path#02 ENABLE	C Path#03 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
78	FDTA::CBEN							
	C Path#10 ENABLE	C Path#11 ENABLE	C Path#12 ENABLE	C Path#13 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
79	FDTA::PKID							
	(RSV)	(RSV)	(RSV)	(RSV)	PKID#			
7A	FDTA::MONI							
	MPID#				LSI REV.			
7B	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7C	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7D	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7E	Micro Information							
	Error Devided Result Code							
7F	Micro Information							
	CHK2 Detected Counter (Low)							

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(6) Byte28 = 80 or 82 or 84 or 86 (1/4)

	0	1	2	3	4	5	6	7
40		FORMAT NO.						
		x'03'						
41		LPA::PnICNTL						
	(RSV)	(RSV)	LPDB INT ENABLE	CHK2A INT ENABLE 4	CHK2A INT ENABLE 3	CHK2A INT ENABLE 2	CHK2A INT ENABLE 1	CHK2A INT ENABLE 0
42		LPA::PnICNTL						
	PLDB31-28 ENABLE	PLDB27-24 ENABLE	PLDB23-20 ENABLE	PLDB19-16 ENABLE	OTHER INT ENABLE	PFA XFR END INT ENABLE	LPA XFR END INT ENABLE	PLDB INT ENABLE
43		LPA::PnISTAT						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	CHK2A ERR 4
44		LPA::PnISTAT						
	CHK2A ERR 3	CHK2A ERR 2	CHK2A ERR 1	CHK2A ERR 0	OTHER INT (960RD FAULT)	PFA XFR END	LPA XFR END	PLDB
45		FDTA::DMACHK2BST0						
	DMA TJ0 PARITY ERR	DMA TJ1 PARITY ERR	DMA TJ2 PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
46		FDTA::DMACHK2BST0						
	CHAIN CNT PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
47		FDTA::DMACHK2CST0						
	HSN ADR CNT1 PARITY ERR0	HSN ADR CNT1 PARITY ERR1	HSN ADR CNT1 PARITY ERR2	HSN ADR CNT1 PARITY ERR3	HSN ADR CNT1 PARITY ERR4	(RSV)	(RSV)	(RSV)
48		FDTA::DMACHK2CST0						
	HSN ADR CNT2 PARITY ERR0	HSN ADR CNT2 PARITY ERR1	HSN ADR CNT2 PARITY ERR2	HSN ADR CNT2 PARITY ERR3	HSN ADR CNT2 PARITY ERR4	(RSV)	(RSV)	(RSV)
49		FDTA::DMACHK2CST0						
	SUB BLOCK PARITY ERR	SUB BLOCK CNT PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4A		FDTA::DMACHK2CST0						
	XBF CMD PARITY ERR	LA CNT PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4B		FDTA::DMACHK2CST1						
	HSN RD ADR CNT PARITY ERR	HSN WT ADR CNT PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4C		FDTA::DMACHK2CST1						
	PWB LRC PARITY ERR0	PWB LRC PARITY ERR1	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4D		FDTA::DMACHK2CST1						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	DMA TIME OUT
4E		FDTA::DMACHK2CST2						
	SDBF0 PARITY ERR	SDBF1 PARITY ERR	SDBF2 PARITY ERR	SDBF3 PARITY ERR	SDLRC ERR	DBF PARITY ERR	XBF BLOCKCODE ERR	XBF PARITY ERR
4F		FDTA::DMACHK2CST2						
	SLRC GEN PARITY ERR	SLRC CHK PARITY ERR	LA ERR	SLRC ERR	(RSV)	(RSV)	RAID MODE ERR	BLKBD ACSERR

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(6) Byte28 = 80 or 82 or 84 or 86 (2/4)

	0	1	2	3	4	5	6	7
50	FDTA::DMACHK2CST2							
	RD DT END-CODE ERR0	RD DT END-CODE ERR1	RD DT END-CODE ERR2	RD DT END-CODE ERR3	(RSV)	(RSV)	RD DT INV-PLRC ERR0	RD DT INV-PLRC ERR1
51	FDTA::DMACHK2CST2							
	(RSV)	(RSV)	(RSV)	(RSV)	DMA TIMER PARITY ERR	(RSV)	(RSV)	DMA SEQ PARITY ERR
52	FDTA::H0CHK2BST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 DBF PARITY ERR
53	FDTA::H0CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 PWB0 PARITY ERR
54	FDTA::H0CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 PWB1 PARITY ERR
55	FDTA::H0CHK2BST2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 SNB0 PARITY ERR	P0 SNB1 PARITY ERR
56	FDTA::H0CHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 TJ1 PARITY ERR	P0 TJ2 PARITY ERR
57	FDTA::H0CHK2CST0							
	P0 TX1 TIMER0 PARITY ERR	(RSV)	(RSV)	(RSV)	P0 TX1 PTR PARITY ERR	P0 TX1 CNT PARITY ERR	(RSV)	P0 TX1 SEQ PARITY ERR
58	FDTA::H0CHK2CST1							
	P0 TX2 TIMER0 PARITY ERR	P0 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P0 TX1 PTR PARITY ERR	(RSV)	(RSV)	P0 TX1 SEQ PARITY ERR
59	FDTA::H0CHK2CST2							
	P0 PRBPTR CMP ERR	P0 PRBPTR PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5A	FDTA::H0CHK2CST2							
	P0 RX TIMER0 PARITY ERR	P0 RX TIMER1 PARITY ERR	(RSV)	(RSV)	P0 RX PTR PARITY ERR	P0 RX CNT PARITY ERR	(RSV)	P0 RX SEQ PARITY ERR
5B	FDTA::H1CHK2BST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 DBF PARITY ERR
5C	FDTA::H1CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 PWB0 PARITY ERR
5D	FDTA::H1CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 PWB1 PARITY ERR
5E	FDTA::H1CHK2BST2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 SNB0 PARITY ERR	P1 SNB1 PARITY ERR
5F	FDTA::H1CHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 TJ1 PARITY ERR	P1 TJ2 PARITY ERR

Copyright ©2000, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(6) Byte28 = 80 or 82 or 84 or 86 (3/4)

	0	1	2	3	4	5	6	7
60	FDTA::H1CHK2CST0							
	P1 TX2 TIMER0 PARITY ERR	P1 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P1 TX1 PTR PARITY ERR	(RSV)	(RSV)	P1 TX1 SEQ PARITY ERR
61	FDTA::H1CHK2CST1							
	P1 TX2 TIMER0 PARITY ERR	P1 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P1 TX1 PTR PARITY ERR	(RSV)	(RSV)	P1 TX1 SEQ PARITY ERR
62	FDTA::H1CHK2CST2							
	P1 PRBPTR CMP ERR	P1 PRBPTR PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
63	FDTA::H1CHK2CST2							
	P1 RX TIMER0 PARITY ERR	P1 RX TIMER1 PARITY ERR	(RSV)	(RSV)	P1 RX PTR PARITY ERR	P1 RX CNT PARITY ERR	(RSV)	P1 RX SEQ PARITY ERR
64	FDTA::HADR1UCNT							
	Slave 1 CACHE Tranfer Address (BYTE0)							
65	FDTA::HADR1LCNT							
	Slave 1 CACHE Tranfer Address (BYTE1)							
66	FDTA::HADR1LCNT							
	Slave 1 CACHE Tranfer Address (BYTE2)							
67	FDTA::HADR1LCNT							
	Slave 1 CACHE Tranfer Address (BYTE3)							
68	FDTA::HADR1LCNT							
	Slave 1 CACHE Tranfer Address (BYTE4)							
69	FDTA::HADR2UCNT							
	Slave 2 CACHE Tranfer Address (BYTE0)							
6A	FDTA::HADR2LCNT							
	Slave 2 CACHE Tranfer Address (BYTE1)							
6B	FDTA::HADR2LCNT							
	Slave 2 CACHE Tranfer Address (BYTE2)							
6C	FDTA::HADR2LCNT							
	Slave 2 CACHE Tranfer Address (BYTE3)							
6D	FDTA::HADR2LCNT							
	Slave 2 CACHE Tranfer Address (BYTE4)							
6E	FDTA::HCMD							
	CACHE Tranfer Command (BYTE0)							
6F	FDTA::HCMD							
	CACHE Tranfer Command (BYTE1)							

Copyright ©2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(6) Byte28 = 80 or 82 or 84 or 86 (4/4)

	0	1	2	3	4	5	6	7
70		FDTA::HCMD						
		CACHE Tranfer Command (BYTE2)						
71		FDTA::LA0						
		LA Expected Value (BYTE0)						
72		FDTA::LA1						
		LA Expected Value (BYTE1)						
73		FDTA::LA1						
		LA Expected Value (BYTE2)						
74		FDTA::LA1						
		LA Expected Value (BYTE3)						
75		FDTA::LA1						
		LA Expected Value (BYTE4)						
76		FDTA::PnMSADR						
	(RSV)	(RSV)	(RSV)	XBF Data Transfer Parameter Address (x‘00’ - x‘1F’)				
77		FDTA::CBEN						
	C Path#00 ENABLE	C Path#01 ENABLE	C Path#02 ENABLE	C Path#03 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
78		FDTA::CBEN						
	C Path#10 ENABLE	C Path#11 ENABLE	C Path#12 ENABLE	C Path#13 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
79		FDTA::PKID						
	(RSV)	(RSV)	(RSV)	(RSV)	PKID#			
7A		FDTA::MONI						
	MPID#				LSI REV.			
7B		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7C		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7D		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7E		Micro Information						
		Error Devided Result Code						
7F		Micro Information						
		CHK2 Detected Counter (Low)						

Copyright ©2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(7) Byte28 = 90 or 93 or 95 or 97 (1/4)

	0	1	2	3	4	5	6	7
40		FORMAT NO. x'11'						
41		LPA::PnICNTL						
	(RSV)	(RSV)	LPDB INT ENABLE	CHK2A INT ENABLE 4	CHK2A INT ENABLE 3	CHK2A INT ENABLE 2	CHK2A INT ENABLE 1	CHK2A INT ENABLE 0
42		LPA::PnICNTL						
	PLDB31-28 ENABLE	PLDB27-24 ENABLE	PLDB23-20 ENABLE	PLDB19-16 ENABLE	OTHER INT ENABLE	PFA XFR END INT ENABLE	LPA XFR END INT ENABLE	PLDB INT ENABLE
43		LPA::PnISTAT						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	CHK2A ERR 4
44		LPA::PnISTAT						
	CHK2A ERR 3	CHK2A ERR 2	CHK2A ERR 1	CHK2A ERR 0	OTHER INT (960RD FAULT)	PFA XFR END	LPA XFR END	PLDB
45		FDTM::PCICHK2A						
	MWB8B PARITY ERR	MWB4B PARITY ERR	MWB8B PARITY GEN CHK ERR	MWB4B PARITY GEN CHK ERR	PMA MRB0 PARITY ERR	PMA MRB1 PARITY ERR	(RSV)	PCI IN PARITY ERR
46		FDTM::PCICHK2A						
	PMA MRB8B PARITY GEN ERR	PMA MWB4B PARITY GEN ERR	PCI ADR PARITY ERR	PCI ADR PARITY GEN CHK ERR	(RSV)	(RSV)	(RSV)	PCI IN SERR
47		FDTM::PCICHK2A						
	PRFLRC PARITY ERR	PRFLRC ERR	PRA CMP ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
48		FDTM::PCICHK2A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
49		FDTM::PCICHK2B0						
	PPACNT PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	PPBFIN PARITY ERR	PCIPBF PARITY ERR	PBFOUT PARITY ERR
4A		FDTM::PCICHK2B0						
	PWTRFCNT PARITY ERR	PWFLRC PARITY ERR	PRTRFCNT PARITY ERR	PRFLRC PARITY ERR	PRFLRC ERR	(RSV)	(RSV)	(RSV)
4B		FDTM::PCICHK2B0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4C		FDTM::PCICHK2B0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4D		FDTM::PCICHK2B1						
	(RSV)	(RSV)	(RSV)	PMA MRB8B PARITY GEN ERR	PMA MRB4B PARITY GEN ERR	(RSV)	(RSV)	(RSV)
4E		FDTM::PCICHK2B1						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4F		FDTM::PCICHK2B1						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(7) Byte28 = 90 or 93 or 95 or 97 (2/4)

	0	1	2	3	4	5	6	7
50	FDTA::PCICHK2B1							
	(RSV)	(RSV)	PMA MRB0 PARITY ERR	PMA MRB1 PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
51	FDTA::PCICHK2B2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
52	FDTA::PCICHK2B2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
53	FDTA::PCICHK2B2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	PWA CMP ERR	PRA CMP ERR
54	FDTA::PCICHK2B2							
	PBF WT ACS ERR	PBF RD ACS ERR	PMA DSTT ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
55	FDTA::PMACHK2BST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
56	FDTA::PMACHK2BST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
57	FDTA::PMACHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
58	FDTA::PMACHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
59	FDTA::PMACHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5A	FDTA::PMACHK2CST0							
	HSN CMD LOAD PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5B	FDTA::PMACHK2CST1							
	HSN RD ADR CNT PARITY ERR	HSN WT ADRR CNT PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5C	FDTA::PMACHK2CST1							
	PWB LRC PARITY ERR0	PWB LRC PARITY ERR1	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5D	FDTA::PMACHK2CST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	PMA TIME OUT
5E	FDTA::PMACHK2CST2							
	TX FLRC ERR	TXFLRC PARITY ERR	RX FLRC PARITY ERR	RX FLRC PARITY ERR	PBF0 PARITY ERR	PBF1 PARITY ERR	PBF2 PARITY ERR	PBF3 PARITY ERR
5F	FDTA::PMACHK2CST2							
	(RSV)	(RSV)	(RSV)	(RSV)	PMA ACCMD ERR	XFC MODE ERR	RAID MODE ERR	BLK MODE ACSERR

Copyright ©2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(7) Byte28 = 90 or 93 or 95 or 97 (3/4)

	0	1	2	3	4	5	6	7
60	FDTM::PMACHK2CST2							
	RD DT END-CODE ERR0	RD DT END-CODE ERR1	RD DT END-CODE ERR2	RD DT END-CODE ERR3	TX FLRC 0 PADDING ERR	RX FLRC 0 PADDING ERR	RD DT INV-PLRC ERR0	RD DT INV-PLRC ERR1
61	FDTM::PMACHK2CST2							
	HSN PBF IN PARITY ERR	(RSV)	(RSV)	(RSV)	PMA TIMER PARITY ERR	(RSV)	PMA ARB SEQ PARITY ERR	PMA SEQ PARITY ERR
62	FDTM::H0CHK2BST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 DBF PARITY ERR
63	FDTM::H0CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 PWB0 PARITY ERR
64	FDTM::H0CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 PWB1 PARITY ERR
65	FDTM::H0CHK2BST2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 SNB0 PARITY ERR	P0 SNB1 PARITY ERR
66	FDTM::H0CHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 TJ1 PARITY ERR	P0 TJ2 PARITY ERR
67	FDTM::H0CHK2CST0							
	P0 TX1 TIMER0 PARITY ERR	(RSV)	(RSV)	(RSV)	P0 TX1 PTR PARITY ERR	P0 TX1 CNT PARITY ERR	(RSV)	P0 TX1 SEQ PARITY ERR
68	FDTM::H0CHK2CST1							
	P0 TX2 TIMER0 PARITY ERR	P0 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P0 TX1 PTR PARITY ERR	(RSV)	(RSV)	P0 TX1 SEQ PARITY ERR
69	FDTM::H0CHK2CST2							
	(RSV)	(RSV)	P0 PRBPTR CMP ERR	P0 PRBPTR PARITY ERR	P0 PRBPTR 0 CMP ERR	P0 PRBPTR 1 CMP ERR	P0 PRBPTR 0 PARITY ERR	P0 PRBPTR 1 PARITY ERR
6A	FDTM::H0CHK2CST2							
	P0 RX TIMER0 PARITY ERR	P0 RX TIMER1 PARITY ERR	(RSV)	(RSV)	P0 RX PTR PARITY ERR	P0 RX CNT PARITY ERR	(RSV)	P0 RX SEQ PARITY ERR
6B	FDTM::H1CHK2BST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 DBF PARITY ERR
6C	FDTM::H1CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 PWB0 PARITY ERR
6D	FDTM::H1CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 PWB1 PARITY ERR
6E	FDTM::H1CHK2BST2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 SNB0 PARITY ERR	P1 SNB1 PARITY ERR
6F	FDTM::H1CHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 TJ1 PARITY ERR	P1 TJ2 PARITY ERR

Copyright ©2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(7) Byte28 = 90 or 93 or 95 or 97 (4/4)

	0	1	2	3	4	5	6	7
70	FDTM::H1CHK2CST0							
	P1 TX2 TIMER0 PARITY ERR	P1 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P1 TX1 PTR PARITY ERR	(RSV)	(RSV)	P1 TX1 SEQ PARITY ERR
71	FDTM::H1CHK2CST1							
	P1 TX2 TIMER0 PARITY ERR	P1 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P1 TX1 PTR PARITY ERR	(RSV)	(RSV)	P1 TX1 SEQ PARITY ERR
72	FDTM::H1CHK2CST2							
	(RSV)	(RSV)	P1 PRBPTR CMP ERR	P1 PRBPTR PARITY ERR	P1 PRBPTR 0 CMP ERR	P1 PRBPTR 1 CMP ERR	P1 PRBPTR 0 PARITY ERR	P1 PRBPTR 1 PARITY ERR
73	FDTM::H1CHK2CST2							
	P1 RX TIMER0 PARITY ERR	P1 RX TIMER1 PARITY ERR	(RSV)	(RSV)	P1 RX PTR PARITY ERR	P1 RX CNT PARITY ERR	(RSV)	P1 RX SEQ PARITY ERR
74	FDTM::COMMCHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
75	FDTM::COMMCHK2CST0							
	(RSV)	(RSV)	80ns TIMER CNT PARITY ERR	60ns TIMER CNT PARITY ERR	(RSV)	ARB0 SEQ PARITY ERR	ARB1 SEQ PARITY ERR	ARB CMP ERR
76	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
77	FDTM::CBEN							
	C Path#00 ENABLE	C Path#01 ENABLE	C Path#02 ENABLE	C Path#03 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
78	FDTM::CBEN							
	C Path#10 ENABLE	C Path#11 ENABLE	C Path#12 ENABLE	C Path#13 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
79	FDTA::PKID							
	(RSV)	(RSV)	(RSV)	(RSV)	PKID#			
7A	FDTA::MONI							
	MPID#				LSI REV.			
7B	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7C	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7D	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7E	Micro Information							
	Error Devided Result Code							
7F	Micro Information							
	CHK2 Detected Counter (Low)							

Copyright ©2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(8) Byte28 = 91 (1/4)

	0	1	2	3	4	5	6	7
40		FORMAT NO.						
		x‘12’						
41		LPA::PnICNTL						
	(RSV)	(RSV)	LPDB INT ENABLE	CHK2A INT ENABLE 4	CHK2A INT ENABLE 3	CHK2A INT ENABLE 2	CHK2A INT ENABLE 1	CHK2A INT ENABLE 0
42		LPA::PnICNTL						
	PLDB31-28 ENABLE	PLDB27-24 ENABLE	PLDB23-20 ENABLE	PLDB19-16 ENABLE	OTHER INT ENABLE	PFA XFR END INT ENABLE	LPA XFR END INT ENABLE	PLDB INT ENABLE
43		LPA::PnISTAT						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	CHK2A ERR 4
44		LPA::PnISTAT						
	CHK2A ERR 3	CHK2A ERR 2	CHK2A ERR 1	CHK2A ERR 0	OTHER INT (960RD FAULT)	PFA XFR END	LPA XFR END	PLDB
45		LPA::PnLCK2A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
46		LPA::PnLCK2A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
47		LPA::PnLCK2A						
	(RSV)	PCI MASTER READ PARITY ERR	PCI MASTER PERR IN	PCI MASTER PERR OUT	(RSV)	PCI TARGET READ PARITY ERR	PCI TARGET PERR IN	PCI TARGET PERR OUT
48		LPA::PnLCK2A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	LBUS TIME OVER	LBUS READ PARITY ERR	LBUS WRITE PARITY ERR
49		LPA::PnCSTA						
	DETECTED PARITY ERR	DETECTED SYSTEM ERR	RECEIVED MASTER ABORT	RECIVED TARGET ABORT	(RSV)	DEVSEL TIMING 01:medium		DATA PARITY REPORT
4A		LPA::PnCSTA						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4B		LPA::PnCCMD						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4C		LPA::PnCCMD						
	(RSV)	ENABLE PARITY RESPONSE	(RSV)	(RSV)	(RSV)	ENABLE BUS MASTER	ENABLE MEMORY SPACE	ENABLE I/O SPACE
4D		LPA::PnPACNF						
		PCI CNF ADDRESS (BYTE0)						
4E		LPA::PnPACNF						
		PCI CNF ADDRESS (BYTE1)						
4F		LPA::PnPACNF						
		PCI CNF ADDRESS (BYTE2)						

Copyright ©2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(8) Byte28 = 91 (2/4)

	0	1	2	3	4	5	6	7
50	LPA::PnPACNF							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	CONFIGURATION TYPE '00':TYPE0 '01':TYPE1	
51	LPA::PnPAIO							
	PCI I/O ADDRESS (BYTE0)							
52	LPA::PnPAIO							
	PCI I/O ADDRESS (BYTE1)							
53	LPA::PnPAIO							
	PCI I/O ADDRESS (BYTE2)							
54	LPA::PnPAIO							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
55	LPA::PnPAMEM							
	PCI MEMORY ADDRESS (BYTE0)							
56	LPA::PnPAMEM							
	PCI MEMORY ADDRESS (BYTE1)							
57	LPA::PnPAMEM							
	PCI MEMORY ADDRESS (BYTE2)							
58	LPA::PnPAMEM							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
59	LPA::PnPAXFR							
	PCI XFR ADDRESS (BYTE0)							
5A	LPA::PnPAXFR							
	PCI XFR ADDRESS (BYTE1)							
5B	LPA::PnPAXFR							
	PCI XFR ADDRESS (BYTE2)							
5C	LPA::PnPAXFR							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5D	LPA::PnACTRL1							
	XFR READ COMMAND				XFR WRITE COMMAND			
5E	LPA::PnACTRL1							
	MEMORY READ COMMAND				MEMORY WRITE COMMAND			
5F	LPA::PnACTRL1							
	I/O READ COMMAND				I/O WRITE COMMAND			

Copyright ©2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(8) Byte28 = 91 (3/4)

	0	1	2	3	4	5	6	7
60	LPA::PnACTRL1							
	CONFIGURATION READ COMMAND				CONFIGURATION WRITE COMMAND			
61	FDTM::PCICHK2A							
	MWB8B PARITY ERR	MWB4B PARITY ERR	MWB8B PARITY GEN CHK ERR	MWB4B PARITY GEN CHK ERR	MRB0 PARITY ERR	MRB1 PARITY ERR	(RSV)	PCI IN PARITY ERR
62	FDTM::PCICHK2A							
	(RSV)	(RSV)	PCI ADR PARITY ERR	PCI ADR PARITY GEN CHK ERR	(RSV)	(RSV)	(RSV)	PCI IN SERR
63	FDTM::PCICHK2A							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
64	FDTM::PCICHK2A							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
65	FDTM::PCICHK2B0							
	DBF0 B0 PARITY ERR	DBF0 B1 PARITY ERR	DBF0 B2 PARITY ERR	DBF0 B3 PARITY ERR	DBF0 B4 PARITY ERR	DBF0 B5 PARITY ERR	DBF0 B6 PARITY ERR	DBF0 B7 PARITY ERR
66	FDTM::PCICHK2B0							
	DBF1 B0 PARITY ERR	DBF1 B1 PARITY ERR	DBF1 B2 PARITY ERR	DBF1 B3 PARITY ERR	DBF1 B4 PARITY ERR	DBF1 B5 PARITY ERR	DBF1 B6 PARITY ERR	DBF1 B7 PARITY ERR
67	FDTM::PCICHK2B0							
	DBF IN PARITY ERR 00	DBF IN PARITY ERR 01	DBF IN PARITY ERR 10	DBF IN PARITY ERR 11	(RSV)	(RSV)	(RSV)	(RSV)
68	FDTM::PCICHK2B0							
	XBF B0 PARITY ERR	XBF B1 PARITY ERR	XBF B2 PARITY ERR	XBF B3 PARITY ERR	(RSV)	(RSV)	(RSV)	XBF IN PARITY ERR
69	FDTM::PCICHK2B1							
	PCI SEQ PARITY ERR	WTBDF SEQ PARITY ERR	WTXBF SEQ PARITY ERR	RDBDF SEQ PARITY ERR	(RSV)	(RSV)	XWB WPTR PARITY ERR	XWB SPTR PARITY ERR
6A	FDTM::PCICHK2B1							
	HWB WPTR PARITY ERR	HWB SPTR PARITY ERR	HRB WPTR PARITY ERR	HRB SPTR PARITY ERR	DLRC CMP ERR	DLRC PARITY ERR	(RSV)	WDLRC PARITY ERR
6B	FDTM::PCICHK2B1							
	HWB PARITY ERR 00	HWB PARITY ERR 01	HWB PARITY ERR 10	HWB PARITY ERR 11	HRB PARITY ERR 00	HRB PARITY ERR 01	HRB PARITY ERR 10	HRB PARITY ERR 11
6C	FDTM::PCICHK2B1							
	XWB0 PARITY ERR	XWB1 PARITY ERR	MRB0 PARITY ERR	MRB1 PARITY ERR	DWA XAD PARITY ERR	PCI XAD PARITY ERR	DBFW ADRCNT PARITY ERR	DBFR ADRCNT PARITY ERR
6D	FDTM::PCICHK2B2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6E	FDTM::PCICHK2B2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6F	FDTM::PCICHK2B2							
	(RSV)	(RSV)	(RSV)	PCI OVER RUN ERR	(RSV)	(RSV)	DWA CMP ERR	DRA CMP ERR

Copyright ©2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(8) Byte28 = 91 (4/4)

	0	1	2	3	4	5	6	7
70	FDTM::PCICHK2B2							
	(RSV)	(RSV)	(RSV)	XFC MODE ERR	ACC WIDTH ERR	STADR ACC ERR	DBF ACC ERR	XBF ACC ERR
71	FDTM::COMMCHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
72	FDTM::COMMCHK2CST0							
	(RSV)	(RSV)	80ns TIMER CNT PARITY ERR	60ns TIMER CNT PARITY ERR	(RSV)	ARB0 SEQ PARITY ERR	ARB1 SEQ PARITY ERR	ARB CMP ERR
73	FDTM::HCMD							
	CACHE Transfer Command (BYTE0)							
74	FDTM::HCMD							
	CACHE Transfer Command (BYTE1)							
75	FDTM::HCMD							
	CACHE Transfer Command (BYTE2)							
76	FDTM::HCMD2							
	CACHE Transfer Command 2 (BYTE0)							
77	FDTM::HCMD2							
	CACHE Transfer Command 2 (BYTE1)							
78	FDTM::HCMD2							
	CACHE Transfer Command 2 (BYTE2)							
79	FDTM::CBEN							
	C Path#00 ENABLE	C Path#01 ENABLE	C Path#02 ENABLE	C Path#03 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
7A	FDTM::CBEN							
	C Path#10 ENABLE	C Path#11 ENABLE	C Path#12 ENABLE	C Path#13 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
7B	FDTA::PKID							
	(RSV)	(RSV)	(RSV)	(RSV)	PKID#			
7C	FDTA::MONI							
	MPID#				LSI REV.			
7D	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7E	Micro Information							
	Error Devided Result Code							
7F	Micro Information							
	CHK2 Detected Counter (Low)							

Copyright ©2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(9) Byte28 = 92 or 94 or 96 (1/4)

	0	1	2	3	4	5	6	7
40		FORMAT NO.						
		x‘13’						
41		LPA::PnICNTL						
	(RSV)	(RSV)	LPDB INT ENABLE	CHK2A INT ENABLE 4	CHK2A INT ENABLE 3	CHK2A INT ENABLE 2	CHK2A INT ENABLE 1	CHK2A INT ENABLE 0
42		LPA::PnICNTL						
	PLDB31-28 ENABLE	PLDB27-24 ENABLE	PLDB23-20 ENABLE	PLDB19-16 ENABLE	OTHER INT ENABLE	PFA XFR END INT ENABLE	LPA XFR END INT ENABLE	PLDB INT ENABLE
43		LPA::PnISTAT						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	CHK2A ERR 4
44		LPA::PnISTAT						
	CHK2A ERR 3	CHK2A ERR 2	CHK2A ERR 1	CHK2A ERR 0	OTHER INT (960RD FAULT)	PFA XFR END	LPA XFR END	PLDB
45		FDTM::PMACHK2BST0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
46		FDTM::PMACHK2BST0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
47		FDTM::PMACHK2CST0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
48		FDTM::PMACHK2CST0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
49		FDTM::PMACHK2CST0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4A		FDTM::PMACHK2CST0						
	HSN CMD LOAD PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4B		FDTM::PMACHK2CST1						
	HSN RD ADR CNT PARTY ERR	HSN WT ADR CNT PARTY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4C		FDTM::PMACHK2CST1						
	PWB LRC PARTY ERR	PWB LRC PARTY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4D		FDTM::PMACHK2CST1						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	PMA TIME OUT
4E		FDTM::PMACHK2CST2						
	TX FLRC ERR	TX FLRC PARITY ERR	RX FLRC PARITY ERR	RX FLRC PARITY ERR	PBF0 PARITY ERR	PBF1 PARITY ERR	PBF2 PARITY ERR	PBF3 PARITY ERR
4F		FDTM::PMACHK2CST2						
	(RSV)	(RSV)	(RSV)	(RSV)	PMA ACCMD ERR	XFC MODE ERR	RAID MODE ERR	BLK MODE ACSERR

Copyright ©2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(9) Byte28 = 92 or 94 or 96 (2/4)

	0	1	2	3	4	5	6	7
50	FDTM::PMACHK2CST2							
	RD DT END-CODE ERR0	RD DT END-CODE ERR1	RD DT END-CODE ERR2	RD DT END-CODE ERR3	TX FLRC 0 PADDING ERR	RX FLRC 0 PADDING ERR	RD DT INV-PLRC ERR0	RD DT INV-PLRC ERR1
51	FDTM::PMACHK2CST2							
	HSN PBF IN PARITY ERR	(RSV)	(RSV)	(RSV)	PMA TIMER PARITY ERR	(RSV)	PMA ARB SEQ PARITY ERR	PMA SEQ PARITY ERR
52	FDTM::H0CHK2BST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 DBF PARITY ERR
53	FDTM::H0CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 PWB0 PARITY ERR
54	FDTM::H0CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 PWB1 PARITY ERR
55	FDTM::H0CHK2BST2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 SNB0 PARITY ERR	P0 SNB1 PARITY ERR
56	FDTM::H0CHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 TJ1 PARITY ERR	P0 TJ2 PARITY ERR
57	FDTM::H0CHK2CST0							
	P0 TX1 TIMER0 PARITY ERR	(RSV)	(RSV)	(RSV)	P0 TX1 PTR PARITY ERR	P0 TX1 CNT PARITY ERR	(RSV)	P0 TX1 SEQ PARITY ERR
58	FDTM::H0CHK2CST1							
	P0 TX2 TIMER0 PARITY ERR	P0 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P0 TX1 PTR PARITY ERR	(RSV)	(RSV)	P0 TX1 SEQ PARITY ERR
59	FDTM::H0CHK2CST2							
	(RSV)	(RSV)	P0 PRBPTR CMP ERR	P0 PRBPTR PARITY ERR	P0 PRBPTR 0 CMP ERR	P0 PRBPTR 1 CMP ERR	P0 PRBPTR 0 PARITY ERR	P0 PRBPTR 1 PARITY ERR
5A	FDTM::H0CHK2CST2							
	P0 RX TIMER0 PARITY ERR	P0 RX TIMER1 PARITY ERR	(RSV)	(RSV)	P0 RX PTR PARITY ERR	P0 RX CNT PARITY ERR	(RSV)	P0 RX SEQ PARITY ERR
5B	FDTM::H1CHK2BST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 DBF PARITY ERR
5C	FDTM::H1CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 PWB0 PARITY ERR
5D	FDTM::H1CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 PWB1 PARITY ERR
5E	FDTM::H1CHK2BST2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 SNB0 PARITY ERR	P1 SNB1 PARITY ERR
5F	FDTM::H1CHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 TJ1 PARITY ERR	P1 TJ2 PARITY ERR

Copyright ©2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(9) Byte28 = 92 or 94 or 96 (3/4)

	0	1	2	3	4	5	6	7
60	FDTM::H1CHK2CST0							
	P1 TX2 TIMER0 PARITY ERR	P1 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P1 TX1 PTR PARITY ERR	(RSV)	(RSV)	P1 TX1 SEQ PARITY ERR
61	FDTM::H1CHK2CST1							
	P1 TX2 TIMER0 PARITY ERR	P1 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P1 TX1 PTR PARITY ERR	(RSV)	(RSV)	P1 TX1 SEQ PARITY ERR
62	FDTM::H1CHK2CST2							
	(RSV)	(RSV)	P1 PRBPTR CMP ERR	P1 PRBPTR PARITY ERR	P1 PRBPTR 0 CMP ERR	P1 PRBPTR 1 CMP ERR	P1 PRBPTR 0 PARITY ERR	P1 PRBPTR 1 PARITY ERR
63	FDTM::H1CHK2CST2							
	P1 TX TIMER0 PARITY ERR	P1 TX TIMER1 PARITY ERR	(RSV)	(RSV)	P1 TX PTR PARITY ERR	P1 TX CNT PARITY ERR	(RSV)	P1 TX SEQ PARITY ERR
64	FDTM::HADR1UCNT							
	Slave 1 CACHE Transfer Address (BYTE0)							
65	FDTM::HADR1LCNT							
	Slave 1 CACHE Transfer Address (BYTE1)							
66	FDTM::HADR1LCNT							
	Slave 1 CACHE Transfer Address (BYTE2)							
67	FDTM::HADR1LCNT							
	Slave 1 CACHE Transfer Address (BYTE3)							
68	FDTM::HADR1LCNT							
	Slave 1 CACHE Transfer Address (BYTE4)							
69	FDTM::HADR2UCNT							
	Slave 2 CACHE Transfer Address (BYTE0)							
6A	FDTM::HADR2LCNT							
	Slave 2 CACHE Transfer Address (BYTE1)							
6B	FDTM::HADR2LCNT							
	Slave 2 CACHE Transfer Address (BYTE2)							
6C	FDTM::HADR2LCNT							
	Slave 2 CACHE Transfer Address (BYTE3)							
6D	FDTM::HADR2LCNT							
	Slave 2 CACHE Transfer Address (BYTE4)							
6E	FDTM::HCMD							
	CACHE Transfer Command (BYTE0)							
6F	FDTM::HCMD							
	CACHE Transfer Command (BYTE1)							

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(9) Byte28 = 92 or 94 or 96 (4/4)

	0	1	2	3	4	5	6	7
70	FDTM::HCMD CACHE Transfer Command (BYTE2)							
71	FDTM::HCMD2 CACHE Transfer Command 2 (BYTE0)							
72	FDTM::HCMD2 CACHE Transfer Command 2 (BYTE1)							
73	FDTM::HCMD2 CACHE Transfer Command 2 (BYTE2)							
74	Reserved (RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
75	Reserved (RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
76	Reserved (RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
77	FDTM::CBEN C Path#00 ENABLE	C Path#01 ENABLE	C Path#02 ENABLE	C Path#03 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
78	FDTM::CBEN C Path#10 ENABLE	C Path#11 ENABLE	C Path#12 ENABLE	C Path#13 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
79	FDTA::PKID (RSV)	(RSV)	(RSV)	(RSV)	PKID#			
7A	FDTA::MONI MPID#				LSI REV.			
7B	Reserved (RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7C	Reserved (RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7D	Reserved (RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7E	Micro Information Error Devided Result Code							
7F	Micro Information CHK2 Detected Counter (Low)							

Copyright ©2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(10) Byte28 = 20 or 3F (1/4)

	0	1	2	3	4	5	6	7
40		CHA::CK2ASR0						
	PDBF PLRC ERR	SLRC ERR	LA ERR	CBUF DT PARITY ERR	SEARCH ERR	SEARCH DT ERR	WRBF INPUT DT PARITY ERR	BYTE ALIGNMENT ERR
41		CHA::CK2AST0						
	LCM OUTPUT DT PARITY ERR	Not used	LA PARITY ERR	RDBF OUTPUT DT PARITY ERR	PARITY ERR	Not used	Not used	Not used
42		CHA::CK2AST2						
	PLIST XFR SEQ PARITY ERR	XR SET XFR SEQ PARITY ERR	PLIST OUT PARITY ERR	PLIST IN PARITY ERR	CBP CNT PARITY ERR	CBUF CKDDL PARITY ERR	TBP PARITY ERR	XFR MODE ERR
43		CHA::CK2AST2						
	Not used	LCM CKDDL PARITY ERR	Not used	Not used	Not used	Not used	Not used	Not used
44		CHA::CK2AST1						
	FBADL PARITY ERR	SGOP PARITY ERR	PFC PARITY ERR	WRBF CNT PARITY ERR	RDBF CNT PARITY ERR	PACKET SEQ PARITY ERR	UNMATCH ERR0	UNMATCH ERR1
45		CHA::CK2AST1						
	SOP PARITY ERR	BOP PARITY ERR	CKDFBA CNG CKDDL PARITY ERR	CKDFBA CNG SEQ PARITY ERR	Not used	Not used	Not used	Not used
46		CHA::CK2AST1						
	SLAVE1 NEXTSEG ADR PARITY ERR	SLAVE1 HSN ADR PARITY ERR	SLAVE2 NEXTSEG ADR PARITY ERR	SLAVE2 HSN ADR PARITY ERR	Not used	Not used	Not used	Not used
47		CHA::CHK2ASTS						
	WRBF RD ADR PNT PARITY ERR	RDBF WT ADR PNT PARITY ERR	SC CNT PARITY ERR	LOS CNT PARITY ERR	HARD TIMER PARITY ERR	WRBF PLRC ERR	HSN ADR PARITY ERR	WRBF OUT DT PARITY ERR
48		CHA::CHK2ASTS						
	P0 Receive PARITY ERR	P1 Receive PARITY ERR	X0 Receive PARITY ERR	X1 Receive PARITY ERR	ADRM PARITY ERR	ADRS PARITY ERR	ADRP PARITY ERR	CMD PARITY ERR
49		CHA::CHK2ASTS						
	XFR CNT PARITY ERR	ILPRM0	ILPRM1	ILPRM2	ILPRM3	ILPRM4	ILPRM5	ILPRM6
4A		CMF::CK2AST3						
	CRC ERR	CCNT PARITY ERR	SBX BUF OUT PNT PARITY ERR	SBX BUF IN PNT PARITY ERR	FBX BUF OUT PNT PARITY ERR	FBX BUF IN PNT PARITY ERR	FR BUF OUT PNT PARITY ERR	FR BUF IN PNT PARITY ERR
4B		CMF::CK2AST3						
	DIB ZERO CHK	DCNT PARITY ERR	SEQ PARITY ERR	WCC CNT PARITY ERR	DIB4 CNT PARITY ERR	DIBC CNT PARITY ERR	FBX/SBX BUF LRC ERR	Not used
4C		CMF::CK2AST3						
	DXBF STR CNT PARITY ERR	DXBF FET CNT PARITY ERR	RCCNT PARITY ERR	CADR PARITY ERR	DXOP PARITY ERR	DXIP PARITY ERR	CCNT DEC ERR	Not used
4D		CMF::DXBFERR0						
	DSEQ PARITY ERR	DTPCHK ERR	CAC RD SEL PARITY ERR	CAC RD ADR PARITY ERR	CAC RD CNT PARITY ERR	CAC RD DT PARITY ERR	Not used	Not used
4E		CMF::DXBFERR0						
	Not used	Not used	CAC WT SEL PARITY ERR	CAC WT ADR PARITY ERR	CAC WT CNT PARITY ERR	Not used	CAC WT ECC 2Bit ERR	CAC WT ECC 1Bit ERR
4F		CHA::CBP						
		Data Transfer Start Address						

Copyright ©2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(10) Byte28 = 20 or 3F (2/4)

	0	1	2	3	4	5	6	7
50		CHA::CKDDL						
		Transfer Data Length (CKD)						
51		CHA::CKDDL						
		Transfer Data Length (CKD)						
52		CHA::FBADL						
		Transfer Data Length (FBA)						
53		CHA::FBADL						
		Transfer Data Length (FBA)						
54		CHA::MCSA00						
		Slave1 CACHE Transfer Address (BYTE0)						
55		CHA::MCSA00						
		Slave1 CACHE Transfer Address (BYTE1)						
56		CHA::MCSA01						
		Slave1 CACHE Transfer Address (BYTE2)						
57		CHA::MCSA01						
		Slave1 CACHE Transfer Address (BYTE3)						
58		CHA::SCSA00						
		Slave2 CACHE Transfer Address (BYTE0)						
59		CHA::SCSA00						
		Slave2 CACHE Transfer Address (BYTE1)						
5A		CHA::SCSA01						
		Slave2 CACHE Transfer Address (BYTE2)						
5B		CHA::SCSA01						
		Slave2 CACHE Transfer Address (BYTE3)						
5C		CHA::CSPGR						
	Slave1 REG Access Flag	Slave1 CARB Access Flag	Not used	Not used	Slave2 REG Access Flag	Slave2 CARB Access Flag	Not used	Not used
5D		CHA::PCMD1						
		CACHE Transfer Command (BYTE0)						
5E		CHA::PCMD2						
		CACHE Transfer Command (BYTE2)						
5F		CHA::LA0						
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used

Copyright ©2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(10) Byte28 = 20 or 3F (3/4)

	0	1	2	3	4	5	6	7
60	CHA::LA1							
	LA Expected Value (BYTE1)							
61	CHA::LA1							
	LA Expected Value (BYTE2)							
62	CHA::LA2							
	LA Expected Value (BYTE3)							
63	CHA::LA2							
	LA Expected Value (BYTE4)							
64	CHA::SOP							
	Subblock Offset Pointer							
65	CHA::SOP							
	Subblock Offset Pointer							
66	CHA::BOP							
	Block Offset Pointer							
67	CHA::BOP							
	Block Offset Pointer							
68	CHA::POP							
	Packet Offset Pointer							
69	CHA::POP							
	Packet Offset Pointer							
6A	CHA::SGOP							
	Segment Offset Pointer							
6B	CHA::SGOP							
	Segment Offset Pointer							
6C	CHA::LPEN							
	C PATH#00 ENABLE	C PATH#01 ENABLE	C PATH#02 ENABLE	C PATH#03 ENABLE	C PATH#10 ENABLE	C PATH#11 ENABLE	C PATH#12 ENABLE	C PATH#13 ENABLE
6D	CHA::PDC/PDS/PLIN							
	ENABLE 0: NORMAL 1: LIST XFR	PLTB FULL	PLHLD E0	PLHLD Q0	Set Parameter Memory Page Pointer (High)			
6E								
	Set Parameter Memory Page Pointer (Low)		Processed Parameter Memory Page Pointer					
6F	CHA::PFC							
	Packet From Counter (Packet Number Able to Transfer)							

Copyright ©2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(10) Byte28 = 20 or 3F (4/4)

	0	1	2	3	4	5	6	7
70	CMF::SFBA							
	ABORT FLAG0	ABORT FLAG1	Not used	Not used	Not used	Not used	Not used	Not used
71	CMF::DXOP DXBF Output address Pointer (BYTE0)							
72	CMF::DXOP DXBF Output address Pointer (BYTE1)							
73	CMF::DXOP DXBF Output address Pointer (BYTE2)							
74	CMF::CADR DXBF Current address Pointer (BYTE0)							
75	CMF::CADR DXBF Current address Pointer (BYTE1)							
76	CMF::CADR DXBF Current address Pointer (BYTE2)							
77	CMF::DXIP DXBF Input address Pointer (BYTE0)							
78	CMF::DXIP DXBF Input address Pointer (BYTE1)							
79	CMF::DXIP DXBF Input address Pointer (BYTE2)							
7A	CMF::DCTL CCNT Current Value (High)							
7B	CMF::DCTL CCNT Current Value (Low)							
7C	CMF::RCCNT RCCNT Current Value (High)							
7D	CMF::RCCNT RCCNT Current Value (Low)							
7E	CMF::DIBC DIB Byte Current Value (High)							
7F	CMF::DIBC DIB Byte Current Value (Low)							

Copyright ©2001, Hitachi, Ltd.

Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(11) Byte28 = 28 or 2F

	0	1	2	3	4	5	6	7
40	Reserved							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
41	Reserved							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
42	CMF::DXBFERR0							
	DSEQ PARITY ERR	DTPCHK ERR	PBF STR SEL PARITY ERR	PBF STR ADR PARITY ERR	PBF STR CNT PARITY ERR	PBF STR DT PARITY ERR	Not used	Not used
43	CMF::DXBFERR0							
	Not used	Not used	PBF FET SEL PARITY ERR	PBF FET ADR PARITY ERR	PBF FET CNT PARITY ERR	Not used	PBF FET ECC 2Bit ERR	PBF FET ECC 1Bit ERR
44	CMF::PADR							
	PRMBF Transfer Pointer (BYTE0)							
45	CMF::PADR							
	PRMBF Transfer Pointer (BYTE1)							
46	CMF::PADR							
	PRMBF Transfer Pointer (BYTE2)							
47	CMF::PADR							
	PRMBF Transfer Pointer (BYTE3)							
48	Not used							
	:							
7F								

Copyright ©2001, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2)

	0	1	2	3	4	5	6	7
00	Time Stamp							
|								
05								
06	Format Message							
07	P/K Type		Processer ID					
08	System Error Code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	HOST Report	SVP Report	Force Log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	PORT#		RCU#			
10	LDEV#							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV#							
15								
16	Internal SSB Log Number							
17								
18	Related Failure Log Number							
19								
1A	Related SIM Log Number							
1B								
1C	Related SSB Log Number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTRL no.	DKU Physical Device no.				
25	Cylinder Address (Low)							
26	Cylinder Address (High)				Head Address			
27	Format (x‘8’)				Message (x‘A’)			
28	SubCode							
29	Detail Information (See Following Pages.)							
|								
31								
32	Module ID							
33	Routine ID							
34	P/K ID				Message Code (x‘0’)			
35	SSID for Self Subsystem							
36	Symptom Code (x‘FF89’:LDEV Type=DKU87I / x‘EF89’: LDEV Type=DKU86I)							
37								
38	Log and Message Control (x‘00’)							
39	Program Action Control (x‘00’)							
3A	Configuration Information							
3B								
3C	Not Used							
3D	Cylinder Address							
3E								
3F	Head Address							
40	Detail Information (See Following Pages.)							
|								
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte28-31 Detail

	0	1	2	3	4	5	6	7
28	SubCode (Note 1)							
29	MMC::RCVINT							
	SYSRST Interrupt Monitor	SELRST Interrupt Monitor	CHK1A Interrupt Monitor	CHK1B Interrupt Monitor	SMP Interrupt Monitor	LAN/SIO Interrupt Monitor	CHA/DRR Interrupt Monitor	ADP/SCA0 Interrupt Monitor
2A	MMC::RCVINT							
	(RSV)	CHK3 Interrupt Monitor	(RSV)	SCA1 Interrupt Monitor	SCA2 Interrupt Monitor	SCA3 Interrupt Monitor	SCA4 Interrupt Monitor	SCA5 Interrupt Monitor
2B	FCA::INTSTS							
	CHK2E ERR Interrupt	CHK2F ERR Interrupt	CHK2G ERR Interrupt	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
2C	FCA::MODE							
	DRV→ CACHE XFR Start	CACHE→ DRV XFR Start	FSB→ CACHE XFR Start	CACHE→ FDB XFR Start	DRV→FSB XFR Start	FDB→DRV XFR Start	(RSV)	(RSV)
2D	FCA::MODE							
	Data/Parity (1: Data)	LA EX MODE	LA CHK MASK	LBA/LLRC CHK MASK	(RSV)	Subblock Length in Packet (MAX: 4)		
2E	FCA::MODE							
	DMA QUE Number for the PDEV							
2F	FCA::DMASTS							
	DMA END	(RSV)	INT5	INT4	INT3	INT2	INT1	INT0
30	FCA::DMASTS							
	CHK2E Occured	CHK2F Occured	CHK2G Occured	(RSV)	CHK2RST	ABORT	PADDING	(RSV)
31	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

(Note 1) Meaning of SubCode:

x‘10’ = QDTA reported CHK2 when writing to cache,
x‘11’ = QDTA reported CHK2 when reading from cache,
x‘20’ = FCA CHK2 when writing to cache,
x‘21’ = FCA CHK2 when reading from cache,
x‘30’ = FCA-QDTA CHK2 when writing to cache,
x‘31’ = FCA-QDTA CHK2 when reading from cache,
x‘40’ = PCI CHK2 when writing to cache,
x‘41’ = PCI CHK2 when reading from cache,
x‘60’ = PCI-FCA CHK2 when writing to cache,
x‘61’ = PCI-FCA CHK2 when reading from cache,
x‘48’ = HDD CHK2 when writing to cache,
x‘19’ = CACHE CHK2 when reading from cache,
x‘F0’ = XFR TOV when writing to cache,
x‘F1’ = XFR TOV when reading from cache

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(1) Byte28 = 10 (1/4)

	0	1	2	3	4	5	6	7
40	DRR::CD0SL1A0 Slave 1 Cache Transfer Address (BYTE0)							
41	DRR::CD0SL1A0 Slave 1 Cache Transfer Address (BYTE1)							
42	DRR::CD0SL1A1 Slave 1 Cache Transfer Address (BYTE2)							
43	DRR::CD0SL1A1 Slave 1 Cache Transfer Address (BYTE3)							
44	DRR::CD0SL1C0 Slave 1 Cache Transfer Address (BYTE4)							
45	DRR::CD0SL1C0 Slave 1 Cache Transfer Command (BYTE0)							
46	DRR::CD0SL1C1 Slave 1 Cache Transfer Command (BYTE1)							
47	DRR::CD0SL1C1 Slave 1 Cache Transfer Command (BYTE2)							
48	DRR::CD0SL2A0 Slave 2 Cache Transfer Address (BYTE0)							
49	DRR::CD0SL2A0 Slave 2 Cache Transfer Address (BYTE1)							
4A	DRR::CD0SL2A1 Slave 2 Cache Transfer Address (BYTE2)							
4B	DRR::CD0SL2A1 Slave 2 Cache Transfer Address (BYTE3)							
4C	DRR::CD0SL2C0 Slave 2 Cache Transfer Address (BYTE4)							
4D	DRR::CD0SL2C0 Slave 2 Cache Transfer Command (BYTE0)							
4E	DRR::CD0SL2C1 Slave 2 Cache Transfer Command (BYTE1)							
4F	DRR::CD0SL2C1 Slave 2 Cache Transfer Command (BYTE2)							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(1) Byte28 = 10 (2/4)

	0	1	2	3	4	5	6	7
50		DRR::D0M0DE5						
	C PATH#00 ENABLE	C PATH#01 ENABLE	C PATH#02 ENABLE	C PATH#03 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
51		DRR::D0M0DE5						
	C PATH#10 ENABLE	C PATH#11 ENABLE	C PATH#12 ENABLE	C PATH#13 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
52		DRR::D0TXM						
		D0 TX SEQ(Master)						
53		DRR::D0MODE1						
	DTN CUDG MODE	DTN SYSTEM CLK MASK	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
54		DRR::D0MODE1						
	DTN ABORT	DTN CHSN ABORT	(RSV)	(RSV)	(RSV)	(RSV)	DTN OUT DIAG	DTN CHK2 RST
55		DRR::D0ERR						
	DTN CTL ERR	P0 CTL ERR	P1 CTL ERR	DTN DT ERR	P0 DT ERR	P1 DT ERR	P0 DT CARB/CMA ERR	P0 ST1 CARB/CMA ERR
56		DRR::D0ERR						
	P0 ERR INT	P1 ERR INT	(RSV)	TIME OVER ERR	ST0 VALID	ST1 VALID	P0 USE FLAG	P1 USE FLAG
57		DRR::D0ESTA0						
	TX DT PARITY ERR	TX PD-PNT PARITY ERR	DTN SEQ ERR	DTN WT-PNT PARITY ERR	WT DT-CNT PARITY ERR	INPUT CTL-SIG PARITY ERR	INPUT-PNT PARITY ERR	RD DT CNT PARITY ERR
58		DRR::D0ESTA0						
	P0 SYNC0 PNT PARITY ERR	P0 SYNC1 PNT PARITY ERR	P0 SYNC0 CLOCK ERR	P0 SYNC1 CLOCK ERR	P0 TXX SEQ ERR	P0 TX RD-PNT PARITY ERR	P0 RX SEQ ERR	P0 TX WT-PNT PARITY ERR
59		DRR::D0ESTA1						
	P1 SYNC0 PNT PARITY ERR	P1 SYNC1 PNT PARITY ERR	P1 SYNC0 CLOCK ERR	P1 SYNC1 CLOCK ERR	P1 TXX SEQ ERR	P1 TX RD-PNT PARITY ERR	P1 RX SEQ ERR	P1 TX WT-PNT PARITY ERR
5A		DRR::D0ESTA1						
	P0 TX SEQ PARITY ERR	P1 TX SEQ PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5B		DRR::D0ESTA2						
	ST0 PLRC ERR	ST0 INV-PLRC ERR	ST0 END-CODE ERR	ST1 PLRC ERR	ST1 INV-PLRC ERR	ST1 END-CODE ERR	TRANS MODE ERR	(RSV)
5C		DRR::D0ESTA2						
	ADR/CMD PLRC ERR	ADR/CMD INV-PLRC ERR	ADR/CMD END-CODE ERR	ADR/CMD DT PARITY ERR	OUT DT00 PARITY ERR	OUT DT01 PARITY ERR	OUT DT02 PARITY ERR	OUT DT03 PARITY ERR
5D		DRR::D0ESTA3						
	OUT DT11 PARITY ERR	OUT DT11 PARITY ERR	OUT DT12 PARITY ERR	OUT DT13 PARITY ERR	OUTPUT LOOP DT0 PARITY ERR	OUTPUT LOOP DT1 PARITY ERR	OUTPUT LOOP DT2 PARITY ERR	OUTPUT LOOP DT3 PARITY ERR
5E		DRR::D0ESTA3						
	TX DT0 PARITY ERR	TX DT1 PARITY ERR	TX DT2 PARITY ERR	TX DT3 PARITY ERR	TX DT4 PARITY ERR	TX DT5 PARITY ERR	TX DT6 PARITY ERR	TX DT7 PARITY ERR
5F		DRR::D0ESTA4						
	ST1 DT0 PARITY ERR	ST1 DT1 PARITY ERR	ST1 DT2 PARITY ERR	ST1 DT3 PARITY ERR	ST1 DT4 PARITY ERR	ST1 DT5 PARITY ERR	ST1 DT6 PARITY ERR	ST1 DT7 PARITY ERR

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(1) Byte28 = 10 (3/4)

	0	1	2	3	4	5	6	7
60		DRR::D0ESTA4						
	ST1 DT0 PARITY ERR	ST1 DT1 PARITY ERR	ST1 DT2 PARITY ERR	ST1 DT3 PARITY ERR	ST1 DT4 PARITY ERR	ST1 DT5 PARITY ERR	ST1 DT6 PARITY ERR	ST1 DT7 PARITY ERR
61		DRR::D0ESTA5						
	P0 TX DT0 PARITY ERR	P0 TX DT1 PARITY ERR	P0 TX DT2 PARITY ERR	P0 TX DT3 PARITY ERR	P0 TX DT4 PARITY ERR	P0 TX DT5 PARITY ERR	P0 TX DT6 PARITY ERR	P0 TX DT7 PARITY ERR
62		DRR::D0ESTA5						
	P0 RX DT0 PARITY ERR	P0 RX DT1 PARITY ERR	P1 RX DT0 PARITY ERR	P1 RX DT1 PARITY ERR	P0 RX DT4 PARITY ERR	P0 RX DT5 PARITY ERR	P1 RX DT4 PARITY ERR	P1 RX DT5 PARITY ERR
63		DRR::D0ESTA6						
	P0 TXX INPUT DT0 PARITY ERR	P0 TXX INPUT DT1 PARITY ERR	P0 TXX OUTPUT DT0 PARITY ERR	P0 TXX OUTPUT DT1 PARITY ERR	P1 TXX INPUT DT0 PARITY ERR	P1 TXX INPUT DT1 PARITY ERR	P1 TXX OUTPUT DT0 PARITY ERR	P1 TXX OUTPUT DT1PARITY ERR
64		DRR::D0ESTA6						
	P1 TX DT0 PARITY ERR	P1 TX DT1 PARITY ERR	P1 TX DT2 PARITY ERR	P1 TX DT3 PARITY ERR	P1 TX DT4 PARITY ERR	P1 TX DT5 PARITY ERR	P1 TX DT6 PARITY ERR	P1 TX DT7 PARITY ERR
65		DRR::D0ESTA7						
	TX DT0 PARITY ERR	TX DT1 PARITY ERR	TX DT2 PARITY ERR	TX DT3 PARITY ERR	P0 RX DT6 PARITY ERR	P0 RX DT7 PARITY ERR	P1 RX DT6 PARITY ERR	P1 RX DT7 PARITY ERR
66		DRR::D0ESTA7						
	INPUT DT0 PARITY ERR	INPUT DT1 PARITY ERR	INPUT DT2 PARITY ERR	INPUT DT3 PARITY ERR	P0 ERR INT	P1 ERR INT	DT CARB/CMA ERR	ST1 CARB/CMA ERR
67		DRR::D0ESTA8						
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	(RSV)	(RSV)	(RSV)	(RSV)
68		DRR::D0ESTA8						
	ST0 VALID	ST1 VALID	(RSV)	(RSV)	P0 USE FLAG	P1 USE FLAG	(RSV)	(RSV)
69		DRR::D0ESTA9						
	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6A		DRR::D0ESTA9						
	ARB SEQ PARITY ERR (M)	ARB SEQ PARITY ERR (S)	P0 ARB CMP CHK ERR	P1 ARB CMP CHK ERR	(RSV)	(RSV)	(RSV)	(RSV)
6B		DRR::D0ESTAB						
	P0 ADR/CMD PLRC ERR	P0 DT PLRC ERR	P0 ST0 PLRC ERR	P0 ST1 PLRC ERR	P0 ADR/CMD INV-PLRC ERR	P0 DT INV-PLRC ERR	P0 ST0 INV-PLRC ERR	P0 ST1 INV-PLRC ERR
6C		DRR::D0ESTAB						
	P0 ADR/CMD END-CODE ERR	P0 DT END-CODE ERR	P0 ST0 END-CODE ERR	P0 ST1 END-CODE ERR	P0 SLRC CHECK ERR	P0 SLRC CAL DT ERR	P0 SLRC RD DT ERR	P0 SBLK DCNT ERR
6D		DRR::D0ESTAC						
	P1 ADR/CMD PLRC ERR	P1 DT PLRC ERR	P1 ST0 PLRC ERR	P1 ST1 PLRC ERR	P1 ADR/CMD INV-PLRC ERR	P1 DT INV-PLRC ERR	P1 ST0 INV-PLRC ERR	P1 ST1 INV-PLRC ERR
6E		DRR::D0ESTAC						
	P1 ADR/CMD END-CODE ERR	P1 DT END-CODE ERR	P1 ST0 END-CODE ERR	P1 ST1 END-CODE ERR	P1 SLRC CHECK ERR	P1 SLRC CAL DT ERR	P1 SLRC RD DT ERR	P1 SBLK DCNT ERR
6F		FCA::BPMWT21						
		BPM0C Value When Writing to Cache						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(1) Byte28 = 10 (4/4)

	0	1	2	3	4	5	6	7
70	FCA::BPMWT21							
	BPM0C Value When Writing to Cache							
71	FCA::C2LA14M							
	CC2 LA Value (BYTE1)							
72	FCA::C2LA14M							
	CC2 LA Value (BYTE2)							
73	FCA::C2LA14M							
	CC2 LA Value (BYTE3)							
74	FCA::C2LA14M							
	CC2 LA Value (BYTE4)							
75	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
76	Micro Information							
	CDEV#							
77	Micro Information							
	RDEV#							
78	Micro Information							
	RDEV#							
79	Micro Information							
	SCSI Command							
7A	Micro Information							
	LBA#(byte0)							
7B	Micro Information							
	LBA#(byte1)							
7C	Micro Information							
	LBA#(byte2)							
7D	Micro Information							
	LBA#(byte3)							
7E	Micro Information							
	Error Devided Result Code							
7F	Micro Information							
	CHK2 Detected Counter (Low)							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(2) Byte28 = 11 (1/4)

	0	1	2	3	4	5	6	7
40	DRR::CD0SL1A0 Slave 1 Cache Transfer Address (BYTE0)							
41	DRR::CD0SL1A0 Slave 1 Cache Transfer Address (BYTE1)							
42	DRR::CD0SL1A1 Slave 1 Cache Transfer Address (BYTE2)							
43	DRR::CD0SL1A1 Slave 1 Cache Transfer Address (BYTE3)							
44	DRR::CD0SL1C0 Slave 1 Cache Transfer Address (BYTE4)							
45	DRR::CD0SL1C0 Slave 1 Cache Transfer Command (BYTE0)							
46	DRR::CD0SL1C1 Slave 1 Cache Transfer Command (BYTE1)							
47	DRR::CD0SL1C1 Slave 1 Cache Transfer Command (BYTE2)							
48	DRR::CD0SL2A0 Slave 2 Cache Transfer Address (BYTE0)							
49	DRR::CD0SL2A0 Slave 2 Cache Transfer Address (BYTE1)							
4A	DRR::CD0SL2A1 Slave 2 Cache Transfer Address (BYTE2)							
4B	DRR::CD0SL2A1 Slave 2 Cache Transfer Address (BYTE3)							
4C	DRR::CD0SL2C0 Slave 2 Cache Transfer Address (BYTE4)							
4D	DRR::CD0SL2C0 Slave 2 Cache Transfer Command (BYTE0)							
4E	DRR::CD0SL2C1 Slave 2 Cache Transfer Command (BYTE1)							
4F	DRR::CD0SL2C1 Slave 2 Cache Transfer Command (BYTE2)							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(2) Byte28 = 11 (2/4)

	0	1	2	3	4	5	6	7
50		DRR::D0M0DE5						
	C PATH#00 ENABLE	C PATH#01 ENABLE	C PATH#02 ENABLE	C PATH#03 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
51		DRR::D0M0DE5						
	C PATH#10 ENABLE	C PATH#11 ENABLE	C PATH#12 ENABLE	C PATH#13 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
52		DRR::D0TXM						
		D0 TX SEQ(Master)						
53		DRR::D0MODE1						
	DTN CUDG MODE	DTN SYSTEM CLK MASK	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
54		DRR::D0MODE1						
	DTN ABORT	DTN CHSN ABORT	(RSV)	(RSV)	(RSV)	(RSV)	DTN OUT DIAG	DTN CHK2 RST
55		DRR::D0ERR						
	DTN CTL ERR	P0 CTL ERR	P1 CTL ERR	DTN DT ERR	P0 DT ERR	P1 DT ERR	P0 DT CARB/CMA ERR	P0 ST1 CARB/CMA ERR
56		DRR::D0ERR						
	P0 ERR INT	P1 ERR INT	(RSV)	TIME OVER ERR	ST0 VALID	ST1 VALID	P0 USE FLAG	P1 USE FLAG
57		DRR::D0ESTA0						
	TX DT PARITY ERR	TX PD-PNT PARITY ERR	DTN SEQ ERR	DTN WT-PNT PARITY ERR	WT DT-CNT PARITY ERR	INPUT CTL-SIG PARITY ERR	INPUT-PNT PARITY ERR	RD DT CNT PARITY ERR
58		DRR::D0ESTA0						
	P0 SYNC0 PNT PARITY ERR	P0 SYNC1 PNT PARITY ERR	P0 SYNC0 CLOCK ERR	P0 SYNC1 CLOCK ERR	P0 TXX SEQ ERR	P0 TX RD-PNT PARITY ERR	P0 RX SEQ ERR	P0 TX WT-PNT PARITY ERR
59		DRR::D0ESTA1						
	P1 SYNC0 PNT PARITY ERR	P1 SYNC1 PNT PARITY ERR	P1 SYNC0 CLOCK ERR	P1 SYNC1 CLOCK ERR	P1 TXX SEQ ERR	P1 TX RD-PNT PARITY ERR	P1 RX SEQ ERR	P1 TX WT-PNT PARITY ERR
5A		DRR::D0ESTA1						
	P0 TX SEQ PARITY ERR	P1 TX SEQ PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5B		DRR::D0ESTA2						
	ST0 PLRC ERR	ST0 INV-PLRC ERR	ST0 END-CODE ERR	ST1 PLRC ERR	ST1 INV-PLRC ERR	ST1 END-CODE ERR	TRANS MODE ERR	(RSV)
5C		DRR::D0ESTA2						
	ADR/CMD PLRC ERR	ADR/CMD INV-PLRC ERR	ADR/CMD END-CODE ERR	ADR/CMD DT PARITY ERR	OUT DT00 PARITY ERR	OUT DT01 PARITY ERR	OUT DT02 PARITY ERR	OUT DT03 PARITY ERR
5D		DRR::D0ESTA3						
	OUT DT11 PARITY ERR	OUT DT11 PARITY ERR	OUT DT12 PARITY ERR	OUT DT13 PARITY ERR	OUTPUT LOOP DT0 PARITY ERR	OUTPUT LOOP DT1 PARITY ERR	OUTPUT LOOP DT2 PARITY ERR	OUTPUT LOOP DT3 PARITY ERR
5E		DRR::D0ESTA3						
	TX DT0 PARITY ERR	TX DT1 PARITY ERR	TX DT2 PARITY ERR	TX DT3 PARITY ERR	TX DT4 PARITY ERR	TX DT5 PARITY ERR	TX DT6 PARITY ERR	TX DT7 PARITY ERR
5F		DRR::D0ESTA4						
	ST1 DT0 PARITY ERR	ST1 DT1 PARITY ERR	ST1 DT2 PARITY ERR	ST1 DT3 PARITY ERR	ST1 DT4 PARITY ERR	ST1 DT5 PARITY ERR	ST1 DT6 PARITY ERR	ST1 DT7 PARITY ERR

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(2) Byte28 = 11 (3/4)

	0	1	2	3	4	5	6	7
60		DRR::D0ESTA4						
	ST1 DT0 PARITY ERR	ST1 DT1 PARITY ERR	ST1 DT2 PARITY ERR	ST1 DT3 PARITY ERR	ST1 DT4 PARITY ERR	ST1 DT5 PARITY ERR	ST1 DT6 PARITY ERR	ST1 DT7 PARITY ERR
61		DRR::D0ESTA5						
	P0 TX DT0 PARITY ERR	P0 TX DT1 PARITY ERR	P0 TX DT2 PARITY ERR	P0 TX DT3 PARITY ERR	P0 TX DT4 PARITY ERR	P0 TX DT5 PARITY ERR	P0 TX DT6 PARITY ERR	P0 TX DT7 PARITY ERR
62		DRR::D0ESTA5						
	P0 RX DT0 PARITY ERR	P0 RX DT1 PARITY ERR	P1 RX DT0 PARITY ERR	P1 RX DT1 PARITY ERR	P0 RX DT4 PARITY ERR	P0 RX DT5 PARITY ERR	P1 RX DT4 PARITY ERR	P1 RX DT5 PARITY ERR
63		DRR::D0ESTA6						
	P0 TXX INPUT DT0 PARITY ERR	P0 TXX INPUT DT1 PARITY ERR	P0 TXX OUTPUT DT0 PARITY ERR	P0 TXX OUTPUT DT1 PARITY ERR	P1 TXX INPUT DT0 PARITY ERR	P1 TXX INPUT DT1 PARITY ERR	P1 TXX OUTPUT DT0 PARITY ERR	P1 TXX OUTPUT DT1PARITY ERR
64		DRR::D0ESTA6						
	P1 TX DT0 PARITY ERR	P1 TX DT1 PARITY ERR	P1 TX DT2 PARITY ERR	P1 TX DT3 PARITY ERR	P1 TX DT4 PARITY ERR	P1 TX DT5 PARITY ERR	P1 TX DT6 PARITY ERR	P1 TX DT7 PARITY ERR
65		DRR::D0ESTA7						
	TX DT0 PARITY ERR	TX DT1 PARITY ERR	TX DT2 PARITY ERR	TX DT3 PARITY ERR	P0 RX DT6 PARITY ERR	P0 RX DT7 PARITY ERR	P1 RX DT6 PARITY ERR	P1 RX DT7 PARITY ERR
66		DRR::D0ESTA7						
	INPUT DT0 PARITY ERR	INPUT DT1 PARITY ERR	INPUT DT2 PARITY ERR	INPUT DT3 PARITY ERR	P0 ERR INT	P1 ERR INT	DT CARB/CMA ERR	ST1 CARB/CMA ERR
67		DRR::D0ESTA8						
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	(RSV)	(RSV)	(RSV)	(RSV)
68		DRR::D0ESTA8						
	ST0 VALID	ST1 VALID	(RSV)	(RSV)	P0 USE FLAG	P1 USE FLAG	(RSV)	(RSV)
69		DRR::D0ESTA9						
	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6A		DRR::D0ESTA9						
	ARB SEQ PARITY ERR (M)	ARB SEQ PARITY ERR (S)	P0 ARB CMP CHK ERR	P1 ARB CMP CHK ERR	(RSV)	(RSV)	(RSV)	(RSV)
6B		DRR::D0ESTAB						
	P0 ADR/CMD PLRC ERR	P0 DT PLRC ERR	P0 ST0 PLRC ERR	P0 ST1 PLRC ERR	P0 ADR/CMD INV-PLRC ERR	P0 DT INV-PLRC ERR	P0 ST0 INV-PLRC ERR	P0 ST1 INV-PLRC ERR
6C		DRR::D0ESTAB						
	P0 ADR/CMD END-CODE ERR	P0 DT END-CODE ERR	P0 ST0 END-CODE ERR	P0 ST1 END-CODE ERR	P0 SLRC CHECK ERR	P0 SLRC CAL DT ERR	P0 SLRC RD DT ERR	P0 SBLK DCNT ERR
6D		DRR::D0ESTAC						
	P1 ADR/CMD PLRC ERR	P1 DT PLRC ERR	P1 ST0 PLRC ERR	P1 ST1 PLRC ERR	P1 ADR/CMD INV-PLRC ERR	P1 DT INV-PLRC ERR	P1 ST0 INV-PLRC ERR	P1 ST1 INV-PLRC ERR
6E		DRR::D0ESTAC						
	P1 ADR/CMD END-CODE ERR	P1 DT END-CODE ERR	P1 ST0 END-CODE ERR	P1 ST1 END-CODE ERR	P1 SLRC CHECK ERR	P1 SLRC CAL DT ERR	P1 SLRC RD DT ERR	P1 SBLK DCNT ERR
6F		FCA::BPMRD21						
		BPM0C Value When Reading to Cache						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(2) Byte28 = 11 (4/4)

	0	1	2	3	4	5	6	7
70		FCA::BPMWT21						
		BPM0C Value When Reading to Cache						
71		FCA::C3LA14M						
		CC3 LA Value (BYTE1)						
72		FCA::C3LA14M						
		CC3 LA Value (BYTE2)						
73		FCA::C3LA14M						
		CC3 LA Value (BYTE3)						
74		FCA::C3LA14M						
		CC3 LA Value (BYTE4)						
75		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
76		Micro Information						
		CDEV#						
77		Micro Information						
		RDEV#						
78		Micro Information						
		RDEV#						
79		Micro Information						
		SCSI Command						
7A		Micro Information						
		LBA# (BYTE0)						
7B		Micro Information						
		LBA# (BYTE1)						
7C		Micro Information						
		LBA# (BYTE2)						
7D		Micro Information						
		LBA# (BYTE3)						
7E		Micro Information						
		Error Devided Result Code						
7F		Micro Information						
		CHK2 Detected Counter (Low)						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(3) Byte28 = 20, F0 (1/4)

	0	1	2	3	4	5	6	7
40		FCA::CHK2E30						
	(RSV)	SEQ15 PARITY ERR	SEQ00 PARITY ERR	SEQ20 PARITY ERR	SEQ25 PARITY ERR	SEQ27 PARITY ERR	SEQ28 PARITY ERR	SEQ30 PARITY ERR
41		FCA::CHK2E30						
	SEQ31 PARITY ERR	SEQ33 PARITY ERR	SEQ34 PARITY ERR	SEQ40 PARITY ERR	SEQ45 PARITY ERR	SEQ63 PARITY ERR	SEQ70 PARITY ERR	SEQ72 PARITY ERR
42		FCA::CHK2E30						
	SEQ90 PARITY ERR	SEQ92 PARITY ERR	PCI WBF WRITE PNT ERR	PCI WBF READ PNT ERR	PCI RBF WRITE PNT ERR	PCI RBF READ PNT ERR	(RSV)	PBF0 CNT PARITY ERR
43		FCA::CHK2E30						
	PBF1 CNT PARITY ERR	PBF0 READ ADDRESS PARITY ERR	PBF1 READ ADDRESS PARITY ERR	PBF0 WRITE ADDRESS PARITY ERR	PBF1 WRITE ADDRESS PARITY ERR	FSB CNT PARITY ERR	FSB WRITE ADDRESS PARITY ERR	SCNT PARITY ERR
44		FCA::CHK2E31						
	SPCNT PARITY ERR	SPOINTER PARITY ERR	TWRSBC CNT PARITY ERR	TWRSSBC PARITY ERR	TRPRC PARITY ERR	TWRSBC CNT PARITY ERR	TWRSSBC PARITY ERR	BPM LRC0 ERR
45		FCA::CHK2E31						
	BPM LRC1 ERR	BPM LRC2 ERR	BPM PARITY ERR0	BPM PARITY ERR1	BPM READ ADR CNT PARITY ERR	BPM WRITE ADR CNT PARITY ERR	SPMS WRITE ADR CNT PARITY ERR	SPMG WRITE ADR CNT PARITY ERR
46		FCA::CHK2E31						
	SPM WRITE PARITY ERR	SPM READ PARITY ERR	SPM LRC ERR	SPMG READ ADR CNT PARITY ERR	SPMS READ ADR CNT PARITY ERR	CW XFR SBC GEN ERR	CW SEGMENT CNT PARITY ERR	CW SLOT CNT PARITY ERR
47		FCA::CHK2E31						
	CR SEGMENT CNT PARITY ERR	CR SLOT CNT PARITY ERR	CR XFR SBC GEN ERR	FDB DCNT PARITY ERR	FDB RCNT PARITY ERR	BPM PARITY ERR (0)	BPM PARITY ERR (1)	BPM PARITY ERR (2)
48		FCA::CHK2E32						
	BPM PARITY ERR (4)	TDSB CNT PARITY ERR	CBUF POINTER0 PARITY ERR	CBUF POINTER1 PARITY ERR	CCNT PARITY ERR	PCI SERR IN DMA	(RSV)	(RSV)
49		FCA::CHK2E32						
	BPM SCNT00 PARITY ERR	BPM SCNT01 PARITY ERR	BPM SCNT02 PARITY ERR	BPM SCNT02 PARITY ERR	BPM SCNT04 PARITY ERR	BPM SCNT05 PARITY ERR	BPM SCNT06 PARITY ERR	BPM SCNT07 PARITY ERR
4A		FCA::CHK2E32						
	BPM SCNT08 PARITY ERR	BPM SCNT09 PARITY ERR	BPM SCNT10 PARITY ERR	BPM SCNT11 PARITY ERR	BPM SCNT12 PARITY ERR	BPM SCNT13 PARITY ERR	BPM SCNT14 PARITY ERR	BPM SCNT15 PARITY ERR
4B		FCA::CHK2E32						
	BPM SCNT16 PARITY ERR	BPM SCNT17 PARITY ERR	BPM SCNT18 PARITY ERR	BPM SCNT19 PARITY ERR	BPM SCNT20 PARITY ERR	BPM SCNT21 PARITY ERR	BPM SCNT22 PARITY ERR	BPM SCNT23 PARITY ERR
4C		FCA::CHK2E33						
	BPM SCNT24 PARITY ERR	BPM SCNT25 PARITY ERR	BPM SCNT26 PARITY ERR	BPM SCNT27 PARITY ERR	BPM SCNT28 PARITY ERR	BPM SCNT29 PARITY ERR	BPM SCNT30 PARITY ERR	BPM SCNT31 PARITY ERR
4D		FCA::CHK2E40						
	DTN WBF WRITE PNT PARITY ERR	DTN WBF READ PNT PARITY ERR	DTN RBF WRITE PNT PARITY ERR	DTN RBF READ PNT PARITY ERR	QDTA ABORT	QDTA TIME OUT	DTN I/F PARITY ERR	DTN TIME OUT CNT PARITY ERR
4E		FCA::CHK2E40						
	FSB RADR PARITY ERR	RPOINT PARITY ERR	FCNT PARITY ERR	FPCNT PARITY ERR	NCNT PARITY ERR	NPCNT PARITY ERR	TCSBC PARITY ERR	ABUF POINT0 PARITY ERR
4F		FCA::CHK2E40						
	ABUF POINT1 PARITY ERR	ACNT PARITY ERR	APCNT PARITY ERR	BBUF POINT0 PARITY ERR	BBUF POINT1 PARITY ERR	BCNT PARITY ERR	BPCNT PARITY ERR	QDTA CHK2

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(3) Byte28 = 20 (2/4)

	0	1	2	3	4	5	6	7
50		FCA::CHK2E40						
	(RSV)	(RSV)	CR CSA CNT PARITY ERR	CW SLV0 CSA CNT PARITY ERR	CW SLV1 CSA CNT PARITY ERR	FMB WADR CNT PARITY ERR	FMB RADR CNT PARITY ERR	FDB WADR CNT PARITY ERR
51		FCA::CHK2E41						
	CC0 LA CNT PARITY ERR	CC2 LA CNT PARITY ERR	CC2 LBA CNT PARITY ERR	CG2 LA CNT PARITY ERR	CC3 LA CNT PARITY ERR	CC3 LBA CNT PARITY ERR	CC4 LA CNT PARITY ERR	CC4 LBA CNT PARITY ERR
52		FCA::CHK2E41						
	SEQ50 PARITY ERR	SEQ55 PARITY ERR	SEQ75 PARITY ERR	SEQ77 PARITY ERR	FLG ERR0	FLG ERR1	(RSV)	(RSV)
53		FCA::CHK2F30						
	PCI RBF0 PARITY ERR	PCI RBF1 PARITY ERR	PCI RBF2 PARITY ERR	PCI RBF3 PARITY ERR	PCI RBF4 PARITY ERR	PCI RBF5 PARITY ERR	PCI RBF6 PARITY ERR	PCI RBF7 PARITY ERR
54		FCA::CHK2F40						
	BBUF OUTPUT DATA PARITY ERR	CC2 SLRC ERR	SLV0 STS PATH ID ERR	SLV1 STS PATH ID ERR	CC3 SLRC ERR	CC3 DATA PLRC0 ERR	CC3 DATA PLRC1 ERR	CC3 DATA INV-PLRC0 ERR
55		FCA::CHK2F40						
	CC3 INV-PLRC1 ERR	CC3 DATA ENDCODE ERR	CC4 SLRC ERR	SLV0 STS PLRC0 ERR	SLV0 STS PLRC1 ERR	SLV0 STS INV-PLRC0 ERR	SLV0 STS INV-PLRC1 ERR	SLV1 STS PLRC0 ERR
56		FCA::CHK2F40						
	SLV1 STS PLRC1 ERR	SLV1 STS INV-PLRC0 ERR	SLV1 STS INV-PLRC1 ERR	SLV0 STS ENDCODE ERR	SLV1 STS ENDCODE ERR	SLV0 STS ANY ERR	SLV1 STS ANY ERR	QDTA ANY ERR
57		FCA::CHK2F40						
	DTN TX BUF0A PARITY ERR	DTN TX BUF1A PARITY ERR	DTN TX BUF2A PARITY ERR	DTN TX BUF3A PARITY ERR	DTN TX BUF4A PARITY ERR	DTN TX BUF5A PARITY ERR	DTN TX BUF6A PARITY ERR	DTN TX BUF7A PARITY ERR
58		FCA::CHK2F41						
	DTN RX BUF0 PARITY ERR	DTN RX BUF1 PARITY ERR	DTN RX BUF2 PARITY ERR	DTN RX BUF3 PARITY ERR	DTN RX BUF4 PARITY ERR	DTN RX BUF5 PARITY ERR	DTN RX BUF6 PARITY ERR	DTN RX BUF7 PARITY ERR
59		FCA::CHK2G40						
	CC2 LA ERR	CC2 LBA ERR	CC2 LLRC ERR	CC3 LA ERR	CC3 LBA ERR	CC3 LLRC ERR	CC,S LA ERR	CC4 LBA ERR
5A		FCA::CHK2G40						
	CC4 LLRC ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5B		FCA::TCSBC						
		TCSBC Counter(Cache Total Tansfer Subblock Number)						
5C		FCA::TCSBC						
		TCSBC Counter(Cache Total Tansfer Subblock Number)						
5D		FCA::BPRD						
		Cache Write Slot Pointer						
5E		FCA::BPRD						
		Cache Write Slot Pointer						
5F		FCA::C2SLRCM						
		CC2 SLRCM Value						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(3) Byte28 = 20 (3/4)

	0	1	2	3	4	5	6	7
60		FCA::C2SVSLRC						
		CC2 SVSLRC Value						
61		FCA::C2LA0						
		CC2 LA Value (BYTE0)						
62		FCA::C2LA14						
		CC2 LA Value (BYTE1)						
63		FCA::C2LA14						
		CC2 LA Value (BYTE2)						
64		FCA::C2LA14						
		CC2 LA Value (BYTE3)						
65		FCA::C2LA14						
		CC2 LA Value (BYTE4)						
66		FCA::C2LBAM						
		CC2 LBAM Value (BYTE0)						
67		FCA::C2LBA13M						
		CC2 LBAM Value (BYTE1)						
68		FCA::C2LBA13M						
		CC2 LBAM Value (BYTE2)						
69		FCA::C2LBA13M						
		CC2 LBAM Value (BYTE3)						
6A		FCA::CWCSA00						
		Slave 1 Cache Write Address (BYTE0)						
6B		FCA::CWCSA0104						
		Slave 1 Cache Write Address (BYTE1)						
6C		FCA::CWCSA0104						
		Slave 1 Cache Write Address (BYTE2)						
6D		FCA::CWCSA0104						
		Slave 1 Cache Write Address (BYTE3)						
6E		FCA::CWCSA0104						
		Slave 1 Cache Write Address (BYTE4)						
6F		FCA::CWCSA10						
		Slave 2 Cache Write Address (BYTE0)						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(3) Byte28 = 20 (4/4)

	0	1	2	3	4	5	6	7
70	FCA::CWCSA1114							
	Slave 2 Cache Write Address (BYTE1)							
71	FCA::CWCSA1114							
	Slave 2 Cache Write Address (BYTE2)							
72	FCA::CWCSA1114							
	Slave 2 Cache Write Address (BYTE3)							
73	FCA::CWCSA1114							
	Slave 2 Cache Write Address (BYTE4)							
74	FCA::BMPWT21							
	BPM0C Value When Writing to Cache							
75	FCA::BMPWT21							
	BPM0C Value When Writing to Cache							
76	Micro Information							
	CDEV#							
77	Micro Information							
	RDEV#							
78	Micro Information							
	RDEV#							
79	Micro Information							
	SCSI Command							
7A	Micro Information							
	LBA# (BYTE0)							
7B	Micro Information							
	LBA# (BYTE1)							
7C	Micro Information							
	LBA# (BYTE2)							
7D	Micro Information							
	LBA# (BYTE3)							
7E	Micro Information							
	Error Devided Result Code							
7F	Micro Information							
	CHK2 Detected Counter (Low)							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(4) Byte28 = 21, F1 (1/4)

	0	1	2	3	4	5	6	7
40		FCA::CHK2E30						
	(RSV)	SEQ15 PARITY ERR	SEQ00 PARITY ERR	SEQ20 PARITY ERR	SEQ25 PARITY ERR	SEQ27 PARITY ERR	SEQ28 PARITY ERR	SEQ30 PARITY ERR
41		FCA::CHK2E30						
	SEQ31 PARITY ERR	SEQ33 PARITY ERR	SEQ34 PARITY ERR	SEQ40 PARITY ERR	SEQ45 PARITY ERR	SEQ63 PARITY ERR	SEQ70 PARITY ERR	SEQ72 PARITY ERR
42		FCA::CHK2E30						
	SEQ90 PARITY ERR	SEQ92 PARITY ERR	PCI WBF WRITE PNT ERR	PCI WBF READ PNT ERR	PCI RBF WRITE PNT ERR	PCI RBF READ PNT ERR	(RSV)	PBF0 CNT PARITY ERR
43		FCA::CHK2E30						
	PBF1 CNT PARITY ERR	PBF0 READ ADDRESS PARITY ERR	PBF1 READ ADDRESS PARITY ERR	PBF0 WRITE ADDRESS PARITY ERR	PBF1 WRITE ADDRESS PARITY ERR	FSB CNT PARITY ERR	FSB WRITE ADDRESS PARITY ERR	SCNT PARITY ERR
44		FCA::CHK2E31						
	SPCNT PARITY ERR	SPOINTER PARITY ERR	TWRSBC CNT PARITY ERR	TWRSSBC PARITY ERR	TRPRC PARITY ERR	TWRSBC CNT PARITY ERR	TWRSSBC PARITY ERR	BPM LRC0 ERR
45		FCA::CHK2E31						
	BPM LRC1 ERR	BPM LRC2 ERR	BPM PARITY ERR0	BPM PARITY ERR1	BPM READ ADR CNT PARITY ERR	BPM WRITE ADR CNT PARITY ERR	SPMS WRITE ADR CNT PARITY ERR	SPMG WRITE ADR CNT PARITY ERR
46		FCA::CHK2E31						
	SPM WRITE PARITY ERR	SPM READ PARITY ERR	SPM LRC ERR	SPMG READ ADR CNT PARITY ERR	SPMS READ ADR CNT PARITY ERR	CW XFR SBC GEN ERR	CW SEGMENT CNT PARITY ERR	CW SLOT CNT PARITY ERR
47		FCA::CHK2E31						
	CR SEGMENT CNT PARITY ERR	CR SLOT CNT PARITY ERR	CR XFR SBC GEN ERR	FDB DCNT PARITY ERR	FDB RCNT PARITY ERR	BPM PARITY ERR (0)	BPM PARITY ERR (1)	BPM PARITY ERR (2)
48		FCA::CHK2E32						
	BPM PARITY ERR (4)	TDSB CNT PARITY ERR	CBUF POINTER0 PARITY ERR	CBUF POINTER1 PARITY ERR	CCNT PARITY ERR	PCI SERR IN DMA	(RSV)	(RSV)
49		FCA::CHK2E32						
	BPM SCNT00 PARITY ERR	BPM SCNT01 PARITY ERR	BPM SCNT02 PARITY ERR	BPM SCNT02 PARITY ERR	BPM SCNT04 PARITY ERR	BPM SCNT05 PARITY ERR	BPM SCNT06 PARITY ERR	BPM SCNT07 PARITY ERR
4A		FCA::CHK2E32						
	BPM SCNT08 PARITY ERR	BPM SCNT09 PARITY ERR	BPM SCNT10 PARITY ERR	BPM SCNT11 PARITY ERR	BPM SCNT12 PARITY ERR	BPM SCNT13 PARITY ERR	BPM SCNT14 PARITY ERR	BPM SCNT15 PARITY ERR
4B		FCA::CHK2E32						
	BPM SCNT16 PARITY ERR	BPM SCNT17 PARITY ERR	BPM SCNT18 PARITY ERR	BPM SCNT19 PARITY ERR	BPM SCNT20 PARITY ERR	BPM SCNT21 PARITY ERR	BPM SCNT22 PARITY ERR	BPM SCNT23 PARITY ERR
4C		FCA::CHK2E33						
	BPM SCNT24 PARITY ERR	BPM SCNT25 PARITY ERR	BPM SCNT26 PARITY ERR	BPM SCNT27 PARITY ERR	BPM SCNT28 PARITY ERR	BPM SCNT29 PARITY ERR	BPM SCNT30 PARITY ERR	BPM SCNT31 PARITY ERR
4D		FCA::CHK2E40						
	DTN WBF WRITE PNT PARITY ERR	DTN WBF READ PNT PARITY ERR	DTN RBF WRITE PNT PARITY ERR	DTN RBF READ PNT PARITY ERR	QDTA ABORT	QDTA TIME OUT	DTN I/F PARITY ERR	DTN TIME OUT CNT PARITY ERR
4E		FCA::CHK2E40						
	FSB RADR PARITY ERR	RPOINT PARITY ERR	FCNT PARITY ERR	FPCNT PARITY ERR	NCNT PARITY ERR	NPCNT PARITY ERR	TCSBC PARITY ERR	ABUF POINT0 PARITY ERR
4F		FCA::CHK2E40						
	ABUF POINT1 PARITY ERR	ACNT PARITY ERR	APCNT PARITY ERR	BBUF POINT0 PARITY ERR	BBUF POINT1 PARITY ERR	BCNT PARITY ERR	BPCNT PARITY ERR	QDTA CHK2

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(4) Byte28 = 21 (2/4)

	0	1	2	3	4	5	6	7
50		FCA::CHK2E40						
	(RSV)	(RSV)	CR CSA CNT PARITY ERR	CW SLV0 CSA CNT PARITY ERR	CW SLV1 CSA CNT PARITY ERR	FMB WADR CNT PARITY ERR	FMB RADR CNT PARITY ERR	FDB WADR CNT PARITY ERR
51		FCA::CHK2E41						
	CC0 LA CNT PARITY ERR	CC2 LA CNT PARITY ERR	CC2 LBA CNT PARITY ERR	CG2 LA CNT PARITY ERR	CC3 LA CNT PARITY ERR	CC3 LBA CNT PARITY ERR	CC4 LA CNT PARITY ERR	CC4 LBA CNT PARITY ERR
52		FCA::CHK2E41						
	SEQ50 PARITY ERR	SEQ55 PARITY ERR	SEQ75 PARITY ERR	SEQ77 PARITY ERR	FLG ERR0	FLG ERR1	(RSV)	(RSV)
53		FCA::CHK2F30						
	PCI RBF0 PARITY ERR	PCI RBF1 PARITY ERR	PCI RBF2 PARITY ERR	PCI RBF3 PARITY ERR	PCI RBF4 PARITY ERR	PCI RBF5 PARITY ERR	PCI RBF6 PARITY ERR	PCI RBF7 PARITY ERR
54		FCA::CHK2F30						
	PCI WBF0 PARITY ERR	PCI WBF1 PARITY ERR	PCI WBF2 PARITY ERR	PCI WBF3 PARITY ERR	PCI WBF4 PARITY ERR	PCI WBF5 PARITY ERR	PCI WBF6 PARITY ERR	PCI WBF7 PARITY ERR
55		FCA::CHK2F40						
	BBUF OUTPUT DATA PARITY ERR	CC2 SLRC ERR	SLV0 STS PATH ID ERR	SLV1 STS PATH ID ERR	CC3 SLRC ERR	CC3 DATA PLRC0 ERR	CC3 DATA PLRC1 ERR	CC3 DATA INV-PLRC0 ERR
56		FCA::CHK2F40						
	CC3 INV-PLRC1 ERR	CC3 DATA ENDCODE ERR	CC4 SLRC ERR	SLV0 STS PLRC0 ERR	SLV0 STS PLRC1 ERR	SLV0 STS INV-PLRC0 ERR	SLV0 STS INV-PLRC1 ERR	SLV1 STS PLRC0 ERR
57		FCA::CHK2F40						
	SLV1 STS PLRC1 ERR	SLV1 STS INV-PLRC0 ERR	SLV1 STS INV-PLRC1 ERR	SLV0 STS ENDCODE ERR	SLV1 STS ENDCODE ERR	SLV0 STS ANY ERR	SLV1 STS ANY ERR	QDTA ANY ERR
58		FCA::CHK2F40						
	DTN TX BUF0A PARITY ERR	DTN TX BUF1A PARITY ERR	DTN TX BUF2A PARITY ERR	DTN TX BUF3A PARITY ERR	DTN TX BUF4A PARITY ERR	DTN TX BUF5A PARITY ERR	DTN TX BUF6A PARITY ERR	DTN TX BUF7A PARITY ERR
59		FCA::CHK2F41						
	DTN RX BUF0 PARITY ERR	DTN RX BUF1 PARITY ERR	DTN RX BUF2 PARITY ERR	DTN RX BUF3 PARITY ERR	DTN RX BUF4 PARITY ERR	DTN RX BUF5 PARITY ERR	DTN RX BUF6 PARITY ERR	DTN RX BUF7 PARITY ERR
5A		FCA::CHK2G40						
	CC2 LA ERR	CC2 LBA ERR	CC2 LLRC ERR	CC3 LA ERR	CC3 LBA ERR	CC3 LLRC ERR	CC,S LA ERR	CC4 LBA ERR
5B		FCA::CHK2G40						
	CC4 LLRC ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5C		FCA::TDSBC						
		TDSBC Counter(Drive Total Tansfer Subblock Number)						
5D		FCA::TDSBC						
		TDSBC Counter(Drive Total Tansfer Subblock Number)						
5E		FCA::BPRE						
		Cache Read Slot Pointer						
5F		FCA::BPRE						
		Cache Read Segment Pointer						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(4) Byte28 = 21 (3/4)

	0	1	2	3	4	5	6	7
60	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
61	FCA::SLRC7SV							
	SLRC7SV Value							
62	FCA::C3SLRCM							
	CC3 SLRCM Value							
63	FCA::C3LA0							
	CC3 LA Value (BYTE0)							
64	FCA::C3LA14M							
	CC3 LA Value (BYTE1)							
65	FCA::C3LA14M							
	CC3 LA Value (BYTE2)							
66	FCA::C3LA14M							
	CC3 LA Value (BYTE3)							
67	FCA::C3LA14M							
	CC3 LA Value (BYTE4)							
68	FCA::C3SVLRC							
	CC3 SVLRC Value							
69	FCA::C3PLRCM							
	CC3 PLRCM Value							
6A	FCA::C3PLRCM							
	CC3 PLRCM Value							
6B	FCA::C3LBAM							
	CC3 LBAM Value (BYTE0)							
6C	FCA::C3LBA13M							
	CC3 LBAM Value (BYTE1)							
6D	FCA::C3LBA13M							
	CC3 LBAM Value (BYTE2)							
6E	FCA::C3LBA13M							
	CC3 LBAM Value (BYTE3)							
6F	FCA::CRCSA00							
	Cache Read Address (BYTE0)							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(4) Byte28 = 21 (4/4)

	0	1	2	3	4	5	6	7
70	FCA::CRCSA0104							
	Cache Read Address (BYTE1)							
71	FCA::CRCSA0104							
	Cache Read Address (BYTE2)							
72	FCA::CRCSA0104							
	Cache Read Address (BYTE3)							
73	FCA::CRCSA0104							
	Cache Read Address (BYTE4)							
74	FCA::BMPRD21							
	BPM0C Value When Reading from Cache							
75	FCA::BMPRD21							
	BPM0C Value When Reading from Cache							
76	Micro Information							
	CDEV#							
77	Micro Information							
	RDEV#							
78	Micro Information							
	RDEV#							
79	Micro Information							
	SCSI Command							
7A	Micro Information							
	LBA# (BYTE0)							
7B	Micro Information							
	LBA# (BYTE1)							
7C	Micro Information							
	LBA# (BYTE2)							
7D	Micro Information							
	LBA# (BYTE3)							
7E	Micro Information							
	Error Devided Result Code							
7F	Micro Information							
	CHK2 Detected Counter (Low)							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(5) Byte28 = 30 (1/4)

	0	1	2	3	4	5	6	7
40		FCA::CHK2E40						
	DTN WBF WR POINTER PARITY ERR	DTN WBF RD POINTER PARITY ERR	DTN RBF WR POINTER PARITY ERR	SEQ20 RD POINTER PARITY ERR	QDTA ABORT	QDTA TIMEOUT	DTN I/F PARITY ERR	DTN TIME OUT CNT PARITY ERR
41		FCA::CHK2E41						
	DTN RX BUF0 PARITY ERR	DTN RX BUF1 PARITY ERR	DTN RX BUF2 PARITY ERR	DTN RX BUF3 PARITY ERR	DTN RX BUF4 PARITY ERR	DTN RX BUF5 PARITY ERR	DTN RX BUF6 PARITY ERR	DTN RX BUF7 PARITY ERR
42		FCA::TCSBC						
		TCSBC Counter(Cache Total Tansfer Subblock Number)						
43		FCA::TCSBC						
		TCSBC Counter(Cache Total Tansfer Subblock Number)						
44		FCA::BPRD						
		Cache Write Slot Pointer						
45		FCA::BPRD						
		Cache Write Slot Pointer						
46		FCA::C2SLRCM						
		CC2 SLRCM Value						
47		FCA::C2SVSLRC						
		CC2 SVSLRC Value						
48		FCA::C2LA0						
		CC2 LA Value (BYTE0)						
49		FCA::C2LA14M						
		CC2 LA Value (BYTE1)						
4A		FCA::C2LA14M						
		CC2 LA Value (BYTE2)						
4B		FCA::C2LA14M						
		CC2 LA Value (BYTE3)						
4C		FCA::C2LA14M						
		CC2 LA Value (BYTE4)						
4D		FCA::CWCSA00						
		Slave 1 Cache Write Address (BYTE0)						
4E		FCA::CWCSA0104						
		Slave 1 Cache Write Address (BYTE1)						
4F		FCA::CWCSA0104						
		Slave 1 Cache Write Address (BYTE2)						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(5) Byte28 = 30 (2/4)

	0	1	2	3	4	5	6	7
50		FCA::CWCSA0104						
		Slave 1 Cache Write Address (BYTE3)						
51		FCA::CWCSA0104						
		Slave 1 Cache Write Address (BYTE4)						
52		FCA::CWCSA10						
		Slave 2 Cache Write Address (BYTE0)						
53		FCA::CWCSA1114						
		Slave 2 Cache Write Address (BYTE1)						
54		FCA::CWCSA1114						
		Slave 2 Cache Write Address (BYTE2)						
55		FCA::CWCSA1114						
		Slave 2 Cache Write Address (BYTE3)						
56		FCA::CWCSA1114						
		Slave 2 Cache Write Address (BYTE4)						
57		FCA::BMPWT21						
		BPM0C Value When Writing to Cache						
58		FCA::BMPWT21						
		BPM0C Value When Writing to Cache						
59		FCA::BMPWT21						
		BPM0C Value When Writing to Cache						
5A		FCA::BMPWT21						
		BPM0C Value When Writing to Cache						
5B		FCA::CHSNSTS00						
	STATUS0 ERR	STATUS0 CARB ERR	STATUS0 CMA ERR	STATUS0 Reserved	STATUS0 CMA STATUS NG	STATUS0 CMA FIFO MODE	STATUS0 CMA WARNING	STATUS0 Reserved
5C		FCA::CHSNSTS00						
	STATUS0 Reserved	STATUS0 PATH ID			STATUS0 Reserved		STATUS0 CACHE P/K#	
5D		FCA::CHSNSTS00						
	STATUS0 Reserved	STATUS0 PATH ID			STATUS0 Reserved		STATUS0 CACHE P/K#	
5E		FCA::CHSNSTS00						
	STATUS0 ERR	STATUS0 CARB ERR	STATUS0 CMA ERR	STATUS0 Reserved	STATUS0 CMA STATUS NG	STATUS0 CMA FIFO MODE	STATUS0 CMA WARNING	STATUS0 Reserved
5F		FCA::CHSNSTS01						
	STS0 CARB PXDR INDPE	STS0 CARB PXLRCE	STS0 CARB PXDR OUTDPE	STS0 CARB PXOR INDPE	STS0 CARB PXTME	STS0 CARB ABTE	STS0 CARB PXHE	STS0 CARB PXMAE

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(5) Byte28 = 30 (3/4)

	0	1	2	3	4	5	6	7
60		FCA::CHSNSTS01						
	STS0 CARB CXOR INDPE	STS0 CARB CXDR INDPE	STS0 CARB CXLRCE	STS0 CARB CXDR OUTDPE	STS0 CARB CXTME	STS0 CARB CXHE	STS0 CARB Reserved	STS0 CARB Reserved
61		FCA::CHSNSTS01						
	STS0 CMA BOARD DISABLE	STS0 CMA MEM NOT RDY	STS0 CMA MODULE DISABLE	STS0 CMA MEM BACKUP MODE	STS0 CMA DIAG UMNT	STS0 CMA SP UMNT	STS0 CMA REG CODE ERR	STS0 CMA INVLD COM
62		FCA::CHSNSTS01						
	STS0 CMA PKID PEER	STS0 CMA GSLRCER	STS0 CMA DT PKT ER	STS0 CMA CMD PKT ER	STS0 CMA MODULE ER	STS0 CMA HCTL ER	STS0 CMA MCTL ER	STS0 CMA BRD ER
63		FCA::CHSNSTS10						
	STATUS1 ERR	STATUS1 CARB ERR	STATUS1 CMA ERR	STATUS1 Reserved	STATUS1 CMA STATUS NG	STATUS1 CMA FIFO MODE	STATUS1 CMA WARNING	STATUS1 Reserved
64		FCA::CHSNSTS10						
	STATUS1 Reserved		STATUS1 PATH ID		STATUS1 Reserved		STATUS1 CACHE P/K#	
65		FCA::CHSNSTS10						
	STATUS1 Reserved		STATUS1 PATH ID		STATUS1 Reserved		STATUS1 CACHE P/K#	
66		FCA::CHSNSTS10						
	STATUS1 ERR	STATUS1 CARB ERR	STATUS1 CMA ERR	STATUS1 Reserved	STATUS1 CMA STATUS NG	STATUS1 CMA FIFO MODE	STATUS1 CMA WARNING	STATUS1 Reserved
67		FCA::CHSNSTS11						
	STS1 CARB PXDR INDPE	STS1 CARB PXLRCE	STS1 CARB PXDR OUTDPE	STS1 CARB PXOR INDPE	STS1 CARB PXTME	STS1 CARB ABTE	STS1 CARB PXHE	STS1 CARB PXMAE
68		FCA::CHSNSTS11						
	STS1 CARB CXOR INDPE	STS1 CARB CXDR INDPE	STS1 CARB CXLRCE	STS1 CARB CXDR OUTDPE	STS1 CARB CXTME	STS1 CARB CXHE	STS1 CARB Reserved	STS1 CARB Reserved
69		FCA::CHSNSTS11						
	STS1 CMA BOARD DISABLE	STS1 CMA MEM NOT RDY	STS1 CMA MODULE DISABLE	STS1 CMA MEM BACKUP MODE	STS1 CMA DIAG UMNT	STS1 CMA SP UMNT	STS1 CMA REG CODE ERR	STS1 CMA INVLD COM
6A		FCA::CHSNSTS11						
	STS1 CMA PKID PEER	STS1 CMA GSLRCER	STS1 CMA DT PKT ER	STS1 CMA CMD PKT ER	STS1 CMA MODULE ER	STS1 CMA HCTL ER	STS1 CMA MCTL ER	STS1 CMA BRD ER
6B		FCA::QDSTS0						
	ANT ERROR	CHK2A/2B	CHK2C	CHK2D	STATUS0 VALID	STATUS1 VALID	P0 USE FLAG	P1 USE FLAG
6C		FCA::QDSTS0						
	P0 ERRINT	P1 ERRINT	STATUS0 C-ERR	STATUS1 C-ERR	DT0 PLRC ERR	DT1 PLRC ERR	STATUS0 PLRC ERR ERR	STATUS0 INV-PLRC ERR
6D		FCA::QDSTS0						
	STATUS0 END-CODE ERR	STATUS0 PLRC ERR ERR	STATUS0 INV-PLRC ERR	STATUS0 END-CODE ERR	(RSV)	(RSV)	I/O DT0 ERR	I/O DT1 ERR
6E		FCA::QDSTS0						
	I/O DT2 ERR	I/O DT3 ERR	STATUS0 DT0-3 PARITY ERR	STATUS0 DT4-7 PARITY ERR	STATUS1 DT0-3 PARITY ERR	STATUS1 DT4-7 PARITY ERR	TIME OUT	ABT ERR
6F		FCA::QDSTS1						
	DTN SEQ ERR	DTN INPUT CTL ERR	DTN RD CTL ERR	DTN WT CTL ERR	P0 SYNCI PNT ERR	P1 SYNCI PNT ERR	P0 SYNCI CLOCK ERR	P1 SYNCI CLOCK ERR

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(5) Byte28 = 30 (4/4)

	0	1	2	3	4	5	6	7
70		FCA::QDSTS1						
	P0 SLRC CNT ERR	P0 SEQ ERR	P0 TX RD PNT PARITY ERR	P0 RX WT PNT PARITY ERR	P1 SLRC CNT ERR	P1 SEQ ERR	P1 TX RD PNT PARITY ERR	P1 RX WT PNT PARITY ERR
71		FCA::QDSTS1						
	I/O DT2 ERR	I/O DT3 ERR	STATUS0 DT0-3 PARITY ERR	STATUS0 DT4-7 PARITY ERR	STATUS1 DT0-3 PARITY ERR	STATUS1 DT4-7 PARITY ERR	TIME OUT	ABT ERR
72		FCA::QDSTS1						
	TRANS MODE ERR	ADR/CMD PLRC ERR	ADR/CMD END-CODE ERR	ADR/CMD DT PARITY ERR	DTN DT0-3 PARITY ERR	DTN DT4-7 PARITY ERR	P0 PLRC ERR	P1 PLRC ERR
73		DRR::D0ESTA0						
	TX DR PARITY ERR	TX RDPT PARITY ERR	DTN SEQ ERR	DTN WTPT PARITY ERR	WT DTCT PARITY ERR	INPUT CLTDT PARITY ERR	IDTPT PARITY ERR	DTN RDDCT PARITY ERR
74		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
75		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
76		Micro Information						
		CDEV#						
77		Micro Information						
		RDEV#						
78		Micro Information						
		RDEV#						
79		Micro Information						
		SCSI Command						
7A		Micro Information						
		LBA# (BYTE0)						
7B		Micro Information						
		LBA# (BYTE1)						
7C		Micro Information						
		LBA# (BYTE2)						
7D		Micro Information						
		LBA# (BYTE3)						
7E		Micro Information						
		Error Devided Result Code						
7F		Micro Information						
		CHK2 Detected Counter (Low)						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(6) Byte28 = 31 (1/4)

	0	1	2	3	4	5	6	7
40	FCA::CHK2E40							
	DTN WBF WR POINTER PARITY ERR	DTN WBF RD POINTER PARITY ERR	DTN RBF WR POINTER PARITY ERR	SEQ20 RD POINTER PARITY ERR	QDTA ABORT	QDTA TIMEOUT	DTN I/F PARITY ERR	DTN TIME OUT CNT PARITY ERR
41	FCA::CHK2E41							
	DTN RX BUF0 PARITY ERR	DTN RX BUF1 PARITY ERR	DTN RX BUF2 PARITY ERR	DTN RX BUF3 PARITY ERR	DTN RX BUF4 PARITY ERR	DTN RX BUF5 PARITY ERR	DTN RX BUF6 PARITY ERR	DTN RX BUF7 PARITY ERR
42	FCA::TDSBC							
	TDSBC Counter(Drive Total Tansfer Subblock Number)							
43	FCA::TDSBC							
	TDSBC Counter(Drive Total Tansfer Subblock Number)							
44	FCA::BPRE							
	Cache Read Slot Pointer							
45	FCA::BPRE							
	Cache Read Segment Pointer							
46	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
47	FCA::SLRC7SV							
	SLRC7SV Value							
48	FCA::C3SLRCM							
	CC3 SLRCM Value							
49	FCA::C3LA0							
	CC3 LA Value (BYTE0)							
4A	FCA::C3LA14M							
	CC3 LA Value (BYTE1)							
4B	FCA::C3LA14M							
	CC3 LA Value (BYTE2)							
4C	FCA::C3LA14M							
	CC3 LA Value (BYTE3)							
4D	FCA::C3LA14M							
	CC3 LA Value (BYTE4)							
4E	FCA::C3SVLRC							
	CC3 SVLRC Value							
4F	FCA::C3PLRCM							
	CC3 PLRCM Value							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(6) Byte28 = 31 (2/4)

	0	1	2	3	4	5	6	7
50		FCA::C3PLRCM						
		CC3 PLRCM Value						
51		FCA::CRCSA00						
		Cache Read Address (BYTE0)						
52		FCA::CRCSA0104						
		Cache Read Address (BYTE1)						
53		FCA::CRCSA0104						
		Cache Read Address (BYTE2)						
54		FCA::CRCSA0104						
		Cache Read Address (BYTE3)						
55		FCA::CRCSA0104						
		Cache Read Address (BYTE4)						
56		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
57		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
58		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
59		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
5A		FCA::CHSNSTS00						
	STATUS0 ERR	STATUS0 CARB ERR	STATUS0 CMA ERR	STATUS0 Reserved	STATUS0 CMA STATUS NG	STATUS0 CMA FIFO MODE	STATUS0 CMA WARNING	STATUS0 Reserved
5B		FCA::CHSNSTS00						
	STATUS0 Reserved	STATUS0 PATH ID			STATUS0 Reserved		STATUS0 CACHE P/K#	
5C		FCA::CHSNSTS00						
	STATUS0 Reserved	STATUS0 PATH ID			STATUS0 Reserved		STATUS0 CACHE P/K#	
5D		FCA::CHSNSTS00						
	STATUS0 ERR	STATUS0 CARB ERR	STATUS0 CMA ERR	STATUS0 Reserved	STATUS0 CMA STATUS NG	STATUS0 CMA FIFO MODE	STATUS0 CMA WARNING	STATUS0 Reserved
5E		FCA::CHSNSTS01						
	STS0 CARB PXDR INDPE	STS0 CARB PXLRCE	STS0 CARB PXDR OUTDPE	STS0 CARB PXOR INDPE	STS0 CARB PXTME	STS0 CARB ABTE	STS0 CARB PXHE	STS0 CARB PXMAE
5F		FCA::CHSNSTS01						
	STS0 CARB CXOR INDPE	STS0 CARB CXDR INDPE	STS0 CARB CXLRCE	STS0 CARB CXDR OUTDPE	STS0 CARB CXTME	STS0 CARB CXHE	STS0 CARB Reserved	STS0 CARB Reserved

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(6) Byte28 = 31 (3/4)

	0	1	2	3	4	5	6	7
60		FCA::CHSNSTS01						
	STS0 CMA BOARD DISABLE	STS0 CMA MEM NOT RDY	STS0 CMA MODULE DISABLE	STS0 CMA MEM BACKUP MODE	STS0 CMA DIAG UMNT	STS0 CMA SP UMNT	STS0 CMA REG CODE ERR	STS0 CMA INVLD COM
61		FCA::CHSNSTS01						
	STS0 CMA PKID PEER	STS0 CMA GSLRCER	STS0 CMA DT PKT ER	STS0 CMA CMD PKT ER	STS0 CMA MODULE ER	STS0 CMA HCTL ER	STS0 CMA MCTL ER	STS0 CMA BRD ER
62		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
63		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
64		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
65		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
66		DRR::D0ESTA0						
	TX DR PARITY ERR	TX RDPT PARITY ERR	DTN SEQ ERR	DTN WTPT PARITY ERR	WT DTCT PARITY ERR	INPUT CLTDT PARITY ERR	IDTPT PARITY ERR	DTN RDDCT PARITY ERR
67		DRR::D0ESTA0						
	P0 SYNCI0 PNT PARITY ERR	P0 SYNCI1 PNT PARITY ERR	P0 SYNCI0 CLOCK ERR	P0 SYNCI1 CLOCK ERR	P0 TXX SEQ ERR	P0 TX RD PNT PARITY ERR	P0 RX SEQ ERR	P0 RX WT PNT PARITY ERR
68		DRR::D0ESTA1						
	P1 SYNCI0 PNT PARITY ERR	P1 SYNCI1 PNT PARITY ERR	P1 SYNCI0 CLOCK ERR	P1 SYNCI1 CLOCK ERR	P1 TXX SEQ ERR	P1 TX RD PNT PARITY ERR	P1 RX SEQ ERR	P1 RX WT PNT PARITY ERR
69		DRR::D0ESTA1						
	P0 TX SEQ PARITY ERR	P1 TX SEQ PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6A		DRR::D0ESTA2						
	STATUS0 PLRC ERR	STATUS0 INV-PLRC ERR	STATUS0 END-CODE ERR	STATUS1 PLRC ERR	STATUS1 INV-PLRC ERR	STATUS1 END-CODE ERR	TRANS MODE ERR	(RSV)
6B		DRR::D0ESTA2						
	ADR/CMD PLRC ERR	ADR/CMD INV-PLRC ERR	ADR/CMD END-CODE ERR	ADR/CMD DT PARITY ERR	OUT DT00 PARITY ERR	OUT DT01 PARITY ERR	OUT DT02 PARITY ERR	OUT DT03 PARITY ERR
6C		DRR::D0ESTA3						
	OUT DT10 PARITY ERR	OUT DT11 PARITY ERR	OUT DT12 PARITY ERR	OUT DT13 PARITY ERR	OUTPUT LOOP DT0 PARITY ERR	OUTPUT LOOP DT1 PARITY ERR	OUTPUT LOOP DT2 PARITY ERR	OUTPUT LOOP DT3 PARITY ERR
6D		DRR::D0ESTA5						
	P0 TX DT0 PARITY ERR	P0 TX DT1 PARITY ERR	P0 TX DT2 PARITY ERR	P0 TX DT3 PARITY ERR	P0 TX DT4 PARITY ERR	P0 TX DT5 PARITY ERR	P0 TX DT6 PARITY ERR	P0 TX DT7 PARITY ERR
6E		DRR::D0ESTA5						
	P0 RX DT0 PARITY ERR	P0 RX DT1 PARITY ERR	P1 RX DT0 PARITY ERR	P1 RX DT1 PARITY ERR	P0 RX DT4 PARITY ERR	P0 RX DT5 PARITY ERR	P1 RX DT4 PARITY ERR	P1 RX DT5 PARITY ERR
6F		DRR::D0ESTA6						
	P0 TXX I-DT0 PARITY ERR	P0 TXX I-DT1 PARITY ERR	P0 TXX O-DT0 PARITY ERR	P0 TXX O-DT1 PARITY ERR	P1 TXX I-DT0 PARITY ERR	P1 TXX I-DT1 PARITY ERR	P1 TXX O-DT0 PARITY ERR	P1 TXX O-DT1 PARITY ERR

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(6) Byte28 = 31 (4/4)

	0	1	2	3	4	5	6	7
70	DRR::D0ESTA6							
	P1 TX DT0 PARITY ERR	P1 TX DT1 PARITY ERR	P1 TX DT2 PARITY ERR	P1 TX DT3 PARITY ERR	P1 TX DT4 PARITY ERR	P1 TX DT5 PARITY ERR	P1 TX DT6 PARITY ERR	P1 TX DT7 PARITY ERR
71	DRR::D0ESTA7							
	IN DT0 PARITY ERR	IN DT1 PARITY ERR	IN DT2 PARITY ERR	IN DT3 PARITY ERR	P0 ERRINT	P1 ERRINT	P0 DT CARB/CMA ERR	P0 STATUS1 CARB/CMA ERR
72	DRR::D0ESTAB							
	P0 ADR/CMD PLRC ERR	P0 DT PLRC ERR	P0 STATUS0 PLRC ERR	P0 STATUS1 PLRC ERR	P0 ADR/CMD INV-PLRC ERR	P0 DT INV-PLRC ERR	P0 STATUS0 INV-PLRC ERR	P0 STATUS1 INV-PLRC ERR
73	DRR::D0ESTAB							
	P0 ADR/CMD END-CODE ERR	P0 DT END-CODE ERR	P0 STATUS0 END-CODE ERR	P0 STATUS1 END-CODE ERR	P0 SLRC CHECK ERR	P0 SLRC CAL DT ERR	P0 SLRC RD DT ERR	P0 SBLK DCNT ERR
74	DRR::D0ESTAC							
	P1 ADR/CMD PLRC ERR	P1 DT PLRC ERR	P1 STATUS0 PLRC ERR	P1 STATUS1 PLRC ERR	P1 ADR/CMD INV-PLRC ERR	P1 DT INV-PLRC ERR	P1 STATUS0 INV-PLRC ERR	P1 STATUS1 INV-PLRC ERR
75	DRR::D0ESTAC							
	P1 ADR/CMD END-CODE ERR	P1 DT END-CODE ERR	P1 STATUS0 END-CODE ERR	P1 STATUS1 END-CODE ERR	P1 SLRC CHECK ERR	P1 SLRC CAL DT ERR	P1 SLRC RD DT ERR	P1 SBLK DCNT ERR
76	Micro Information							
	CDEV#							
77	Micro Information							
	RDEV#							
78	Micro Information							
	RDEV#							
79	Micro Information							
	SCSI Command							
7A	Micro Information							
	LBA#(byte0)							
7B	Micro Information							
	LBA#(byte1)							
7C	Micro Information							
	LBA#(byte2)							
7D	Micro Information							
	LBA#(byte3)							
7E	Micro Information							
	Error Devided Result Code							
7F	Micro Information							
	CHK2 Detected Counter (Low)							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(7) Byte28 = 40, 41, 60, 61 (1/4)

	0	1	2	3	4	5	6	7
40	FCA::CHK2E30							
	(RSV)	SEQ15 PARITY ERR	SEQ00 PARITY ERR	SEQ20 PARITY ERR	SEQ25 PARITY ERR	SEQ27 PARITY ERR	SEQ28 PARITY ERR	SEQ30 PARITY ERR
41	FCA::CHK2E30							
	SEQ31 PARITY ERR	SEQ33 PARITY ERR	SEQ34 PARITY ERR	SEQ40 PARITY ERR	SEQ45 PARITY ERR	SEQ63 PARITY ERR	SEQ70 PARITY ERR	SEQ72 PARITY ERR
42	FCA::CHK2E30							
	SEQ90 PARITY ERR	SEQ92 PARITY ERR	PCI WBF WRITE PNT ERR	PCI WBF READ PNT ERR	PCI RBF WRITE PNT ERR	PCI RBF READ PNT ERR	(RSV)	PBF0 CNT PARITY ERR
43	FCA::CHK2E30							
	PBF1 CNT PARITY ERR	PBF0 READ ADDRESS PARITY ERR	PBF1 READ ADDRESS PARITY ERR	PBF0 WRITE ADDRESS PARITY ERR	PBF1 WRITE ADDRESS PARITY ERR	FSB CNT PARITY ERR	FSB WRITE ADDRESS PARITY ERR	SCNT PARITY ERR
44	FCA::CHK2F30							
	PCI RBF0 PARITY ERR	PCI RBF1 PARITY ERR	PCI RBF2 PARITY ERR	PCI RBF3 PARITY ERR	PCI RBF4 PARITY ERR	PCI RBF5 PARITY ERR	PCI RBF6 PARITY ERR	PCI RBF7 PARITY ERR
45	FCA::CHK2F30							
	PCI WBF0 PARITY ERR	PCI WBF1 PARITY ERR	PCI WBF2 PARITY ERR	PCI WBF3 PARITY ERR	PCI WBF4 PARITY ERR	PCI WBF5 PARITY ERR	PCI WBF6 PARITY ERR	PCI WBF7 PARITY ERR
46	FCA::TCSBC							
	TCSBC Counter(Cache Total Tansfer Subblock Number)							
47	FCA::TCSBC							
	TCSBC Counter(Cache Total Tansfer Subblock Number)							
48	FCA::TDSBC							
	TDSBC Counter(Drive Total Tansfer Subblock Number)							
49	FCA::TDSBC							
	TDSBC Counter(Drive Total Tansfer Subblock Number)							
4A	FCA::BPRD							
	Cache Write Slot Pointer							
4B	FCA::BPRD							
	Cache Write Segment Pointer							
4C	FCA::BPRE							
	Cache Read Slot Pointer							
4D	FCA::BPRE							
	Cache Read Segment Pointer							
4E	FCA::PBFID							
	PBF0 Side DMA ID							
4F	FCA::PBFID							
	PBF0 Side DMA ID							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(7) Byte28 = 40, 41, 60, 61 (2/4)

	0	1	2	3	4	5	6	7
50		FCA::PBFID						
		PBF1 Side DMA ID						
51		FCA::PBFID						
		PBF1 Side DMA ID						
52		FCA::BMPWT21						
		BPM0C Value When Writing to Cache						
53		FCA::BMPWT21						
		BPM0C Value When Writing to Cache						
54		FCA::BMPWT21						
		BPM0C Value When Writing to Cache						
55		FCA::BMPWT21						
		BPM0C Value When Writing to Cache						
56		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
57		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
58		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
59		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
5A		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5B		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5C		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5D		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5E		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5F		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(7) Byte28 = 40, 41, 60, 61 (3/4)

	0	1	2	3	4	5	6	7
60	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
61	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
62	FCA::PCICTL							
	PCI BUS RESET	PCI ARB RESET	OPEN MODE	PCI BUS ENABLE	PCI ARB ENABLE	REQ0 ENABLE	REQ1 ENABLE	REQ2 ENABLE
63	FCA::PCICTL							
	SERR OUT ENABLE	SERR RCV ENABLE	PERR RCV ENABLE	(RSV)	(RSV)	(RSV)	(RSV)	PCI DATA EX MODE
64	FCA::SPREQAD							
	PDEV ID							
65	FCA::SPREQAD							
	QUE ID							
66	FCA::DPREQAD							
	PDEV ID							
67	FCA::DPREQAD							
	QUE ID							
68	FCA::TLMWAM							
	TLMWAM Value							
69	FCA::TLMWAM							
	TLMWAM Value							
6A	FCA::TLMRAM							
	TLMRAM Value							
6B	FCA::TLMRAM							
	TLMRAM Value							
6C	FCA::CWCSA00							
	Slave 1 Cache Write Address (BYTE0)							
6D	FCA::CWCSA0104							
	Slave 1 Cache Write Address (BYTE1)							
6E	FCA::CWCSA0104							
	Slave 1 Cache Write Address (BYTE2)							
6F	FCA::CWCSA0104							
	Slave 1 Cache Write Address (BYTE3)							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(7) Byte28 = 40, 41, 60, 61 (4/4)

	0	1	2	3	4	5	6	7
70	FCA::CWCSA0104							
	Slave 1 Cache Write Address (BYTE4)							
71	FCA::CRCSA00							
	Cache Read Address (BYTE0)							
72	FCA::CRCSA0104							
	Cache Read Address (BYTE1)							
73	FCA::CRCSA0104							
	Cache Read Address (BYTE2)							
74	FCA::CRCSA0104							
	Cache Read Address (BYTE3)							
75	FCA::CRCSA0104							
	Cache Read Address (BYTE4)							
76	Micro Information							
	CDEV#							
77	Micro Information							
	RDEV#							
78	Micro Information							
	RDEV#							
79	Micro Information							
	SCSI Command							
7A	Micro Information							
	LBA#(byte0)							
7B	Micro Information							
	LBA#(byte1)							
7C	Micro Information							
	LBA#(byte2)							
7D	Micro Information							
	LBA#(byte3)							
7E	Micro Information							
	Error Devided Result Code							
7F	Micro Information							
	CHK2 Detected Counter (Low)							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(8) Byte28 = 48 (1/4)

	0	1	2	3	4	5	6	7
40	FCA::CHK2G40							
	CC2 LA ERR	CC2 LBA ERR	CC2 LLRC ERR	CC3 LA ERR	CC3 LBA ERR	CC3 LLRC ERR	CC,S LA ERR	CC4 LBA ERR
41	FCA::CHK2G40							
	CC4 LLRC ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
42	FCA::TCSBC							
	TCSBC Counter(Cache Total Tansfer Subblock Number)							
43	FCA::TCSBC							
	TCSBC Counter(Cache Total Tansfer Subblock Number)							
44	FCA::BPRD							
	Cache Write Slot Pointer							
45	FCA::BPRD							
	Cache Write Segment Pointer							
46	FCA::LA2FEEX							
	LA Value of Start Subblock When LA Err Occurred (BYTE0)							
47	FCA::LA2FEEX							
	LA Value of LA Err Detected Subblock (BYTE0)							
48	FCA::LA2FEEX							
	Expected LA Value When LA Err Occurred (BYTE0)							
49	FCA::C2LA14M							
	CC2 LA Value (BYTE1)							
4A	FCA::C2LA14M							
	CC2 LA Value (BYTE2)							
4B	FCA::C2LA14M							
	CC2 LA Value (BYTE3)							
4C	FCA::C2LA14M							
	CC2 LA Value (BYTE4)							
4D	FCA::LA2FNC							
	Expected LA Value when When LA Err Occured (BYTE1)							
4E	FCA::LA2FNC							
	Expected LA Value When LA Err Occured (BYTE2)							
4F	FCA::LA2FNC							
	Expected LA Value When LA Err Occured (BYTE3)							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(8) Byte28 = 48 (2/4)

	0	1	2	3	4	5	6	7
50		FCA::LA2FNC						
		Expected LA Value When LA Err Occured (BYTE4)						
51		FCA::LA2INI						
		LA Value of Start Subblock When LA Err Occured (BYTE1)						
52		FCA::LA2INI						
		LA Value of Start Subblock When LA Err Occured (BYTE2)						
53		FCA::LA2INI						
		LA Value of Start Subblock When LA Err Occured (BYTE3)						
54		FCA::LA2INI						
		LA Value of Start Subblock When LA Err Occured (BYTE4)						
55		FCA::LA2ERR						
		LA Value of LA Err Detected Subblock (BYTE1)						
56		FCA::LA2ERR						
		LA Value of LA Err Detected Subblock (BYTE2)						
57		FCA::LA2ERR						
		LA Value of LA Err Detected Subblock (BYTE3)						
58		FCA::LA2ERR						
		LA Value of LA Err Detected Subblock (BYTE4)						
59		FCA::C2LBAM						
		CC2 LBAM Value (BYTE0)						
5A		FCA::C2LBA13M						
		CC2 LBAM Value (BYTE1)						
5B		FCA::C2LBA13M						
		CC2 LBAM Value (BYTE2)						
5C		FCA::C2LBA13M						
		CC2 LBAM Value (BYTE3)						
5D		FCA::CWCSA00						
		Slave 1 Cache Write Address (BYTE0)						
5E		FCA::CWCSA0104						
		Slave 1 Cache Write Address (BYTE1)						
5F		FCA::CWCSA0104						
		Slave 1 Cache Write Address (BYTE2)						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(8) Byte28 = 48 (3/4)

	0	1	2	3	4	5	6	7
60	FCA::CWCSA0104 Slave 1 Cache Write Address (BYTE3)							
61	FCA::CWCSA0104 Slave 1 Cache Write Address (BYTE4)							
62	FCA::BMPWT21 BPM0C Value When Writing to Cache							
63	FCA::BMPWT21 BPM0C Value When Writing to Cache							
64	FCA::BMPWT21 BPM0C Value When Writing to Cache							
65	FCA::BMPWT21 BPM0C Value When Writing to Cache							
66	FCA::SPMSW00 SPMSW00 Value							
67	FCA::SPMSW01 SPMSW01 Value							
68	FCA::SPMSW01 SPMSW01 Value							
69	FCA::SPMSW01 SPMSW01 Value							
6A	FCA::SPMSW01 SPMSW01 Value							
6B	FCA::PBFID PBF0 Side DMA ID							
6C	FCA::PBFID PBF0 Side DMA ID							
6D	FCA::PBFID PBF1 Side DMA ID							
6E	FCA::PBFID PBF1 Side DMA ID							
6F	FCA::SPREQAD PDEV ID							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(8) Byte28 = 48 (4/4)

	0	1	2	3	4	5	6	7
70		FCA::SPREQAD						
		QUE ID						
71		FCA::DPREQAD						
		PDEV ID						
72		FCA::DPREQAD						
		QUE ID						
73		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
74		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
75		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
76		Micro Information						
		CDEV#						
77		Micro Information						
		RDEV#						
78		Micro Information						
		RDEV#						
79		Micro Information						
		SCSI Command						
7A		Micro Information						
		LBA# (BYTE0)						
7B		Micro Information						
		LBA# (BYTE1)						
7C		Micro Information						
		LBA# (BYTE2)						
7D		Micro Information						
		LBA# (BYTE3)						
7E		Micro Information						
		Error Devided Result Code						
7F		Micro Information						
		CHK2 Detected Counter (Low)						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(9) Byte28 = 19 (1/4)

	0	1	2	3	4	5	6	7
40	FCA::CHK2G40							
	CC2 LA ERR	CC2 LBA ERR	CC2 LLRC ERR	CC3 LA ERR	CC3 LBA ERR	CC3 LLRC ERR	CC,S LA ERR	CC4 LBA ERR
41	FCA::CHK2G40							
	CC4 LLRC ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
42	FCA::TDSBC							
	TDSBC Counter(Drive Total Tansfer Subblock Number)							
43	FCA::TDSBC							
	TDSBC Counter(Drive Total Tansfer Subblock Number)							
44	FCA::BPRE							
	Cache Read Slot Pointer							
45	FCA::BPRE							
	Cache Read Segment Pointer							
46	FCA::LA3FEEX							
	LA Value of Start Subblock When LA Err Occurred (BYTE0)							
47	FCA::LA3FEEX							
	LA Value of LA Err Detected Subblock (BYTE0)							
48	FCA::C3PLRCM							
	CC3 PLRCM Value							
49	FCA::C3PLRCM							
	CC3 PLRCM Value							
4A	FCA::LA3FEEX							
	Expected LA Value When LA Err Occurred (BYTE0)							
4B	FCA::C3LA14M							
	CC3 LA Value (BYTE1)							
4C	FCA::C3LA14M							
	CC3 LA Value (BYTE2)							
4D	FCA::C3LA14M							
	CC3 LA Value (BYTE3)							
4E	FCA::C3LA14M							
	CC3 LA Value (BYTE4)							
4F	FCA::LA3FNC							
	Expected LA Value when When LA Err Occured (BYTE1)							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(9) Byte28 = 19 (2/4)

	0	1	2	3	4	5	6	7
50	FCA::LA3FNC Expected LA Value when When LA Err Occured (BYTE2)							
51	FCA::LA3FNC Expected LA Value when When LA Err Occured (BYTE3)							
52	FCA::LA3FNC Expected LA Value when When LA Err Occured (BYTE4)							
53	FCA::LA3INI LA Value of Start Subblock When LA Err Occured (BYTE1)							
54	FCA::LA3INI LA Value of Start Subblock When LA Err Occured (BYTE2)							
55	FCA::LA3INI LA Value of Start Subblock When LA Err Occured (BYTE3)							
56	FCA::LA3INI LA Value of Start Subblock When LA Err Occured (BYTE4)							
57	FCA::LA3ERR LA Value of LA Err Detected Subblock (BYTE1)							
58	FCA::LA3ERR LA Value of LA Err Detected Subblock (BYTE2)							
59	FCA::LA3ERR LA Value of LA Err Detected Subblock (BYTE3)							
5A	FCA::LA3ERR LA Value of LA Err Detected Subblock (BYTE4)							
5B	FCA::C3LBAM CC3 LBAM Value (BYTE0)							
5C	FCA::C3LBA13M CC3 LBAM Value (BYTE1)							
5D	FCA::C3LBA13M CC3 LBAM Value (BYTE2)							
5E	FCA::C3LBA13M CC3 LBAM Value (BYTE3)							
5F	FCA::CRCSA00 Cache Read Address (BYTE0)							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(9) Byte28 = 19 (3/4)

	0	1	2	3	4	5	6	7
60		FCA::CRCSA0104						
		Cache Read Address (BYTE1)						
61		FCA::CRCSA0104						
		Cache Read Address (BYTE2)						
62		FCA::CRCSA0104						
		Cache Read Address (BYTE3)						
63		FCA::CRCSA0104						
		Cache Read Address (BYTE4)						
64		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
65		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
66		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
67		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
68		FCA::SPMSR00						
		SPMSR00 Value						
69		FCA::SPMSR01						
		SPMSR01 Value						
6A		FCA::SPMSR01						
		SPMSR01 Value						
6B		FCA::SPMSR01						
		SPMSR01 Value						
6C		FCA::SPMSR01						
		SPMSR01 Value						
6D		FCA::CHSNSTS00						
	STATUS0 ERR	STATUS0 CARB ERR	STATUS0 CMA ERR	STATUS0 Reserved	STATUS0 CMA STATUS NG	STATUS0 CMA FIFO MODE	STATUS0 CMA WARNING	STATUS0 Reserved
6E		FCA::CHSNSTS00						
	STATUS0 Reserved	STATUS0 PATH ID			STATUS0 Reserved	STATUS0 CACHE P/K#		
6F		FCA::CHSNSTS00						
	STATUS0 Reserved	STATUS0 PATH ID			STATUS0 Reserved	STATUS0 CACHE P/K#		

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(9) Byte28 = 19 (4/4)

	0	1	2	3	4	5	6	7
70		FCA::CHSNSTS00						
	STATUS0 ERR	STATUS0 CARB ERR	STATUS0 CMA ERR	STATUS0 Reserved	STATUS0 CMA STATUS NG	STATUS0 CMA FIFO MODE	STATUS0 CMA WARNING	STATUS0 Reserved
71		FCA::CHSNSTS01						
	STS0 CARB PXDR INDPE	STS0 CARB PXLRCE	STS0 CARB PXDR OUTDPE	STS0 CARB PXOR INDPE	STS0 CARB PXTME	STS0 CARB ABTE	STS0 CARB PXHE	STS0 CARB PXMAE
72		FCA::CHSNSTS01						
	STS0 CARB CXOR INDPE	STS0 CARB CXDR INDPE	STS0 CARB CXLRCE	STS0 CARB CXDR OUTDPE	STS0 CARB CXTME	STS0 CARB CXHE	STS0 CARB Reserved	STS0 CARB Reserved
73		FCA::CHSNSTS01						
	STS0 CMA BOARD DISABLE	STS0 CMA MEM NOT RDY	STS0 CMA MODULE DISABLE	STS0 CMA MEM BACKUP MODE	STS0 CMA DIAG UMNT	STS0 CMA SP UMNT	STS0 CMA REG CODE ERR	STS0 CMA INVLD COM
74		FCA::CHSNSTS01						
	STS0 CMA PKID PEER	STS0 CMA GSLRCER	STS0 CMA DT PKT ER	STS0 CMA CMD PKT ER	STS0 CMA MODULE ER	STS0 CMA HCTL ER	STS0 CMA MCTL ER	STS0 CMA BRD ER
75		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
76		Micro Information						
		CDEV#						
77		Micro Information						
		RDEV#						
78		Micro Information						
		RDEV#						
79		Micro Information						
		SCSI Command						
7A		Micro Information						
		LBA# (BYTE0)						
7B		Micro Information						
		LBA# (BYTE1)						
7C		Micro Information						
		LBA# (BYTE2)						
7D		Micro Information						
		LBA# (BYTE3)						
7E		Micro Information						
		Error Devided Result Code						
7F		Micro Information						
		CHK2 Detected Counter (Low)						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2)

	0	1	2	3	4	5	6	7
00	Time Stamp							
|								
05								
06	Format Message							
07	P/K Type		Processer ID					
08	System Error Code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	HOST Report	SVP Report	Force Log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	DRR#		RCU#			
10	LDEV#							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV#							
15								
16	Internal SSB Log Number							
17								
18	Related Failure Log Number							
19								
1A	Related SIM Log Number							
1B								
1C	Related SSB Log Number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTRL no.	DKU Physical Device no.				
25	Cylinder Address (Low)							
26	Cylinder Address (High)				Head Address			
27	Format (x‘8’)				Message (x‘B’)			
28	SubCode							
29	Detail Information (See Following Pages.)							
|								
31								
32	Module ID							
33	Routine ID							
34	P/K ID				Message Code (x‘0’)			
35	SSID for Self Subsystem							
36	Symptom Code (x‘FF89’:LDEV Type=DKU87I / x‘EF89’: LDEV Type=DKU86I)							
37								
38	Log and Message Control (x‘00’)							
39	Program Action Control (x‘00’)							
3A	Configuration Information							
3B								
3C	Not Used							
3D	Cylinder Address							
3E								
3F	Head Address							
40	Detail Information (See Following Pages.)							
|								
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(1) Byte28 = 10

	0	1	2	3	4	5	6	7
28	SubCode (x'10' : DRR CHK2B - DRR DATA ERROR)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Excuting	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Excuting
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRESTA2							
	P0 SEQ6 PARITY ERR	P1 SEQ6 PARITY ERR	SLRC CAL-DT PARITY ERR	SLRC DT PARITY ERR	AC PLRC-GEN DT PARITY ERR0	AC PLRC-GEN DT PARITY ERR1	DT PLRC-GEN DT PARITY ERR0	DT PLRC-GEN DT PARITY ERR1
2C	DRR::DRESTA3							
	STATUS0 PLRC ERR	STATUS0 INV-PLRC ERR	STATUS1 PLRC ERR	STATUS1 INV-PLRC ERR	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE ERR	LA DT PARITY ERR
2D	DRR::DRESTA3							
	DM0 DT0 PARITY ERR	DM0 DT1 PARITY ERR	DM0 DT2 PARITY ERR	DM0 DT3 PARITY ERR	DM0 DT4 PARITY ERR	DM0 DT5 PARITY ERR	DM0 DT6 PARITY ERR	DM0 DT7 PARITY ERR
2E	DRR::DRESTA4							
	ELA/CLA DT PARITY ERR	CMD PARITY ERR AT64-CMD	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	SLAVE1 CMD-A ADR PARITY ERR	SLAVE1 CMD-B ADR PARITY ERR	SLAVE2 CMD-A ADR PARITY ERR	SLAVE2 CMD-B ADR PARITY ERR
2F	DRR::DRESTA4							
	STATUS0 DT0 PARITY ERR	STATUS0 DT1 PARITY ERR	STATUS0 DT2 PARITY ERR	STATUS0 DT3 PARITY ERR	STATUS0 DT4 PARITY ERR	STATUS0 DT5 PARITY ERR	STATUS0 DT6 PARITY ERR	STATUS0 DT7 PARITY ERR
30	DRR::DRESTA5							
	STATUS1 DT0 PARITY ERR	STATUS1 DT1 PARITY ERR	STATUS1 DT2 PARITY ERR	STATUS1 DT3 PARITY ERR	STATUS1 DT4 PARITY ERR	STATUS1 DT5 PARITY ERR	STATUS1 DT6 PARITY ERR	STATUS1 DT7 PARITY ERR
31	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(2) Byte28 = 11

	0	1	2	3	4	5	6	7
28	SubCode (x'11' : DRR CHK2B - CHSN0 DATA ERROR)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Excuting	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Excuting
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRESTA5							
	P0 TX DT0 PARITY ERR	P0 TX DT1 PARITY ERR	P0 TX DT2 PARITY ERR	P0 TX DT3 PARITY ERR	P0 TX DT4 PARITY ERR	P0 TX DT5 PARITY ERR	P0 TX DT6 PARITY ERR	P0 TX DT7 PARITY ERR
2C	DRR::DRESTA6							
	P0 RX DT0 PARITY ERR	P0 RX DT1 PARITY ERR	P0 RX DT2 PARITY ERR	P0 RX DT3 PARITY ERR	P0 RX DT4 PARITY ERR	P0 RX DT5 PARITY ERR	P0 RX DT6 PARITY ERR	P0 RX DT7 PARITY ERR
2D	DRR::DRESTA6							
	P0 TXX I-DT0 PARITY ERR	P0 TXX I-DT1 PARITY ERR	P0 TXX O-DT0 PARITY ERR	P0 TXX O-DT1 PARITY ERR	P1 TXX I-DT0 PARITY ERR	P1 TXX I-DT1 PARITY ERR	P1 TXX O-DT0 PARITY ERR	P1 TXX O-DT1 PARITY ERR
2E	DRR::DRESTAB							
	P0 AC PLRC ERR	P0 DT PLRC ERR	P0 STATUS0 PLRC ERR	P0 STATUS1 PLRC ERR	P0 AC PLRC- IV ERR	P0 DT PLRC- IV ERR	P0 STATUS0 PLRC-IV ERR	P0 STATUS1 PLRC-IV ERR
2F	DRR::DRESTAB							
	P0 AC END CODE ERR	P0 DT END CODE ERR	P0 STATUS0 END CODE ERR	P0 STATUS1 END CODE ERR	P0 SLRC CHECK ERR	P0 SLRC CAL DT ERR	P0 SLRC RD DT ERR	P0 SBLK DCNT ERR
30	DRR::DRESTA8							
	LA0/LA1 COMP ERR	LA2 COMP ERR	SYND (ECC) ERR	DT END CODE ERR	P0 ERRINT	P1 ERRINT	STATUS0 CARB/ CMA ERR	STATUS1 CARB/ CMA ERR
31	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(3) Byte28 = 12

	0	1	2	3	4	5	6	7
28	SubCode (x'12' : DRR CHK2B - CHSN1 DATA ERROR)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Excuting	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Excuting
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRESTA6							
	P0 TXX I-DT0 PARITY ERR	P0 TXX I-DT1 PARITY ERR	P0 TXX O-DT0 PARITY ERR	P0 TXX O-DT1 PARITY ERR	P1 TXX I-DT0 PARITY ERR	P1 TXX I-DT1 PARITY ERR	P1 TXX O-DT0 PARITY ERR	P1 TXX O-DT1 PARITY ERR
2C	DRR::DRESTA7							
	P1 TX DT0 PARITY ERR	P1 TX DT1 PARITY ERR	P1 TX DT2 PARITY ERR	P1 TX DT3 PARITY ERR	P1 TX DT4 PARITY ERR	P1 TX DT5 PARITY ERR	P1 TX DT6 PARITY ERR	P1 TX DT7 PARITY ERR
2D	DRR::DRESTA7							
	P1 RX DT0 PARITY ERR	P1 RX DT1 PARITY ERR	P1 RX DT2 PARITY ERR	P1 RX DT3 PARITY ERR	P1 RX DT4 PARITY ERR	P1 RX DT5 PARITY ERR	P1 RX DT6 PARITY ERR	P1 RX DT7 PARITY ERR
2E	DRR::DRESTAC							
	P1 AC PLRC ERR	P1 DT PLRC ERR	P1 STATUS0 PLRC ERR	P1 STATUS1 PLRC ERR	P1 AC PLRC-IV ERR	P1 DT PLRC-IV ERR	P1 STATUS0 PLRC-IV ERR	P1 STATUS1 PLRC-IV ERR
2F	DRR::DRESTAC							
	P1 AC END CODE ERR	P1 DT END CODE ERR	P1 STATUS0 END CODE ERR	P1 STATUS1 END CODE ERR	P1 SLRC CHECK ERR	P1 SLRC CAL DT ERR	P1 SLRC RD DT ERR	P1 SBLK DCNT ERR
30	DRR::DRESTA8							
	LA0/LA1 COMP ERR	LA2 COMP ERR	SYND (ECC) ERR	DT END CODE ERR	P0 ERRINT	P1 ERRINT	STATUS0 CARB/ CMA ERR	STATUS1 CARB/ CMA ERR
31	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(4) Byte28 = 13

	0	1	2	3	4	5	6	7
28	SubCode (x'13' : DRR CHK2B - DRR&CHSN0 DATA ERROR)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Excuting	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Excuting
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRESTA2							
	P0 SEQ6 PARITY ERR	P1 SEQ6 PARITY ERR	SLRC CAL-DT PARITY ERR	SLRC DT PARITY ERR	AC PLRC-GEN DT PARITY ERR0	AC PLRC-GEN DT PARITY ERR1	DT PLRC-GEN DT PARITY ERR0	DT PLRC-GEN DT PARITY ERR1
2C	DRR::DRESTA3							
	STATUS0 PLRC ERR	STATUS0 INV-PLRC ERR	STATUS1 PLRC ERR	STATUS1 INV-PLRC ERR	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE ERR	LA DT PARITY ERR
2D	DRR::DRESTA3							
	DM0 DT0 PARITY ERR	DM0 DT1 PARITY ERR	DM0 DT2 PARITY ERR	DM0 DT3 PARITY ERR	DM0 DT4 PARITY ERR	DM0 DT5 PARITY ERR	DM0 DT6 PARITY ERR	DM0 DT7 PARITY ERR
2E	DRR::DRESTA4							
	ELA/CLA DT PARITY ERR	CMD PARITY ERR AT64-CMD	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	SLAVE1 CMD-A ADR PARITY ERR	SLAVE1 CMD-B ADR PARITY ERR	SLAVE2 CMD-A ADR PARITY ERR	SLAVE2 CMD-B ADR PARITY ERR
2F	DRR::DRESTA4							
	STATUS0 DT0 PARITY ERR	STATUS0 DT1 PARITY ERR	STATUS0 DT2 PARITY ERR	STATUS0 DT3 PARITY ERR	STATUS0 DT4 PARITY ERR	STATUS0 DT5 PARITY ERR	STATUS0 DT6 PARITY ERR	STATUS0 DT7 PARITY ERR
30	DRR::DRESTA5							
	STATUS1 DT0 PARITY ERR	STATUS1 DT1 PARITY ERR	STATUS1 DT2 PARITY ERR	STATUS1 DT3 PARITY ERR	STATUS1 DT4 PARITY ERR	STATUS1 DT5 PARITY ERR	STATUS1 DT6 PARITY ERR	STATUS1 DT7 PARITY ERR
31	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(5) Byte28 = 14

	0	1	2	3	4	5	6	7
28	SubCode (x'14' : DRR CHK2B - DRR&CHSN1 DATA ERROR)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Excuting	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Excuting
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRESTA2							
	P0 SEQ6 PARITY ERR	P1 SEQ6 PARITY ERR	SLRC CAL-DT PARITY ERR	SLRC DT PARITY ERR	AC PLRC-GEN DT PARITY ERR0	AC PLRC-GEN DT PARITY ERR1	DT PLRC-GEN DT PARITY ERR0	DT PLRC-GEN DT PARITY ERR1
2C	DRR::DRESTA3							
	STATUS0 PLRC ERR	STATUS0 INV-PLRC ERR	STATUS1 PLRC ERR	STATUS1 INV-PLRC ERR	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE ERR	LA DT PARITY ERR
2D	DRR::DRESTA3							
	DM0 DT0 PARITY ERR	DM0 DT1 PARITY ERR	DM0 DT2 PARITY ERR	DM0 DT3 PARITY ERR	DM0 DT4 PARITY ERR	DM0 DT5 PARITY ERR	DM0 DT6 PARITY ERR	DM0 DT7 PARITY ERR
2E	DRR::DRESTA4							
	ELA/CLA DT PARITY ERR	CMD PARITY ERR AT 64-CMD	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	SLAVE1 CMD-A ADR PARITY ERR	SLAVE1 CMD-B ADR PARITY ERR	SLAVE2 CMD-A ADR PARITY ERR	SLAVE2 CMD-B ADR PARITY ERR
2F	DRR::DRESTA4							
	STATUS0 DT0 PARITY ERR	STATUS0 DT1 PARITY ERR	STATUS0 DT2 PARITY ERR	STATUS0 DT3 PARITY ERR	STATUS0 DT4 PARITY ERR	STATUS0 DT5 PARITY ERR	STATUS0 DT6 PARITY ERR	STATUS0 DT7 PARITY ERR
30	DRR::DRESTA5							
	STATUS1 DT0 PARITY ERR	STATUS1 DT1 PARITY ERR	STATUS1 DT2 PARITY ERR	STATUS1 DT3 PARITY ERR	STATUS1 DT4 PARITY ERR	STATUS1 DT5 PARITY ERR	STATUS1 DT6 PARITY ERR	STATUS1 DT7 PARITY ERR
31	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(6) Byte28 =20

	0	1	2	3	4	5	6	7
28	SubCode (x'20' : DRR CHK2B - DRR DATA ERROR2)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Excuting	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Excuting
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRESTA2							
	P0 SEQ6 PARITY ERR	P1 SEQ6 PARITY ERR	SLRC CAL-DT PARITY ERR	SLRC DT PARITY ERR	AC PLRC-GEN DT PARITY ERR0	AC PLRC-GEN DT PARITY ERR1	DT PLRC-GEN DT PARITY ERR0	DT PLRC-GEN DT PARITY ERR1
2C	DRR::DRESTA3							
	STATUS0 PLRC ERR	STATUS0 INV-PLRC ERR	STATUS1 PLRC ERR	STATUS1 INV-PLRC ERR	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE ERR	LA DT PARITY ERR
2D	DRR::DRESTA3							
	DM0 DT0 PARITY ERR	DM0 DT1 PARITY ERR	DM0 DT2 PARITY ERR	DM0 DT3 PARITY ERR	DM0 DT4 PARITY ERR	DM0 DT5 PARITY ERR	DM0 DT6 PARITY ERR	DM0 DT7 PARITY ERR
2E	DRR::DRESTA4							
	ELA/CLA DT PARITY ERR	CMD PARITY ERR AT 64-CMD	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	SLAVE1 CMD-A ADR PARITY ERR	SLAVE1 CMD-B ADR PARITY ERR	SLAVE2 CMD-A ADR PARITY ERR	SLAVE2 CMD-B ADR PARITY ERR
2F	DRR::DRESTA4							
	STATUS0 DT0 PARITY ERR	STATUS0 DT1 PARITY ERR	STATUS0 DT2 PARITY ERR	STATUS0 DT3 PARITY ERR	STATUS0 DT4 PARITY ERR	STATUS0 DT5 PARITY ERR	STATUS0 DT6 PARITY ERR	STATUS0 DT7 PARITY ERR
30	DRR::DRESTA5							
	STATUS1 DT0 PARITY ERR	STATUS1 DT1 PARITY ERR	STATUS1 DT2 PARITY ERR	STATUS1 DT3 PARITY ERR	STATUS1 DT4 PARITY ERR	STATUS1 DT5 PARITY ERR	STATUS1 DT6 PARITY ERR	STATUS1 DT7 PARITY ERR
31	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(7) Byte28 =30

	0	1	2	3	4	5	6	7
28	SubCode (x'30' : DRR CHK2A - DRR CTL ERROR)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Excuting	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Excuting
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRERR							
	DRR CTL ERR	P0 CTL ERR	P1 CTL ERR	DRR DT ERR	P0 DT ERR	P1 DT ERR	STATUS0 CARB/ CMA ERR	STATUS1 CARB/ CMA ERR
2C	DRR::DRESTA0							
	CMD A/B SEQ ERR	TRANS SEQ ERR	DRB-CBUF SEQ ERR	CBUF-DM0 SEQ ERR	DM0-BUFF SEQ ERR	CBUF-CHSN SEQ ERR	CBUF→ PBUF WR-PNT PARITY ERR	CBUF→ DM0 PK-CNT PARITY ERR
2D	DRR::DRESTA0							
	DRB→ CBUF PK-CNT PARITY ERR	CBUF→ PBUF PK-CNT PARITY ERR	PBUF→ CBUF PK-CNT PARITY ERR	TL CNT PARITY ERR	PL CNT PARITY ERR	TL/PL PRM ERR CMD A	TL/PL PRM ERR CMD B	DRB WT-ADR CNT PARITY ERR
2E	DRR::DRESTA1							
	DRB RD-ADR CNT PARITY ERR	SB-BLK DT-CNT PARITY ERR	C0BUF WT-ADR CNT PARITY ERR	C0BUF RD-ADR CNT PARITY ERR	C1BUF WT-ADR CNT PARITY ERR	C1BUF RD-ADR CNT PARITY ERR	BMP0 DT PERR	BMP1 DT PERR
2F	DRR::DRESTA1							
	P0 SYNC0 PNT PARITY ERR	P0 SYNC1 PNT PARITY ERR	P0 SYNC0 CLOCK PARITY ERR	P0 SYNC1 CLOCK PARITY ERR	P0 TX SEQ ERR	P0 TX RD PNT PARITY ERR	P0 RX SEQ ERR	P0 RX RD PNT PARITY ERR
30	DRR::DRESTA2							
	P1 SYNC0 PNT PARITY ERR	P1 SYNC1 PNT PARITY ERR	P1 SYNC0 CLOCK PARITY ERR	P1 SYNC1 CLOCK PARITY ERR	P1 TX SEQ ERR	P1 TX RD PNT PARITY ERR	P1 RX SEQ ERR	P1 RX RD PNT PARITY ERR
31	DRR::DRESTA2							
	P0 SEQ PARITY ERR	P1 SEQ PARITY ERR	SLRC CAL-DT PARITY ERR	SLRC DT PARITY ERR	AC PLRC-GEN DT PARITY ERR0	AC PLRC-GEN DT PARITY ERR1	DT PLRC-GEN DT PARITY ERR0	DT PLRC-GEN DT PARITY ERR1

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(8) Byte28 =40

	0	1	2	3	4	5	6	7
28	SubCode (x‘40’ : DRR CHK2D - ARBITER TIMER ERROR)							
29	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE
2A	DRR::P0ETM0							
	P0 ENT-TIMER (High)							
2B	DRR::P0ETM0							
	P0 ENT-TIMER (High)							
2C	DRR::P0ETM1							
	P0 ENT-TIMER (Low)							
2D	DRR::P0ETM1							
	P0 ENT-TIMER (Low)							
2E	DRR::P0ATM0							
	P0 ACK-TIMER (High)							
2F	DRR::P0ATM0							
	P0 ACK-TIMER (High)							
30	DRR::P0ATM1							
	P0 ACK-TIMER (Low)							
31	DRR::P0ATM1							
	P0 ACK-TIMER (Low)							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(8) Byte28 =A0

	0	1	2	3	4	5	6	7
28	SubCode (x'A0' : DRR NO ERR - TIME OVER)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Excuting	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Excuting
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRESTA2							
	P0 SEQ6 PARITY ERR	P1 SEQ6 PARITY ERR	SLRC CAL-DT PARITY ERR	SLRC DT PARITY ERR	AC PLRC-GEN DT PARITY ERR0	AC PLRC-GEN DT PARITY ERR1	DT PLRC-GEN DT PARITY ERR0	DT PLRC-GEN DT PARITY ERR1
2C	DRR::DRESTA3							
	STATUS0 PLRC ERR	STATUS0 INV-PLRC ERR	STATUS1 PLRC ERR	STATUS1 INV-PLRC ERR	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE ERR	LA DT PARITY ERR
2D	DRR::DRESTA3							
	DM0 DT0 PARITY ERR	DM0 DT1 PARITY ERR	DM0 DT2 PARITY ERR	DM0 DT3 PARITY ERR	DM0 DT4 PARITY ERR	DM0 DT5 PARITY ERR	DM0 DT6 PARITY ERR	DM0 DT7 PARITY ERR
2E	DRR::DRESTA4							
	ELA/CLA DT PARITY ERR	CMD PARITY ERR AT 64-CMD	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	SLAVE1 CMD-A ADR PARITY ERR	SLAVE1 CMD-B ADR PARITY ERR	SLAVE2 CMD-A ADR PARITY ERR	SLAVE2 CMD-B ADR PARITY ERR
2F	DRR::DRESTA4							
	STATUS0 DT0 PARITY ERR	STATUS0 DT1 PARITY ERR	STATUS0 DT2 PARITY ERR	STATUS0 DT3 PARITY ERR	STATUS0 DT4 PARITY ERR	STATUS0 DT5 PARITY ERR	STATUS0 DT6 PARITY ERR	STATUS0 DT7 PARITY ERR
30	DRR::DRESTA5							
	STATUS1 DT0 PARITY ERR	STATUS1 DT1 PARITY ERR	STATUS1 DT2 PARITY ERR	STATUS1 DT3 PARITY ERR	STATUS1 DT4 PARITY ERR	STATUS1 DT5 PARITY ERR	STATUS1 DT6 PARITY ERR	STATUS1 DT7 PARITY ERR
31	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(9) Byte28 =B0

	0	1	2	3	4	5	6	7
28	SubCode (x'B0' : DRR CHK2C)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Excuting	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Excuting
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRESTA2							
	P0 SEQ6 PARITY ERR	P1 SEQ6 PARITY ERR	SLRC CAL-DT PARITY ERR	SLRC DT PARITY ERR	AC PLRC-GEN DT PARITY ERR0	AC PLRC-GEN DT PARITY ERR1	DT PLRC-GEN DT PARITY ERR0	DT PLRC-GEN DT PARITY ERR1
2C	DRR::DRESTA3							
	STATUS0 PLRC ERR	STATUS0 INV-PLRC ERR	STATUS1 PLRC ERR	STATUS1 INV-PLRC ERR	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE ERR	LA DT PARITY ERR
2D	DRR::DRESTA3							
	DM0 DT0 PARITY ERR	DM0 DT1 PARITY ERR	DM0 DT2 PARITY ERR	DM0 DT3 PARITY ERR	DM0 DT4 PARITY ERR	DM0 DT5 PARITY ERR	DM0 DT6 PARITY ERR	DM0 DT7 PARITY ERR
2E	DRR::DRESTA4							
	ELA/CLA DT PARITY ERR	CMD PARITY ERR AT 64-CMD	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	SLAVE1 CMD-A ADR PARITY ERR	SLAVE1 CMD-B ADR PARITY ERR	SLAVE2 CMD-A ADR PARITY ERR	SLAVE2 CMD-B ADR PARITY ERR
2F	DRR::DRESTA4							
	STATUS0 DT0 PARITY ERR	STATUS0 DT1 PARITY ERR	STATUS0 DT2 PARITY ERR	STATUS0 DT3 PARITY ERR	STATUS0 DT4 PARITY ERR	STATUS0 DT5 PARITY ERR	STATUS0 DT6 PARITY ERR	STATUS0 DT7 PARITY ERR
30	DRR::DRESTA5							
	STATUS1 DT0 PARITY ERR	STATUS1 DT1 PARITY ERR	STATUS1 DT2 PARITY ERR	STATUS1 DT3 PARITY ERR	STATUS1 DT4 PARITY ERR	STATUS1 DT5 PARITY ERR	STATUS1 DT6 PARITY ERR	STATUS1 DT7 PARITY ERR
31	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(10) Byte28 =B1

	0	1	2	3	4	5	6	7
28	SubCode (x'B1' : P0 CHK2C)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Excuting	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Excuting
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRESTA2							
	P0 SEQ6 PARITY ERR	P1 SEQ6 PARITY ERR	SLRC CAL-DT PARITY ERR	SLRC DT PARITY ERR	AC PLRC-GEN DT PARITY ERR0	AC PLRC-GEN DT PARITY ERR1	DT PLRC-GEN DT PARITY ERR0	DT PLRC-GEN DT PARITY ERR1
2C	DRR::DRESTA3							
	STATUS0 PLRC ERR	STATUS0 INV-PLRC ERR	STATUS1 PLRC ERR	STATUS1 INV-PLRC ERR	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE ERR	LA DT PARITY ERR
2D	DRR::DRESTA3							
	DM0 DT0 PARITY ERR	DM0 DT1 PARITY ERR	DM0 DT2 PARITY ERR	DM0 DT3 PARITY ERR	DM0 DT4 PARITY ERR	DM0 DT5 PARITY ERR	DM0 DT6 PARITY ERR	DM0 DT7 PARITY ERR
2E	DRR::DRESTA4							
	ELA/CLA DT PARITY ERR	CMD PARITY ERR AT 64-CMD	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	SLAVE1 CMD-A ADR PARITY ERR	SLAVE1 CMD-B ADR PARITY ERR	SLAVE2 CMD-A ADR PARITY ERR	SLAVE2 CMD-B ADR PARITY ERR
2F	DRR::DRESTA4							
	STATUS0 DT0 PARITY ERR	STATUS0 DT1 PARITY ERR	STATUS0 DT2 PARITY ERR	STATUS0 DT3 PARITY ERR	STATUS0 DT4 PARITY ERR	STATUS0 DT5 PARITY ERR	STATUS0 DT6 PARITY ERR	STATUS0 DT7 PARITY ERR
30	DRR::DRESTA5							
	STATUS1 DT0 PARITY ERR	STATUS1 DT1 PARITY ERR	STATUS1 DT2 PARITY ERR	STATUS1 DT3 PARITY ERR	STATUS1 DT4 PARITY ERR	STATUS1 DT5 PARITY ERR	STATUS1 DT6 PARITY ERR	STATUS1 DT7 PARITY ERR
31	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(10) Byte28 =B2

	0	1	2	3	4	5	6	7
28	SubCode (x'B2' : P1 CHK2C)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Excuting	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Excuting
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRESTA2							
	P0 SEQ6 PARITY ERR	P1 SEQ6 PARITY ERR	SLRC CAL-DT PARITY ERR	SLRC DT PARITY ERR	AC PLRC-GEN DT PARITY ERR0	AC PLRC-GEN DT PARITY ERR1	DT PLRC-GEN DT PARITY ERR0	DT PLRC-GEN DT PARITY ERR1
2C	DRR::DRESTA3							
	STATUS0 PLRC ERR	STATUS0 INV-PLRC ERR	STATUS1 PLRC ERR	STATUS1 INV-PLRC ERR	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE ERR	LA DT PARITY ERR
2D	DRR::DRESTA3							
	DM0 DT0 PARITY ERR	DM0 DT1 PARITY ERR	DM0 DT2 PARITY ERR	DM0 DT3 PARITY ERR	DM0 DT4 PARITY ERR	DM0 DT5 PARITY ERR	DM0 DT6 PARITY ERR	DM0 DT7 PARITY ERR
2E	DRR::DRESTA4							
	ELA/CLA DT PARITY ERR	CMD PARITY ERR AT64-CMD	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	SLAVE1 CMD-A ADR PARITY ERR	SLAVE1 CMD-B ADR PARITY ERR	SLAVE2 CMD-A ADR PARITY ERR	SLAVE2 CMD-B ADR PARITY ERR
2F	DRR::DRESTA4							
	STATUS0 DT0 PARITY ERR	STATUS0 DT1 PARITY ERR	STATUS0 DT2 PARITY ERR	STATUS0 DT3 PARITY ERR	STATUS0 DT4 PARITY ERR	STATUS0 DT5 PARITY ERR	STATUS0 DT6 PARITY ERR	STATUS0 DT7 PARITY ERR
30	DRR::DRESTA5							
	STATUS1 DT0 PARITY ERR	STATUS1 DT1 PARITY ERR	STATUS1 DT2 PARITY ERR	STATUS1 DT3 PARITY ERR	STATUS1 DT4 PARITY ERR	STATUS1 DT5 PARITY ERR	STATUS1 DT6 PARITY ERR	STATUS1 DT7 PARITY ERR
31	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte40-7F Detail
(1) Byte28 = 10, 20, 30, 40, A0, B0 (1/4)

	0	1	2	3	4	5	6	7
40		MMC::RCVINT						
	SYSRST Interrupt Monitor	SELRST Interrupt Monitor	CHK1A Interrupt Monitor	CHK1B Interrupt Monitor	SMP Interrupt Monitor	LAN/SIO Interrupt Monitor	CHA/DRR Interrupt Monitor	ADP/SCA0 Interrupt Monitor
41		MMC::RCVINT						
	(RSV)	CHK3 Interrupt Monitor	(RSV)	SCA1 Interrupt Monitor	SCA2 Interrupt Monitor	SCA3 Interrupt Monitor	SCA4 Interrupt Monitor	SCA5 Interrupt Monitor
42		DRR::DRMODE1						
	DRR CUDG MODE	DRR SYSTEM CLK MASK	DRR FORCE ERR	(RSV)	(RSV)	DRB W/R ENABLE	SLRC CHK MASK	SUBBLOCK DT-NO
43		DRR::DRMODE1						
	64-CMD MODE	SLAVE 2 ADR SEL	DATA ERR REPORT ENABLE	CHSN ABORT	(RSV)	RNGOSC ENABLE	DRR ABORT	DRR CHK2RST ON
44		DRR::DRMODE5						
	C PATH#00 ENABLE	C PATH#01 ENABLE	C PATH#02 ENABLE	C PATH#03 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
45		DRR::DRMODE5						
	C PATH#10 ENABLE	C PATH#11 ENABLE	C PATH#12 ENABLE	C PATH#13 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
46		DRR::CMD0A						
	CMD A SLRC CHK	(RSV)	(RSV)	CMD A SP MODE	CMD A DIAG MODE	(RSV)	(RSV)	(RSV)
47		DRR::CMD0A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
48		DRR::ADR0A						
		CMD A Slave 1 Cache Transfer Address (BYTE0)						
49		DRR::ADR0A						
		CMD A Slave 2 Cache Transfer Address (BYTE0)						
4A		DRR::ADR1A						
		CMD A Slave 1 Cache Transfer Address (BYTE1)						
4B		DRR::ADR3A						
		CMD A Slave 2 Cache Transfer Address (BYTE1)						
4C		DRR::TRMDA						
	CMD A SYND CHK	(RSV)	CMD A MRCF FUNCTION	CMD A DOUBLE WT MODE	CMD A Transfer Command			
4D		DRR::TRMDA						
	LA0(LBA) COMP CHK ENABLE	LA1 COMP CHK ENABLE	LA2 COMP CHK ENABLE	(RSV)	EXLA COUNT UP STOP	(RSV)	(RSV)	(RSV)
4E		DRR::LA0A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4F		DRR::LA0A						
		CMD A Expect LA Value (BYTE0)						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte40-7F Detail
(1) Byte28 = 10, 20, 30, 40, A0, B0 (2/4)

	0	1	2	3	4	5	6	7
50		DRR::LA1A						
		CMD A Expect LA Value (BYTE1)						
51		DRR::LA1A						
		CMD A Expect LA Value (BYTE2)						
52		DRR::LA2A						
		CMD A Expect LA Value (BYTE3)						
53		DRR::LA2A						
		CMD A Expect LA Value (BYTE4)						
54		DRR::CMD0B						
	CMD B SLRC CHK	(RSV)	(RSV)	CMD B SP MODE	CMD B DIAG MODE	(RSV)	(RSV)	(RSV)
55		DRR::CMD0B						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
56		DRR::ADR0B						
		CMD B Slave 1 Cache Transfer Address (BYTE0)						
57		DRR::ADR0B						
		CMD B Slave 2 Cache Transfer Address (BYTE0)						
58		DRR::ADR1B						
		CMD B Slave 1 Cache Transfer Address (BYTE1)						
59		DRR::ADR3B						
		CMD B Slave 2 Cache Transfer Address (BYTE1)						
5A		DRR::TRMDB						
	CMD B SYND CHK	(RSV)	CMD B MRCF FUNCTION	CMD B DOUBLE WT MODE	CMD B Transfer Command			
5B		DRR::TRMDB						
	LA0(LBA) COMP CHK ENABLE	LA1 COMP CHK ENABLE	LA2 COMP CHK ENABLE	(RSV)	EXLA COUNT UP STOP	(RSV)	(RSV)	(RSV)
5C		DRR::LA0B						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5D		DRR::LA0B						
		CMD B Expect LA Value (BYTE0)						
5E		DRR::LA1B						
		CMD B Expect LA Value (BYTE1)						
5F		DRR::LA1B						
		CMD B Expect LA Value (BYTE2)						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte40-7F Detail
(1) Byte28 = 10, 20, 30, 40, A0, B0 (3/4)

	0	1	2	3	4	5	6	7
60		DRR::LA2B						
		CMD B Expect LA Value (BYTE3)						
61		DRR::LA2B						
		CMD B Expect LA Value (BYTE4)						
62		DRR::RLALR0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
63		DRR::RLALR0						
		LA Value When LA ERR Occured (BYTE0)						
64		DRR::RLALR1						
		LA Value When LA ERR Occured (BYTE1)						
65		DRR::RLALR1						
		LA Value When LA ERR Occured (BYTE2)						
66		DRR::RLALR2						
		LA Value When LA ERR Occured (BYTE3)						
67		DRR::RLALR2						
		LA Value When LA ERR Occured (BYTE4)						
68		DRR::D64CNTM						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	Command Pointer(High)	
69		DRR::D64CNTM						
		Command Pointer(Low)						
6A		DRR::DRSEQM						
		DRSEQM						
6B		DRR::PBSEQM						
		PBSEQM						
6C		DRR::DMISQMREG						
		DMISQMREG						
6D		DRR::TRISQMREG						
		TRISQMREG						
6E		DRR::P0TXSQM						
		P0TXSQM						
6F		DRR::P0RXSQM						
		P0RXSQM						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte40-7F Detail
(1) Byte28 = 10, 20, 30, 40, A0, B0 (4/4)

	0	1	2	3	4	5	6	7
70		DRR::P1TXSQM						
		P1TXSQM						
71		DRR::P1RXSQM						
		P1TXSQM						
72		DRR::DRREV						
	QDTA FLAG (1:QDTA)	(RSV)	MP# '00':MP_A '01':MP_B '02':MP_A '03':MP_B		LSI Rev.			
73		DRR::DRREV						
	SELF MP ALARM	SELF MP MESSAGE	SELF MP CUDG3A FAIL	SELF MP CUDG3B FAIL	LSIMP ALARM	LSIMP MESSAGE	LSIMP CUDG3A FAIL	LSIMP CUDG3B FAIL
74		DRR::STATS						
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Excuting	CMD B Transfer END	(RSV)	CMD B Transfer Start	CMD B Transfer Excuting
75		DRR::STATS						
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	ABORT Detected	Force Err Detected
76		DRR::DRESTAD						
	ARB SEQ PARITY ERR (M)	ARB SEQ PARITY ERR (S)	P0 ARB CMP CHK ERR	P1 ARB CMP CHK ERR	PKID CHK ERR	(RSV)	(RSV)	(RSV)
77		DRR::DRESTAD						
	CBUF0/1 DATA0 PARITY ERR	CBUF0/1 DATA1 PARITY ERR	CBUF0/1 DATA2 PARITY ERR	CBUF0/1 DATA3 PARITY ERR	CBUF0/1 DATA4 PARITY ERR	CBUF0/1 DATA5 PARITY ERR	CBUF0/1 DATA6 PARITY ERR	CBUF0/1 DATA7 PARITY ERR
78		Micro Information						
		List Number Expect to Execute						
79		Micro Information						
		List Number Expect to Execute						
7A		Micro Information						
		List Number Executed						
7B		Micro Information						
		List Number Executed						
7C		Micro Information						
		Job Restart Bits						
7D		Micro Information						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7E		Micro Information						
		Error Devided Result Code						
7F		Micro Information						
		CHK2 Detected Counter (Low)						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte40-7F Detail
(2) Byte28 = 11, 13, B1 (1/4)

	0	1	2	3	4	5	6	7
40		MMC::RCVINT						
	SYSRST Interrupt Monitor	SELRST Interrupt Monitor	CHK1A Interrupt Monitor	CHK1B Interrupt Monitor	SMP Interrupt Monitor	LAN/SIO Interrupt Monitor	CHA/DRR Interrupt Monitor	ADP/SCA0 Interrupt Monitor
41		MMC::RCVINT						
	(RSV)	CHK3 Interrupt Monitor	(RSV)	SCA1 Interrupt Monitor	SCA2 Interrupt Monitor	SCA3 Interrupt Monitor	SCA4 Interrupt Monitor	SCA5 Interrupt Monitor
42		DRR::DRMODE1						
	DRR CUDG MODE	DRR SYSTEM CLK MASK	DRR FORCE ERR	(RSV)	(RSV)	DRB W/R ENABLE	SLRC CHK MASK	SUBBLOCK DT-NO
43		DRR::DRMODE1						
	64-CMD MODE	SLAVE 2 ADR SEL	DATA ERR REPORT ENABLE	CHSN ABORT	(RSV)	RNGOSC ENABLE	DRR ABORT	DRR CHK2RST ON
44		DRR::DRMODE5						
	C PATH#00 ENABLE	C PATH#01 ENABLE	C PATH#02 ENABLE	C PATH#03 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
45		DRR::DRMODE5						
	C PATH#10 ENABLE	C PATH#11 ENABLE	C PATH#12 ENABLE	C PATH#13 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
46		DRR::CMD0A						
	CMD A SLRC CHK	(RSV)	(RSV)	CMD A SP MODE	CMD A DIAG MODE	(RSV)	(RSV)	(RSV)
47		DRR::CMD0A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
48		DRR::ADR0A						
		CMD A Slave 1 Cache Transfer Address (BYTE0)						
49		DRR::ADR0A						
		CMD A Slave 2 Cache Transfer Address (BYTE0)						
4A		DRR::ADR1A						
		CMD A Slave 1 Cache Transfer Address (BYTE1)						
4B		DRR::ADR3A						
		CMD A Slave 2 Cache Transfer Address (BYTE1)						
4C		DRR::TRMDA						
	CMD A SYND CHK	(RSV)	CMD A MRCF FUNCTION	CMD A DOUBLE WT MODE	CMD A Transfer Command			
4D		DRR::TRMDA						
	LA0(LBA) COMP CHK ENABLE	LA1 COMP CHK ENABLE	LA2 COMP CHK ENABLE	(RSV)	EXLA COUNT UP STOP	(RSV)	(RSV)	(RSV)
4E		DRR::LA0A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4F		DRR::LA0A						
		CMD A Expect LA Value (BYTE0)						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte40-7F Detail
(2) Byte28 = 11, 13, B1 (2/4)

	0	1	2	3	4	5	6	7
50		DRR::LA1A						
		CMD A Expect LA Value (BYTE1)						
51		DRR::LA1A						
		CMD A Expect LA Value (BYTE2)						
52		DRR::LA2A						
		CMD A Expect LA Value (BYTE3)						
53		DRR::LA2A						
		CMD A Expect LA Value (BYTE4)						
54		DRR::CMD0B						
	CMD B SLRC CHK	(RSV)	(RSV)	CMD B SP MODE	CMD B DIAG MODE	(RSV)	(RSV)	(RSV)
55		DRR::CMD0B						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
56		DRR::ADR0B						
		CMD B Slave 1 Cache Transfer Address (BYTE0)						
57		DRR::ADR0B						
		CMD B Slave 2 Cache Transfer Address (BYTE0)						
58		DRR::ADR1B						
		CMD B Slave 1 Cache Transfer Address (BYTE1)						
59		DRR::ADR3B						
		CMD B Slave 2 Cache Transfer Address (BYTE1)						
5A		DRR::TRMDB						
	CMD B SYND CHK	(RSV)	CMD B MRCF FUNCTION	CMD B DOUBLE WT MODE	CMD B Transfer Command			
5B		DRR::TRMDB						
	LA0(LBA) COMP CHK ENABLE	LA1 COMP CHK ENABLE	LA2 COMP CHK ENABLE	(RSV)	EXLA COUNT UP STOP	(RSV)	(RSV)	(RSV)
5C		DRR::LA0B						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5D		DRR::LA0B						
		CMD B Expect LA Value (BYTE0)						
5E		DRR::LA1B						
		CMD B Expect LA Value (BYTE1)						
5F		DRR::LA1B						
		CMD B Expect LA Value (BYTE2)						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte40-7F Detail
(2) Byte28 = 11, 13, B1 (3/4)

	0	1	2	3	4	5	6	7
60	DRR::LA2B CMD B Expect LA Value (BYTE3)							
61	DRR::LA2B CMD B Expect LA Value (BYTE4)							
62	DRR::RLALR0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
63	DRR::RLALR0 LA Value When LA ERR Occured (BYTE0)							
64	DRR::RLALR1 LA Value When LA ERR Occured (BYTE1)							
65	DRR::RLALR1 LA Value When LA ERR Occured (BYTE2)							
66	DRR::RLALR2 LA Value When LA ERR Occured (BYTE3)							
67	DRR::RLALR2 LA Value When LA ERR Occured (BYTE4)							
68	DRR::D64CNTM							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	Command Pointer(High)	
69	DRR::D64CNTM Command Pointer(Low)							
6A	DRR::DRST10 CHSN STATUS0 BYTE0							
6B	DRR::DRST10 CHSN STATUS0 BYTE1							
6C	DRR::DRST11 CHSN STATUS0 BYTE1 (SUB)							
6D	DRR::DRST11 CHSN STATUS0 BYTE0 (SYB)							
6E	DRR::DRST20 CHSN STATUS1 BYTE0							
6F	DRR::DRST20 CHSN STATUS1 BYTE1							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte40-7F Detail
(2) Byte28 = 11, 13, B1 (4/4)

	0	1	2	3	4	5	6	7
70		DRR::DRST21						
		CHSN STATUS1 BYTE1 (SUB)						
71		DRR::DRST21						
		CHSN STATUS1 BYTE0 (SUB)						
72		DRR::DRESTA4						
	STS0 DT0 PARITY ERR	STS0 DT1 PARITY ERR	STS0 DT2 PARITY ERR	STS0 DT3 PARITY ERR	STS0 DT4 PARITY ERR	STS0 DT5 PARITY ERR	STS0 DT6 PARITY ERR	STS0 DT7 PARITY ERR
73		DRR::DRESTA5						
	P0 TX DT0 PARITY ERR	P0 TX DT1 PARITY ERR	P0 TX DT2 PARITY ERR	P0 TX DT3 PARITY ERR	P0 TX DT4 PARITY ERR	P0 TX DT5 PARITY ERR	P0 TX DT6 PARITY ERR	P0 TX DT7 PARITY ERR
74		DRR::DRESTA6						
	P0 RX DT0 PARITY ERR	P0 RX DT1 PARITY ERR	P0 RX DT2 PARITY ERR	P0 RX DT3 PARITY ERR	P0 RX DT4 PARITY ERR	P0 RX DT5 PARITY ERR	P0 RX DT6 PARITY ERR	P0 RX DT7 PARITY ERR
75		DRR::DRESTA6						
	P0 TXX I-DT0	P0 TXX I-DT1	P0 TXX O-DT0	P0 TXX O-DT1	P1 TXX I-DT0	P1 TXX I-DT1	P1 TXX O-DT0	P1 TXX O-DT1
76		DRR::DRESTAB						
	P0 AC PLRC ERR	P0 DT PLRC ERR	P0 STS0 PLRC ERR	P1 STS0 PLRC ERR	P0 AC INV-PLRC ERR	P0 DT INV-PLRC ERR	P0 STS0 INV-PLRC ERR	P0 STS1 INV-PLRC ERR
77		DRR::DRESTAB						
	P0 AC END-CODE ERR	P0 DT END-CODE ERR	P0 STS0 END-CODE ERR	P0 STS1 END-CODE ERR	P0 SLRC CHECK ERR	P0 SLRC CAL DT ERR	P0 SLRC RD DT ERR	P0 SBLK DCNT ERR
78		Micro Information						
		List Number Expect to Execute						
79		Micro Information						
		List Number Expect to Execute						
7A		Micro Information						
		List Number Executed						
7B		Micro Information						
		List Number Executed						
7C		Micro Information						
		Job Restart Bits						
7D		Micro Information						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7E		Micro Information						
		Error Devided Result Code						
7F		Micro Information						
		CHK2 Detected Counter (Low)						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte40-7F Detail
(3) Byte28 = 12, 14, B2 (1/4)

	0	1	2	3	4	5	6	7
40		MMC::RCVINT						
	SYSRST Interrupt Monitor	SELRST Interrupt Monitor	CHK1A Interrupt Monitor	CHK1B Interrupt Monitor	SMP Interrupt Monitor	LAN/SIO Interrupt Monitor	CHA/DRR Interrupt Monitor	ADP/SCA0 Interrupt Monitor
41		MMC::RCVINT						
	(RSV)	CHK3 Interrupt Monitor	(RSV)	SCA1 Interrupt Monitor	SCA2 Interrupt Monitor	SCA3 Interrupt Monitor	SCA4 Interrupt Monitor	SCA5 Interrupt Monitor
42		DRR::DRMODE1						
	DRR CUDG MODE	DRR SYSTEM CLK MASK	DRR FORCE ERR	(RSV)	(RSV)	DRB W/R ENABLE	SLRC CHK MASK	SUBBLOCK DT-NO
43		DRR::DRMODE1						
	64-CMD MODE	SLAVE 2 ADR SEL	DATA ERR REPORT ENABLE	CHSN ABORT	(RSV)	RNGOSC ENABLE	DRR ABORT	DRR CHK2RST ON
44		DRR::DRMODE5						
	C PATH#00 ENABLE	C PATH#01 ENABLE	C PATH#02 ENABLE	C PATH#03 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
45		DRR::DRMODE5						
	C PATH#10 ENABLE	C PATH#11 ENABLE	C PATH#12 ENABLE	C PATH#13 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
46		DRR::CMD0A						
	CMD A SLRC CHK	(RSV)	(RSV)	CMD A SP MODE	CMD A DIAG MODE	(RSV)	(RSV)	(RSV)
47		DRR::CMD0A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
48		DRR::ADR0A						
		CMD A Slave 1 Cache Transfer Address (BYTE0)						
49		DRR::ADR0A						
		CMD A Slave 2 Cache Transfer Address (BYTE0)						
4A		DRR::ADR1A						
		CMD A Slave 1 Cache Transfer Address (BYTE1)						
4B		DRR::ADR3A						
		CMD A Slave 2 Cache Transfer Address (BYTE1)						
4C		DRR::TRMDA						
	CMD A SYND CHK	(RSV)	CMD A MRCF FUNCTION	CMD A DOUBLE WT MODE	CMD A Transfer Command			
4D		DRR::TRMDA						
	LA0(LBA) COMP CHK ENABLE	LA1 COMP CHK ENABLE	LA2 COMP CHK ENABLE	(RSV)	EXLA COUNT UP STOP	(RSV)	(RSV)	(RSV)
4E		DRR::LA0A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4F		DRR::LA0A						
		CMD A Expect LA Value (BYTE0)						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte40-7F Detail
(3) Byte28 = 12, 14, B2 (2/4)

	0	1	2	3	4	5	6	7
50		DRR::LA1A						
		CMD A Expect LA Value (BYTE1)						
51		DRR::LA1A						
		CMD A Expect LA Value (BYTE2)						
52		DRR::LA2A						
		CMD A Expect LA Value (BYTE3)						
53		DRR::LA2A						
		CMD A Expect LA Value (BYTE4)						
54		DRR::CMD0B						
	CMD B SLRC CHK	(RSV)	(RSV)	CMD B SP MODE	CMD B DIAG MODE	(RSV)	(RSV)	(RSV)
55		DRR::CMD0B						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
56		DRR::ADR0B						
		CMD B Slave 1 Cache Transfer Address (BYTE0)						
57		DRR::ADR0B						
		CMD B Slave 2 Cache Transfer Address (BYTE0)						
58		DRR::ADR1B						
		CMD B Slave 1 Cache Transfer Address (BYTE1)						
59		DRR::ADR3B						
		CMD B Slave 2 Cache Transfer Address (BYTE1)						
5A		DRR::TRMDB						
	CMD B SYND CHK	(RSV)	CMD B MRCF FUNCTION	CMD B DOUBLE WT MODE	CMD B Transfer Command			
5B		DRR::TRMDB						
	LA0(LBA) COMP CHK ENABLE	LA1 COMP CHK ENABLE	LA2 COMP CHK ENABLE	(RSV)	EXLA COUNT UP STOP	(RSV)	(RSV)	(RSV)
5C		DRR::LA0B						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5D		DRR::LA0B						
		CMD B Expect LA Value (BYTE0)						
5E		DRR::LA1B						
		CMD B Expect LA Value (BYTE1)						
5F		DRR::LA1B						
		CMD B Expect LA Value (BYTE2)						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte40-7F Detail
(3) Byte28 = 12, 14, B2 (3/4)

	0	1	2	3	4	5	6	7
60		DRR::LA2B						
		CMD B Expect LA Value (BYTE3)						
61		DRR::LA2B						
		CMD B Expect LA Value (BYTE4)						
62		DRR::RLALR0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
63		DRR::RLALR0						
		LA Value When LA ERR Occured (BYTE0)						
64		DRR::RLALR1						
		LA Value When LA ERR Occured (BYTE1)						
65		DRR::RLALR1						
		LA Value When LA ERR Occured (BYTE2)						
66		DRR::RLALR2						
		LA Value When LA ERR Occured (BYTE3)						
67		DRR::RLALR2						
		LA Value When LA ERR Occured (BYTE4)						
68		DRR::D64CNTM						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	Command Pointer(High)	
69		DRR::D64CNTM						
		Command Pointer(Low)						
6A		DRR::DRST10						
		CHSN STATUS0 BYTE0						
6B		DRR::DRST10						
		CHSN STATUS0 BYTE1						
6C		DRR::DRST11						
		CHSN STATUS0 BYTE1 (SUB)						
6D		DRR::DRST11						
		CHSN STATUS0 BYTE0 (SYB)						
6E		DRR::DRST20						
		CHSN STATUS1 BYTE0						
6F		DRR::DRST20						
		CHSN STATUS1 BYTE1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8B (DRR CHK2) Byte40-7F Detail
(3) Byte28 = 12, 14, B2 (4/4)

	0	1	2	3	4	5	6	7
70		DRR::DRST21						
		CHSN STATUS1 BYTE1 (SUB)						
71		DRR::DRST21						
		CHSN STATUS1 BYTE0 (SUB)						
72		DRR::DRESTA4						
	STS1 DT0 PARITY ERR	STS1 DT1 PARITY ERR	STS1 DT2 PARITY ERR	STS1 DT3 PARITY ERR	STS1 DT4 PARITY ERR	STS1 DT5 PARITY ERR	STS1 DT6 PARITY ERR	STS1 DT7 PARITY ERR
73		DRR::DRESTA7						
	P1 TXX I-DT0	P1 TXX I-DT1	P1 TXX O-DT0	P1 TXX O-DT1	P1 TXX I-DT0	P1 TXX I-DT1	P1 TXX O-DT0	P1 TXX O-DT1
74		DRR::DRESTA7						
	P1 TX DT0 PARITY ERR	P1 TX DT1 PARITY ERR	P1 TX DT2 PARITY ERR	P1 TX DT3 PARITY ERR	P1 TX DT4 PARITY ERR	P1 TX DT5 PARITY ERR	P1 TX DT6 PARITY ERR	P1 TX DT7 PARITY ERR
75		DRR::DRESTA6						
	P1 RX DT0 PARITY ERR	P1 RX DT1 PARITY ERR	P1 RX DT2 PARITY ERR	P1 RX DT3 PARITY ERR	P1 RX DT4 PARITY ERR	P1 RX DT5 PARITY ERR	P1 RX DT6 PARITY ERR	P1 RX DT7 PARITY ERR
76		DRR::DRESTAC						
	P1 AC PLRC ERR	P1 DT PLRC ERR	P1 STS0 PLRC ERR	P1 STS0 PLRC ERR	P1 AC INV-PLRC ERR	P1 DT INV-PLRC ERR	P1 STS0 INV-PLRC ERR	P1 STS1 INV-PLRC ERR
77		DRR::DRESTAC						
	P1 AC END-CODE ERR	P1 DT END-CODE ERR	P1 STS0 END-CODE ERR	P1 STS1 END-CODE ERR	P1 SLRC CHECK ERR	P1 SLRC CAL DT ERR	P1 SLRC RD DT ERR	P1 SBLK DCNT ERR
78		Micro Information						
		List Number Expect to Execute						
79		Micro Information						
		List Number Expect to Execute						
7A		Micro Information						
		List Number Executed						
7B		Micro Information						
		List Number Executed						
7C		Micro Information						
		Job Restart Bits						
7D		Micro Information						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7E		Micro Information						
		Error Devided Result Code						
7F		Micro Information						
		CHK2 Detected Counter (Low)						

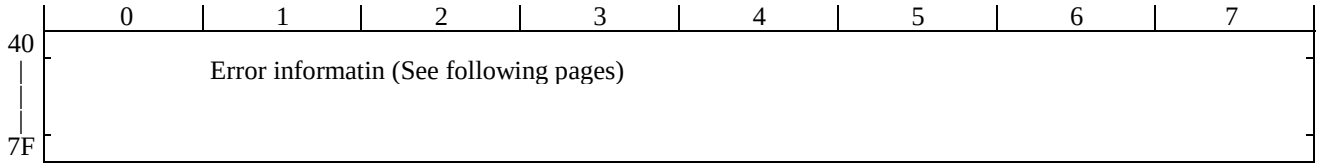
Copyright ©2000, Hitachi, Ltd.

Byte27 = 8C (SVP Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘8’)				Message (x‘C’)			
28								
29	Error information (See following pages)							
2A								
2B								
2C								
2D								
2E								
2F								
30	Error type code (Note 1)							
31								
32								
33	Error information (See following pages)							
34								
35								
36	Sympton code (x‘FF8C’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8C (SVP Failure) (2/2)



(Note 1) Error type code

x‘0000’ : Logical inconsistency
x‘0001’ : HEAP related error
x‘0002’ : File related error
x‘0003’ : LAN failure
x‘0004’ : SSVP failure
x‘0005’ : Windows failure
x‘0006’ : CUDG detected error
x‘0009’ : BOOT detected error
x‘000A’ : SVP message

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8 C (SVP Failure) Byte28-35,40-7F detail

(1) Logical inconsistency / HEEP/File/LAN/Windows failure/SVP message

	0	1	2	3	4	5	6	7
28	Failed AP code (Note 1)							
29								
2A	Reserved							
⋮								
2F								
30	Error type code (x‘0000’ /x‘0001’ /x‘0002’ /x‘0003’ /x‘0005’ /x‘000A’)							
31								
32	Error code							
⋮								
35								
40	Failed Window class							
⋮								
47								
48	Failed function name							
⋮								
5F								
60	Failed line number							
61								
62	Error code							
⋮								
65								
66	Reserved							
⋮								
7F								

(Note 1) Failed AP code

x‘0000’ : Dump task
x‘0001’ : DKU inline
x‘0002’ : Microprogram change (online)
x‘0003’ : Information
x‘0004’ : LOGOUT
x‘0005’ : PATH inline
x‘0006’ : Back ground
x‘0007’ : DIAG
x‘0008’ : Install
x‘0009’ : On-line
x‘000A’ : Micro-program change (off-line)
x‘000B’ : Special package change
x‘000C’ : Common function for communication
x‘00FF’ : Others

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8C (SVP Failure) Byte28-35,40-7F detail

(2) SSVP failure

	0	1	2	3	4	5	6	7
28	Failed AP code (x‘000C’)							
29								
2A	Reserved							
2F								
30	Error type code (x‘0004’)							
31								
32	Reserved							
33								
34	SSVP Error code							
35								
40	SSVP IMPL Sequence							
41	Detect Code							
42	Part Code							
43								
44	SSVP Error							
45								
46	Detail Information							
4F								
50	Reserved							
57								
58	Reserved							
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8C (SVP Failure) Byte28-35,40-7F detail

(3) CUDG detected error

	0	1	2	3	4	5	6	7
28 29 2A 2B 2C 2D 2E 2F	‘CUDG ERR’ (x‘43 55 44 47 20 45 52 52’)							
30 31	Error type code (x‘0006’)							
32 33 34 35	Error code (x‘00000000’)							

40	Error occured time (year)
41	Error occured time (month)
42	Error occured time (day)
43	Error occured time (hour)
44	Error occured time (minute)
45	Error occured time (second)
46	Report MPID
47	Test object
48	Test type (x‘01’ : CUDG3, x‘10’ : LCDG3/FCDG3)
49	Failed LCP number
4A	Test contents
4B	Test contents
4C	Error code
4D	Error code
4E	Not used
4F	Not used
50	Cache module group number (slave 1)
51	Cache module group number (slave 1)
52	Cache module group number (slave 1)
53	Cache module group number (slave 1)
54	Cache module group number (slave 2)
55	Cache module group number (slave 2)
56	Cache module group number (slave 2)
57	Cache module group number (slave 2)
58	PCB location (main platter)
59	PCB location (main platter)
5A	PCB location (main platter)
5B	PCB location (cache platter 1)
5C	PCB location (cache platter 1)
5D	PCB location (cache platter 2)
5E	PCB location (cache platter 2)
5F	Run option
60 ⋮ 7F	Additional information (Note 1)

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 8C (SVP Failure) Byte28-35, 40-7F detail

(Note 1) Additional information (for LCDG3/FCDG3 only)

	0	1	2	3	4	5	6	7
60								
61		Reserved						
62								
63								
64		Record type (x‘0F’ : LCP IMPL diagnostic, x‘10’ : HTP IMPL diagnostic)						
65		Reserved						
66		MP ID (of CHP : x‘10’~x‘17’)						
67		LCP ID (LCP#A : x‘80’~LCP#H : x‘01’)						
68		Error code (Note 2)						
69		Process type (Note 3)						
6A		Error status 1 (Record type (Byte 64) = x‘0F’ (Note 4), x‘10’ (Note 6))						
6B								
6C								
6D		Error status 2 (Note 5)						
6E								
6F								
70								
71								
72								
73								
74								
|		Reserved						
7F								

(Note 2) Error code

Code	Meaning	Function	Remarks
0A	LCDG3’/FCDG3’ load error	LCDG3’/FCDG3’	Make status in loading process
10	Memory clear and test error	LCDG3’/FCDG3’	Set LCP address into error status 1
18	LCDG3’/FCDG3’ MP detected error	LCDG3/FCDG3	Detail information in error status 1 and 2
1A	LCDG3/FCDG3 load error	LCDG3/FCDG3	Make status in loading process
1F	LCDG3’ error before LCP loading	Main loading	LCDG 3 information in status
20	SCAN detected error	All	MP detected error
2A	LCP main load error	Main loading	Make status in loading process
30	LCPdetected error	LCDG3’	Detail information in error status 1 and 2
|		LCDG3	
FF			

(Note 3) Process type

Code	Process	Remarks
01	LCDG3’/FCDG3’	Set loading error status when a loading error occured.
02	LCDG3/FCDG3	Set loading error status when a loading error occured.
03	Loading	

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 8C (SVP Failure) Byte 28-35,40-7F detail

(Note 4) Error status 1 (Record type (Byte 64) = x‘0F’: LCDG3)

Code	Meaning
0101	LCDG3’ activation faild.
010F	LCP terminated after LCDG3’ activation.
0118	No notification after LCDG3’ communication.
011F	LCP CHK1 occured after LCDG3’ activation.
0120	No REQM after LCDG3’ completion.
0122	No notification after LCDG3’ set CALM.
0123	No notification after LCDG3’ set DGIN.
0125	LCP# ≠ Board#
0301	CRC check start error after loading.
030F	LCP terminated after CRC check completion.
0318	No notification for communicatin after CRC check completion.
031F	CHK1 occured in CRC check.
0320	No REQM after CRC check completion.
0322	No notification after CRC check and CALM completion.
0323	No notification after CRC check and DGIN completion.
0325	LCP# ≠ Board#
032F	No CRC check status ID.
0340	CRC check error in LCDG3 loading/Main loaking.
0380	No start address for CRC check routine.
0385	An error occured in configuration/version information transfer for Main loading.
0401	LCDG3 activation for internal diagnosis failed.
040F	LCP terminated after LCDG3’ activation.
0418	No notification after communication for internal diagnosis.
041F	LCP CHK1 occured after internal diagnosis activation.
0420	No REQM after internal diagnosis completion.
0422	No notification after internal diagnosis and CALM.
0423	No notification after internal diagnosis and DGIN.
0425	LCP# ≠ Board#
042F	No status ID for internal diagnosis effect.
043F	No parameter ID for internal diagnosis activation.
044F	No activation address ID for internal diagnosis.
04F0	Controller in configutation is inconsistent with rea1 machine.
04F1	Controller in configutation is inconsistent with rea1 machine.
0501	LCDG3 activation for communication diagnosis failed.
050F	LCP terminated after LCDG3’ activation.
0518	No notification after communication for communication diagnosis.
051F	LCP CHK1 occured after communication diagnosis activation.
0520	No REQM after communication diagnosis completion.
0522	No notification after communication diagnosis and CALM.
0523	No notification after communication diagnosis and DGIN.
0525	LCP# ≠ Board#
052F	No effect status ID for communication diagnosis.
053F	No activation parameter ID for communication diagnosis.
054F	No activation address ID for communication diagnosis.
1000-FFFF	An error address of memory clear test (when error code = x‘10’)
1000-FFFF	LCDG3 error code for internal/communication diagnosis (when error code ≥ x‘30’)
XXXX	MP error code for LCDG3 communication diagnosis (when error code = x‘18’)

Copyright ©2000,2001, Hitachi, Ltd.

(Note 5) Error status 2

(1) When process type = x‘01’ and error code ≥ x‘30’ and error status 1 ≥ x‘1000’,
LCP error code for LCDG3’.
(2) When process type = x‘02’ and error code ≥ x‘30’ and error status 1 ≥ x‘1000’),
LCP error code for LCDG3.
(3) When process type = x‘02’ and error code = x‘18’,
Byte 6C-6D : Error register address
Byte 6E-6F : Active register value.
Byte 70-71 : Expected register value
Byte 72-73 : Return sequence
(4) When other case, this value is invalid.

(Note 6) Error status 1 (Record type (Byte 64) = x‘10’ :FCDG3)

Code	Meaning
0101	FCDG3’ Waiting for end of diagnosis timeout
0102	FCDG3’ SVC I/F error
0103	FCDG3’ ASTS Initialization Error
0110	FCDG3’ Failure detected in preliminary diagnosis
0111	FCDG3’ Failure detected in Memory diagnosis (Fixed pattern)
0112	FCDG3’ Failure detected in Memory diagnosis (Sequential access)
0113	FCDG3’ Failure detected in Memory diagnosis (Byte increment data)
08xx	FCDG3 HTP Processor Diagnosis
09xx	FCDG3 HTP → CHP Transfer diagnosis (Pointer Addressing Area)
0Axx	FCDG3 HTP → CHP Transfer diagnosis (Direct Addressing COMM Area)
0Bxx	FCDG3 HTP → CHP Transfer diagnosis (Direct Addressing DXBF Area)
0Cxx	FCDG3 CHP → HTP Transfer diagnosis
0Dxx	FCDG3 Hot Line Communication diagnosis
0Exx	FCDG3 IntReq diagnosis
0Fxx	FCDG3 Info Transmission diagnosis
10xx	FCDG3 Signal Diagnosis
11xx	FCDG3 Transfer diagnosis
12xx	FCDG3 Link Diagnosis/LSI Rev. Check

xx: 01 ASTS Initialization Error
02 MPCK Detected
10 SVC I/F Error
20 Time-out
21 Frame transmission time-out
22 Frame reception time-out
23 DXBF Access Time-out
24 XFS Time-out
25 PXSTS Time-out
30 CHK1B Detected
31 CHK2 Detected
32 CHK2E Detected
40 Compare Error
50 MMC Status Error
51 XFS Status Error
52 HTPSTS Status Error
53 ONLSTS Status Error

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 8C (SVP Failure) Byte28-35,40-7F detail

(4) BOOT detected error

	0	1	2	3	4	5	6	7
28								
29								
2A								
2B								
2C								
2D								
2E								
2F								
30								
31								
32								
33								
34								
35								
40								
|								
4F								
50								
51								
52								
53								
54								
55								
56								
57								
58								
59								
5A								
5B								
5C								
5D								
5E								
5F								
60								
|								
7F								

'BOOT ERR' (x'42 4F 4F 54 20 45 52 52')

Error type code (x'0009')

Error code (x'0000X000' X:Processor number)

Error detection point

Reserved

Error code for loading error

Error code of internal interface

Error code of initialization function (Note 1)

Reserved

(Note 1) Error code of initialization function.

x'31000041' : Forcible start with jumper pin.

x'40000041' : Load module ID in FM is incorrect.
(FM writing was failed or load module is incorrect)

x'42000041' : Sum check error of FM.
(Failure occured at FM writing or input/output error of FM occurred)

x'48000041' : This MP has the micro-programs which type is different from the PCB name.
(In the MP-Install procedure, the package may have been set which type is different from one that is specified in the define configuration.)

x'56000041' : Sum check error of the load module.
(SVP Failure occured)

Others : Loading for the load module impossible.
(The load module was incorrect)

Copyright ©2000, Hitachi, Ltd.

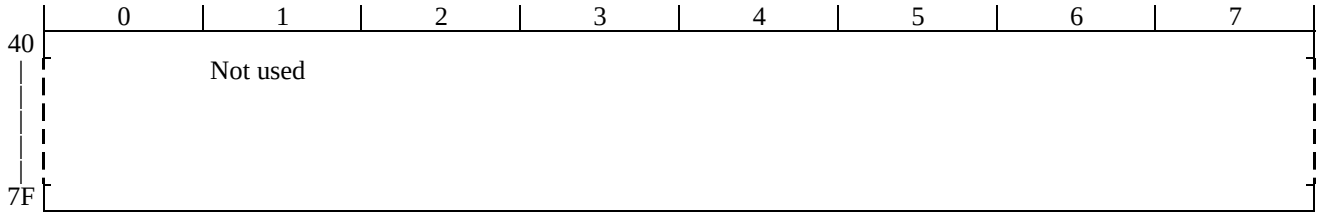
Byte27 = 8D (Power Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low order)							
26	Cylinder address (high order)				Head address			
27	Format (x‘8’)				Message (x‘D’)			
28								
29	Hardware information (See following pages)							
2A								
2B								
2C								
2D								
2E								
2F								
30								
31								
32	Not used							
33								
34	PCB							
35	SSID of self subsystem (low order)							
36	Sympton code (x‘FF8D’ : LDEV type = DKU87I/x‘EF8D’ : LDEV type = DKU86I)*							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8D (Power Failure) (2/2)



Copyright ©2000, Hitachi, Ltd.

Byte27 = 8D (DKU/HDU Power Failure) Hard information

	0	1	2	3	4	5	6	7
28	Subcode : x‘80’ : DKA detected DKU/HDU Power Failure							
29	Failure detected PDEV							
	SPC Pass# (0 ~ 3)				SCSI id# (0 ~ x‘F’)			
2A	PDEV Power Status (SPC Pass#0, basic DKU box)							
	PDEV (id# x‘F’)	PDEV (id# x‘E’)	PDEV (id# x‘D’)	PDEV (id# x‘C’)	PDEV (id# x‘B’)	PDEV (id# x‘A’)	PDEV (id# x‘9’)	PDEV (id# x‘8’)
2B	PDEV Power Status (SPC Pass#0, extent DKU box)							
	PDEV (id# x‘7’)	PDEV (id# x‘6’)	PDEV (id# x‘5’)	PDEV (id# x‘4’)	PDEV (id# x‘3’)	PDEV (id# x‘2’)	PDEV (id# x‘1’)	PDEV (id# x‘0’)
2C	PDEV Power Status (SPC Pass#1, basic DKU box)							
	PDEV (id# x‘F’)	PDEV (id# x‘E’)	PDEV (id# x‘D’)	PDEV (id# x‘C’)	PDEV (id# x‘B’)	PDEV (id# x‘A’)	PDEV (id# x‘9’)	PDEV (id# x‘8’)
2D	PDEV Powr Status (SPC Pass#1, extent DKU box)							
	PDEV (id# x‘7’)	PDEV (id# x‘6’)	PDEV (id# x‘5’)	PDEV (id# x‘4’)	PDEV (id# x‘3’)	PDEV (id# x‘2’)	PDEV (id# x‘1’)	PDEV (id# x‘0’)
2E	PDEV Power Status (SPC Pass#2,basic DKU box)							
	PDEV (id# x‘F’)	PDEV (id# x‘E’)	PDEV (id# x‘D’)	PDEV (id# x‘C’)	PDEV (id# x‘B’)	PDEV (id# x‘A’)	PDEV (id# x‘9’)	PDEV (id# x‘8’)
2F	PDEV Power Status (SPC Pass#2, extent DKU box)							
	PDEV (id# x‘7’)	PDEV (id# x‘6’)	PDEV (id# x‘5’)	PDEV (id# x‘4’)	PDEV (id# x‘3’)	PDEV (id# x‘2’)	PDEV (id# x‘1’)	PDEV (id# x‘0’)
30	PDEV Power Status (SPC Pass#3, basic DKU box)							
	PDEV (id# x‘F’)	PDEV (id# x‘E’)	PDEV (id# x‘D’)	PDEV (id# x‘C’)	PDEV (id# x‘B’)	PDEV (id# x‘A’)	PDEV (id# x‘9’)	PDEV (id# x‘8’)
31	PDEV Power Status (SPC Pass#3, extent DKU box)							
	PDEV (id# x‘7’)	PDEV (id# x‘6’)	PDEV (id# x‘5’)	PDEV (id# x‘4’)	PDEV (id# x‘3’)	PDEV (id# x‘2’)	PDEV (id# x‘1’)	PDEV (id# x‘0’)

(*) BYTE32 ~ 7F : Not Used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8D (DKU/HDU Power Failure) Hard information

	0	1	2	3	4	5	6	7
28	Subcode : x‘90’ : DKA detected DKU/HDU Power Failure							
29	Failure HDU (SPC Pass) before restore detected							
	0				Pass#3 Status	Pass#2 Status	Pass#1 Status	Pass#0 Status
2A	PDEV Power Status (SPC Pass#0, basic DKU box)							
	PDEV (id# x‘F’)	PDEV (id# x‘E’)	PDEV (id# x‘D’)	PDEV (id# x‘C’)	PDEV (id# x‘B’)	PDEV (id# x‘A’)	PDEV (id# x‘9’)	PDEV (id# x‘8’)
2B	PDEV Power Status (SPC Pass#0, extent DKU box)							
	PDEV (id# x‘7’)	PDEV (id# x‘6’)	PDEV (id# x‘5’)	PDEV (id# x‘4’)	PDEV (id# x‘3’)	PDEV (id# x‘2’)	PDEV (id# x‘1’)	PDEV (id# x‘0’)
2C	PDEV Power Status (SPC Pass#1, basic DKU box)							
	PDEV (id# x‘F’)	PDEV (id# x‘E’)	PDEV (id# x‘D’)	PDEV (id# x‘C’)	PDEV (id# x‘B’)	PDEV (id# x‘A’)	PDEV (id# x‘9’)	PDEV (id# x‘8’)
2D	PDEV Powr Status (SPC Pass#1, extent DKU box)							
	PDEV (id# x‘7’)	PDEV (id# x‘6’)	PDEV (id# x‘5’)	PDEV (id# x‘4’)	PDEV (id# x‘3’)	PDEV (id# x‘2’)	PDEV (id# x‘1’)	PDEV (id# x‘0’)
2E	PDEV Power Status (SPC Pass#2,basic DKU box)							
	PDEV (id# x‘F’)	PDEV (id# x‘E’)	PDEV (id# x‘D’)	PDEV (id# x‘C’)	PDEV (id# x‘B’)	PDEV (id# x‘A’)	PDEV (id# x‘9’)	PDEV (id# x‘8’)
2F	PDEV Power Status (SPC Pass#2, extent DKU box)							
	PDEV (id# x‘7’)	PDEV (id# x‘6’)	PDEV (id# x‘5’)	PDEV (id# x‘4’)	PDEV (id# x‘3’)	PDEV (id# x‘2’)	PDEV (id# x‘1’)	PDEV (id# x‘0’)
30	PDEV Power Status (SPC Pass#3, basic DKU box)							
	PDEV (id# x‘F’)	PDEV (id# x‘E’)	PDEV (id# x‘D’)	PDEV (id# x‘C’)	PDEV (id# x‘B’)	PDEV (id# x‘A’)	PDEV (id# x‘9’)	PDEV (id# x‘8’)
31	PDEV Power Status (SPC Pass#3, extent DKU box)							
	PDEV (id# x‘7’)	PDEV (id# x‘6’)	PDEV (id# x‘5’)	PDEV (id# x‘4’)	PDEV (id# x‘3’)	PDEV (id# x‘2’)	PDEV (id# x‘1’)	PDEV (id# x‘0’)

(*) BYTE32 ~ 7F : Not Used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 0X/10-13/15-17/2X/30-33/35-36/FE (CHK1A/WCHK1) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder addres (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Hardware information (See following pages)							
|								
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Sympton code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

Note : Failed processor number for WCHK1

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 0X/10-13/15-17/2X/30-33/35-36/FE (CHK1A/WCHK1) (2/5)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT No.							
	'00'							
41	MMC::ERRSTS							
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42	MMC::C1WSTS							
	Not used	Not used	Not used	Not used	Not used	i960 parity error	LANC parity error	CHK1A at FM
43	MMC::C1WSTS							
	CHK1A detected	WCHK1 detected	CHK1A at MPCHK	CHK1A at SRAM	CHK1A at DRAM	WCHK1 at MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
44	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
45	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
46	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
47	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						
48	MMC::ERSTS0							
	Not used	Not used	Not used	CHK1A cause detected	CHK1B cause detected	LM, XR Access error in scanning	DRAM control signal error	Not used
49	MMC::DRAMCTRLERR							
	Not used	Not used	DRAM control signal RAMADR error	DRAM control signal RAS error	DRAM control signal BAS error	DRAM control signal CAS error	DRAM control signal WE error	DRAM control signal DQM error
4A	MMC::ERADR							
	Address from L bus							
4B	MMC::ERADR							
	Address from L bus							
4C	MMC::ERADR							
	Address from L bus							
4D	MMC::ERADR							
	Address from L bus						Not used	Not used
4E	MMC::ERBYT							
	Not used	Not used	DRAM control signal RAMADR error	DRAM control signal RAS error	DRAM control signal BAS error	DRAM control signal CAS error	DRAM control signal WE error	DRAM control signal DQM error
4F	MMC::ERORD							
	Data before correction							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 0X/10-13/15-17/2X/30-33/35-36/FE (CHK1A/WCHK1) (3/5)

	0	1	2	3	4	5	6	7
50		MMC::ERORD						
		Data before correction						
51		MMC::ERORD						
		Data before correction						
52		MMC::ERORD						
		Data before correction						
53		MMC::ERORC						
		Check bit before correction						
54		MMC::ERORC						
		Check bit before correction						
55		MMC::ERRSYD						
		Syndrome before correction						
56		MMC::ERRSYD						
		Syndrome before correction						
57		MMC::ERWA						
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	WR signal value
58		MMC: LAST1IP						
		Last address before CHK1A occurred						
59		MMC: LAST1IP						
		Last address before CHK1A occurred						
5A		MMC: LAST1IP						
		Last address before CHK1A occurred						
5B		MMC: LAST1IP						
		Last address before CHK1A occurred			Not used	Not used	Not used	Not used
5C		MMC: LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
5D		MMC: LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
5E		MMC: LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
5F		MMC: LAST2IP						
		Address one generation older than the last one before CHK1A occurred			Not used	Not used	Not used	Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 0X/10-13/15-17/2X/30-33/35-36/FE (CHK1A/WCHK1) (4/5)

	0	1	2	3	4	5	6	7
60	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1A occurred							
61	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1A occurred							
62	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1A occurred							
63	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1A occurred				Not used	Not used	Not used	Not used
64	MMC:: LAST4IP							
	Address three generations older than the last one before CHK1A occurred							
65	MMC:: LAST4IP							
	Address three generations older than the last one before CHK1A occurred							
66	MMC:: LAST4IP							
	Address three generations older than the last one before CHK1A occurred							
67	MMC:: LAST4IP							
	Address three generations older than the last one before CHK1A occurred				Not used	Not used	Not used	Not used
68	MMC:: LAST1							
	Execution address one generation older than the last one before CHK1A occurred							
69	MMC:: LAST1							
	Execution address one generation older than the last one before CHK1A occurred							
6A	MMC:: LAST1							
	Execution address one generation older than the last one before CHK1A occurred							
6B	MMC:: LAST1							
	Execution address one generation older than the last one before CHK1A occurred				Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address
6C	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred							
6D	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred							
6E	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred							
6F	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred				Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 0X/10-13/15-17/2X/30-33/35-36/FE (CHK1A/WCHK1) (5/5)

	0	1	2	3	4	5	6	7
70	MMC::FMERRSTS							
	Not used	Not used	Not used	Not used	Access to out of FM area	Write to FM write protect area	Parity error of FM CTL sequencer	VPPON signal error
71	MMC::FMERRSTS							
	FMCS0 signal error	FMCS1 signal error	FMCS2 signal error	FMCS3 signal error	FMOE signal error	FMWE signal error	FMBDIR signal error	FMBENB signal error
72	MMC::CECNT							
	Correctable error counter (for upper address bank)							
73	MMC::CECNT							
	Correctable error counter (for upper address bank)							
74	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHK1B at CHA/QDTA	CHK1B at SMP	CHK1B at MIC
75	MMC::CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2 CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
76	MMC::MPCERRSTS							
	Not used	Not used	WCHK1 at MPCHK	CHK1A at MPCHK	Timeout monitor timer parity error	A/B REG inconsistent check error	A/B REG write time-out	A/B REG access sequence error
77	Not used							
78	Not used							
79	MMC::DRAMC1BSTS							
	i960→LM access Correctable errors are over the specified time		I960 XR read incorrect address	I960 XR write incorrect address	Not used	Not used	Not used	Not used
	Bank 0	Bank 1						
7A	MMC::DRAMC1BSTS							
	LANC→LM access Correctable errors are over the specified time		LANC→LM access Uncorrectable error detected		LANC→XR incorrect address	Not used	Not used	Not used
	Bank 0	Bank 1	Bank 0	Bank 1				
7B	MMC::DRAMC1BSTS							
	Not used	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
7C	Not used							
7D	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
7E	MMC::MICCHK1STS							
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	MIC internal bus parity error	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
7F	MMC::MICCHK1STS							
	LAN hold timeout	Wait timeout	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus parity error	XR data parity error

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : WCHK1) Byte28-31 Detail

(1) I960 uncorrectable error

	0	1	2	3	4	5	6	7
28	Subcode x'00': I960 uncorrecctable error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::ERWA							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	WR signal value
2E	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
2F	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
30	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
31	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : WCHK1) Byte28-31 Detail

(2) I960 inbalid BE error

	0	1	2	3	4	5	6	7
28	Subcode x'01': I960 inbalid BE error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::ERBYT							
	LM error occurred word 0	LM error occurred word 1	LM error occurred word 2	LM error occurred word 3	LM access Uncorrectable error signal			
					BE0	BE1	BE2	BE3
2E	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
2F	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
30	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
31	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : WCHK1) Byte28-31 Detail

(3) DRAM control line error

	0	1	2	3	4	5	6	7
28	Subcode x'02': DRAM control line error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::DRAMCTRLERR							
	Not used	Not used	DRAM control signal RAMADR error	DRAM control signal RAS error	DRAM control signal BAS error	DRAM control signal CAS error	DRAM control signal WE error	DRAM control signal DQM error
2E	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
2F	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
30	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
31	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : WCHK1) Byte28-31 Detail

(4) MP W/R sequencer parity error

	0	1	2	3	4	5	6	7
28	Subcode x'03': MP W/R sequencer parity error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::ERBYT							
	LM error occurred word 0	LM error occurred word 1	LM error occurred word 2	LM error occurred word 3	LM access Uncorrectable error signal			
					BE0	BE1	BE2	BE3
2E	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
2F	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
30	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
31	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : WCHK1) Byte28-31 Detail

(5) LANC R/W sequencer parity error

	0	1	2	3	4	5	6	7
28	Subcode x'04': LANC R/W sequencer parity error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::ERBYT							
	LM error occurred word 0	LM error occurred word 1	LM error occurred word 2	LM error occurred word 3	LM access Uncorrectable error signal			
					BE0	BE1	BE2	BE3
2E	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
2F	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
30	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
31	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : WCHK1) Byte28-31 Detail

(6) LM W/R control error

	0	1	2	3	4	5	6	7
28	Subcode x'05': LM W/R control error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::ERBYT							
	LM error occurred word 0	LM error occurred word 1	LM error occurred word 2	LM error occurred word 3	LM access Uncorrectable error signal			
					BE0	BE1	BE2	BE3
2E	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
2F	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
30	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
31	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : WCHK1) Byte28-31 Detail

(7) LM W/R data parity error

	0	1	2	3	4	5	6	7
28	Subcode x'06': LM W/R data parity error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::ERBYT							
	LM error occurred word 0	LM error occurred word 1	LM error occurred word 2	LM error occurred word 3	LM access Uncorrectable error signal			
					BE0	BE1	BE2	BE3
2E	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
2F	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
30	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
31	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : WCHK1) Byte28-31 Detail

(8) DRAM control error

	0	1	2	3	4	5	6	7
28	Subcode x'07': DRAM control error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::ERBYT							
	LM error occurred word 0	LM error occurred word 1	LM error occurred word 2	LM error occurred word 3	LM access Uncorrectable error signal			
					BE0	BE1	BE2	BE3
2E	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
2F	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
30	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
31	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : WCHK1) Byte28-31 Detail

(9) INST buffer control error

	0	1	2	3	4	5	6	7
28	Subcode x'08': INST buffer control error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::ERBYT							
	LM error occurred word 0	LM error occurred word 1	LM error occurred word 2	LM error occurred word 3	LM access Uncorrectable error signal			
					BE0	BE1	BE2	BE3
2E	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
2F	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
30	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
31	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : WCHK1) Byte28-31 Detail

(10) FM sequencer parity error

	0	1	2	3	4	5	6	7
28	Subcode x'09': FM sequencer parity error							
29	MMC::C1WSTS							
	Not used	Not used	Not used	Not used	Not used	I960 parity error was detected	LANC parity error was detected	CHK1A was detected in FM
2A	MMC::C1WSTS							
	CHK1A occurred	WCHK1 occurred	CHK1A occurred in MPCHK	CHK1A occurred at SRAM	CHK1A occurred at DRAM	WCHK1 occurred in MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
2B	MMC::FMERRSTS							
	Not used	Not used	Not used	Not used	Access to out of FM area	Write to FM write protect area	Parity error of FM CTL sequencer	VPPON signal error
2C	MMC::FMERRSTS							
	FMCS0 signal error	FMCS1 signal error	FMCS2 signal error	FMCS3 signal error	FMOE signal error	FMWE signal error	FMBDIR signal error	FMBENB signal error
2D	Not used							
2E	MMC::LAST1							
	Execution address before CHK1A occurred							
2F	MMC::LAST1							
	Execution address before CHK1A occurred							
30	MMC::LAST1							
	Execution address before CHK1A occurred							
31	MMC::LAST1							
	Execution address before CHK1A occurred				Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : WCHK1) Byte28-31 Detail

(11) FM control line error

	0	1	2	3	4	5	6	7
28	Subcode x‘0A’: FM control line error							
29	MMC::C1WSTS							
	Not used	Not used	Not used	Not used	Not used	I960 parity error was detected	LANC parity error was detected	CHK1A was detected in FM
2A	MMC::C1WSTS							
	CHK1A occurred	WCHK1 occurred	CHK1A occurred in MPCHK	CHK1A occurred at SRAM	CHK1A occurred at DRAM	WCHK1 occurred in MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
2B	MMC::FMERRSTS							
	Not used	Not used	Not used	Not used	Access to out of FM area	Write to FM write protect area	Parity error of FM CTL sequencer	VPPON signal error
2C	MMC::FMERRSTS							
	FMCS0 signal error	FMCS1 signal error	FMCS2 signal error	FMCS3 signal error	FMOE signal error	FMWE signal error	FMBDIR signal error	FMBENB signal error
2D	Not used							
2E	MMC::LAST1							
	Execution address before CHK1A occurred							
2F	MMC::LAST1							
	Execution address before CHK1A occurred							
30	MMC::LAST1							
	Execution address before CHK1A occurred							
31	MMC::LAST1							
	Execution address before CHK1A occurred				Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : WCHK1) Byte28-31 Detail

(12) I960 read data parity error

	0	1	2	3	4	5	6	7
28	Subcode x'0B': I960 read data parity error							
29	MMC::C1WSTS							
	Not used	Not used	Not used	Not used	Not used	I960 parity error was detected	LANC parity error was detected	CHK1A was detected in FM
2A	MMC::C1WSTS							
	CHK1A occurred	WCHK1 occurred	CHK1A occurred in MPCHK	CHK1A occurred at SRAM	CHK1A occurred at DRAM	WCHK1 occurred in MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
2B	MMC::MICCHK1STS							
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2C	MMC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error
2D	MMC::LBUSPERR							
	Not used	Not used	Not used	Not used	L bus data parity error			
					<00-07>	<10-17>	<20-27>	<30-37>
2E	MMC::LAST1							
	Execution address before CHK1A occurred							
2F	MMC::LAST1							
	Execution address before CHK1A occurred							
30	MMC::LAST1							
	Execution address before CHK1A occurred							
31	MMC::LAST1							
	Execution address before CHK1A occurred				Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : WCHK1) Byte28-31 Detail

(13) LANC read data parity error

	0	1	2	3	4	5	6	7
28	Subcode x'0C': LANC read data parity error							
29	MMC::C1WSTS							
	Not used	Not used	Not used	Not used	Not used	I960 parity error was detected	LANC parity error was detected	CHK1A was detected in FM
2A	MMC::C1WSTS							
	CHK1A occurred	WCHK1 occurred	CHK1A occurred in MPCHK	CHK1A occurred at SRAM	CHK1A occurred at DRAM	WCHK1 occurred in MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
2B	MMC::MICCHK1STS							
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2C	MMC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error
2D	MMC::LBUSPERR							
	Not used	Not used	Not used	Not used	L bus data parity error			
					<00-07>	<10-17>	<20-27>	<30-37>
2E	MMC::LAST1							
	Execution address before CHK1A occurred							
2F	MMC::LAST1							
	Execution address before CHK1A occurred							
30	MMC::LAST1							
	Execution address before CHK1A occurred							
31	MMC::LAST1							
	Execution address before CHK1A occurred				Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : WCHK1) Byte28-31 Detail

(14) I960 LM write protect error

	0	1	2	3	4	5	6	7
28	Subcode x‘10’: I960 LM write protect error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::LMWRADRU							
	Upper limit address of writable LM mounting area (high)							
2E	MMC::LMWRADRU							
	Upper limit address of writable LM mounting area (low)						Not used	Not used
2F	MMC::LMWRADRL							
	Lower limit address of writable LM mounting area (high)							
30	MMC::LMWRADRL							
	Lower limit address of writable LM mounting area (low)						Not used	Not used
31	MMC::CHK1ASTS							
	I960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : WCHK1) Byte28-31 Detail

(15)I960 LM address over error

	0	1	2	3	4	5	6	7
28	Subcode x‘11’: I960 LM address over error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::LMADRLMT							
	Not used	Not used	Not used	Not used	Not used	Not used	Upper limit address of LM mounting area	
2E	MMC::LMADRLMT							
	Upper limit address of LM mounting area							
2F	MMC::ERWR							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	WR signal value
30	MMC::ERSTS0							
	Not used	Not used	Not used	CHK1A cause detected	CHK1B cause detected	LM, XR Access error in scanning	DRAM control signal error	Not used
31	MMC::CHK1ASTS							
	I960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : WCHK1) Byte28-31 Detail

(16) LANC LM write protect error

	0	1	2	3	4	5	6	7
28	Subcode x'12': LANC LM write protect error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::LMWRADRU							
	Upper limit address of writable LM mounting area (high)							
2E	MMC::LMWRADRU							
	Upper limit address of writable LM mounting area (low)						Not used	Not used
2F	MMC::LMWRADRL							
	Lower limit address of writable LM mounting area (high)							
30	MMC::LMWRADRL							
	Lower limit address of writable LM mounting area (low)						Not used	Not used
31	MMC::CHK1ASTS							
	I960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : WCHK1) Byte28-31 Detail

(17) LANC LM address over error

	0	1	2	3	4	5	6	7
28	Subcode x'13': LANC LM address over error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::LMADRLMT							
	Not used	Not used	Not used	Not used	Not used	Not used	Upper limit address of LM mounting area	
2E	MMC::LMADRLMT							
	Upper limit address of LM mounting area							
2F	MMC::ERWR							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	
30	MMC::ERSTS0							
	Not used	Not used	Not used	CHK1A cause detected	CHK1B cause detected	LM, XR Access error in scanning	DRAM control signal error	Not used
31	MMC::CHK1ASTS							
	I960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : WCHK1) Byte28-31 Detail

(18) FM write protect error

	0	1	2	3	4	5	6	7
28	Subcode x‘15’: FM write protect error							
29	MMC::C1WSTS							
	Not used	Not used	Not used	Not used	Not used	I960 parity error was detected	LANC parity error was detected	CHK1A was detected in FM
2A	MMC::C1WSTS							
	CHK1A occurred	WCHK1 occurred	CHK1A occurred in MPCHK	CHK1A occurred at SRAM	CHK1A occurred at DRAM	WCHK1 occurred in MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
2B	MMC::FMERRSTS							
	Not used	Not used	Not used	Not used	Access to out of FM area	Write to FM write protect area	Parity error of FM CTL sequencer	VPPON signal error
2C	MMC::FMERRSTS							
	FMCS0 signal error	FMCS1 signal error	FMCS2 signal error	FMCS3 signal error	FMOE signal error	FMWE signal error	FMBDIR signal error	FMBENB signal error
2D	Not used							
2E	MMC::LAST1							
	Execution address before CHK1A occurred							
2F	MMC::LAST1							
	Execution address before CHK1A occurred							
30	MMC::LAST1							
	Execution address before CHK1A occurred							
31	MMC::LAST1							
	Execution address before CHK1A occurred				Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : WCHK1) Byte28-31 Detail

(19) FM address over error

	0	1	2	3	4	5	6	7
28	Subcode x'16': FM address over error							
29	MMC::C1WSTS							
	Not used	Not used	Not used	Not used	Not used	I960 parity error was detected	LANC parity error was detected	CHK1A was detected in FM
2A	MMC::C1WSTS							
	CHK1A occurred	WCHK1 occurred	CHK1A occurred in MPCHK	CHK1A occurred at SRAM	CHK1A occurred at DRAM	WCHK1 occurred in MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
2B	MMC::FMERRSTS							
	Not used	Not used	Not used	Not used	Access to out of FM area	Write to FM write protect area	Parity error of FM CTL sequencer	VPPON signal error
2C	MMC::FMERRSTS							
	FMCS0 signal error	FMCS1 signal error	FMCS2 signal error	FMCS3 signal error	FMOE signal error	FMWE signal error	FMBDIR signal error	FMBENB signal error
2D	Not used							
2E	MMC::LAST1							
	Execution address before CHK1A occurred							
2F	MMC::LAST1							
	Execution address before CHK1A occurred							
30	MMC::LAST1							
	Execution address before CHK1A occurred							
31	MMC::LAST1							
	Execution address before CHK1A occurred				Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : WCHK1) Byte28-31 Detail

(20) MP check error

	0	1	2	3	4	5	6	7
28	Subcode x'17': MP check error							
29	MMC::C1WSTS							
	Not used	Not used	Not used	Not used	Not used	I960 parity error was detected	LANC parity error was detected	CHK1A was detected in FM
2A	MMC::C1WSTS							
	CHK1A occurred	WCHK1 occurred	CHK1A occurred in MPCHK	CHK1A occurred at SRAM	CHK1A occurred at DRAM	WCHK1 occurred in MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
2B	MMC::MPCERRSTS							
	Not used	Not used	WCHK1 at MPCHK	CHK1A at MPCHK	Timeout monitor timer parity error	A/B REG inconsistent check error	A/B REG write time-out	A/B REG access sequence error
2C	MIC::MICCHK1STS							
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2D	Not used							
	LAN hold time-out	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error
2E	MMC::LAST1							
	Execution address before CHK1A occurred							
2F	MMC::LAST1							
	Execution address before CHK1A occurred							
30	MMC::LAST1							
	Execution address before CHK1A occurred							
31	MMC::LAST1							
	Execution address before CHK1A occurred				Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHK1A) Byte28-31 Detail

(21) I960 uncorrectable error

	0	1	2	3	4	5	6	7
28	Subcode x'20': I960 uncorrecctable error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::ERWA							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	WR signal value
2E	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
2F	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
30	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
31	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHK1A) Byte28-31 Detail

(22) I960 inbalid BE error

	0	1	2	3	4	5	6	7
28	Subcode x'21': I960 inbalid BE error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::ERBYT							
	LM error occurred word 0	LM error occurred word 1	LM error occurred word 2	LM error occurred word 3	LM access Uncorrectable error signal			
					BE0	BE1	BE2	BE3
2E	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
2F	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
30	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
31	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHK1A) Byte28-31 Detail

(23) DRAM control line error

	0	1	2	3	4	5	6	7
28	Subcode x'22': DRAM control line error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::DRAMCTRLERR							
	Not used	Not used	DRAM control signal RAMADR error	DRAM control signal RAS error	DRAM control signal BAS error	DRAM control signal CAS error	DRAM control signal WE error	DRAM control signal DQM error
2E	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
2F	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
30	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
31	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHK1A) Byte28-31 Detail

(24) MP W/R sequencer parity error

	0	1	2	3	4	5	6	7
28	Subcode x'23': MP W/R sequencer parity error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::ERBYT							
	LM error occurred word 0	LM error occurred word 1	LM error occurred word 2	LM error occurred word 3	LM access Uncorrectable error signal			
					BE0	BE1	BE2	BE3
2E	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
2F	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
30	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
31	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHK1A) Byte28-31 Detail

(25) LANC R/W sequencer parity error

	0	1	2	3	4	5	6	7
28	Subcode x'24': LANC R/W sequencer parity error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::ERBYT							
	LM error occurred word 0	LM error occurred word 1	LM error occurred word 2	LM error occurred word 3	LM access Uncorrectable error signal			
					BE0	BE1	BE2	BE3
2E	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
2F	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
30	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
31	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHK1A) Byte28-31 Detail

(26) LM W/R control error

	0	1	2	3	4	5	6	7
28	Subcode x'25': LM W/R control error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::ERBYT							
	LM error occurred word 0	LM error occurred word 1	LM error occurred word 2	LM error occurred word 3	LM access Uncorrectable error signal			
					BE0	BE1	BE2	BE3
2E	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
2F	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
30	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
31	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHK1A) Byte28-31 Detail

(27) LM W/R data parity error

	0	1	2	3	4	5	6	7
28	Subcode x'26': LM W/R data parity error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::ERBYT							
	LM error occurred word 0	LM error occurred word 1	LM error occurred word 2	LM error occurred word 3	LM access Uncorrectable error signal			
					BE0	BE1	BE2	BE3
2E	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
2F	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
30	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
31	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHK1A) Byte28-31 Detail

(28) DRAM control error

	0	1	2	3	4	5	6	7
28	Subcode x'27': DRAM control error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::ERBYT							
	LM error occurred word 0	LM error occurred word 1	LM error occurred word 2	LM error occurred word 3	LM access Uncorrectable error signal			
					BE0	BE1	BE2	BE3
2E	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
2F	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
30	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
31	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHK1A) Byte28-31 Detail

(29) INST buffer control error

	0	1	2	3	4	5	6	7
28	Subcode x'28': INST buffer control error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::ERBYT							
	LM error occurred word 0	LM error occurred word 1	LM error occurred word 2	LM error occurred word 3	LM access Uncorrectable error signal			
					BE0	BE1	BE2	BE3
2E	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
2F	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
30	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
31	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHK1A) Byte28-31 Detail

(30) FM sequencer parity error

	0	1	2	3	4	5	6	7
28	Subcode x'29': FM sequencer parity error							
29	MMC::C1WSTS							
	Not used	Not used	Not used	Not used	Not used	I960 parity error was detected	LANC parity error was detected	CHK1A was detected in FM
2A	MMC::C1WSTS							
	CHK1A occurred	WCHK1 occurred	CHK1A occurred in MPCHK	CHK1A occurred at SRAM	CHK1A occurred at DRAM	WCHK1 occurred in MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
2B	MMC::FMERRSTS							
	Not used	Not used	Not used	Not used	Access to out of FM area	Write to FM write protect area	Parity error of FM CTL sequencer	VPPON signal error
2C	MMC::FMERRSTS							
	FMCS0 signal error	FMCS1 signal error	FMCS2 signal error	FMCS3 signal error	FMOE signal error	FMWE signal error	FMBDIR signal error	FMBENB signal error
2D	Not used							
2E	MMC::LAST1							
	Execution address before CHK1A occurred							
2F	MMC::LAST1							
	Execution address before CHK1A occurred							
30	MMC::LAST1							
	Execution address before CHK1A occurred							
31	MMC::LAST1							
	Execution address before CHK1A occurred				Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHK1A) Byte28-31 Detail

(31) FM control line error

	0	1	2	3	4	5	6	7
28	Subcode x‘2A’: FM control line error							
29	MMC::C1WSTS							
	Not used	Not used	Not used	Not used	Not used	I960 parity error was detected	LANC parity error was detected	CHK1A was detected in FM
2A	MMC::C1WSTS							
	CHK1A occurred	WCHK1 occurred	CHK1A occurred in MPCHK	CHK1A occurred at SRAM	CHK1A occurred at DRAM	WCHK1 occurred in MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
2B	MMC::FMERRSTS							
	Not used	Not used	Not used	Not used	Access to out of FM area	Write to FM write protect area	Parity error of FM CTL sequencer	VPPON signal error
2C	MMC::FMERRSTS							
	FMCS0 signal error	FMCS1 signal error	FMCS2 signal error	FMCS3 signal error	FMOE signal error	FMWE signal error	FMBDIR signal error	FMBENB signal error
2D	Not used							
2E	MMC::LAST1							
	Execution address before CHK1A occurred							
2F	MMC::LAST1							
	Execution address before CHK1A occurred							
30	MMC::LAST1							
	Execution address before CHK1A occurred							
31	MMC::LAST1							
	Execution address before CHK1A occurred				Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHK1A) Byte28-31 Detail

(32) I960 read data parity error

	0	1	2	3	4	5	6	7
28	Subcode x'2B': I960 read data parity error							
29	MMC::C1WSTS							
	Not used	Not used	Not used	Not used	Not used	I960 parity error was detected	LANC parity error was detected	CHK1A was detected in FM
2A	MMC::C1WSTS							
	CHK1A occurred	WCHK1 occurred	CHK1A occurred in MPCHK	CHK1A occurred at SRAM	CHK1A occurred at DRAM	WCHK1 occurred in MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
2B	MMC::MICCHK1STS							
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2C	MMC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error
2D	MMC::LBUSPERR							
	Not used	Not used	Not used	Not used	L bus data parity error			
					<00-07>	<10-17>	<20-27>	<30-37>
2E	MMC::LAST1							
	Execution address before CHK1A occurred							
2F	MMC::LAST1							
	Execution address before CHK1A occurred							
30	MMC::LAST1							
	Execution address before CHK1A occurred							
31	MMC::LAST1							
	Execution address before CHK1A occurred				Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHK1A) Byte28-31 Detail

(33) LANC read data parity error

	0	1	2	3	4	5	6	7
28	Subcode x'2C': LANC read data parity error							
29	MMC::C1WSTS							
	Not used	Not used	Not used	Not used	Not used	I960 parity error was detected	LANC parity error was detected	CHK1A was detected in FM
2A	MMC::C1WSTS							
	CHK1A occurred	WCHK1 occurred	CHK1A occurred in MPCHK	CHK1A occurred at SRAM	CHK1A occurred at DRAM	WCHK1 occurred in MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
2B	MMC::MICCHK1STS							
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2C	MMC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error
2D	MMC::LBUSPERR							
	Not used	Not used	Not used	Not used	L bus data parity error			
					<00-07>	<10-17>	<20-27>	<30-37>
2E	MMC::LAST1							
	Execution address before CHK1A occurred							
2F	MMC::LAST1							
	Execution address before CHK1A occurred							
30	MMC::LAST1							
	Execution address before CHK1A occurred							
31	MMC::LAST1							
	Execution address before CHK1A occurred				Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address

Copyright ©2000, Hitachi, Ltd.

(34) I960 LM write protect error

	0	1	2	3	4	5	6	7
28	Subcode x'30': I960 LM write protect error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::LMWRADRU							
	Upper limit address of writable LM mounting area (high)							
2E	MMC::LMWRADRU							
	Upper limit address of writable LM mounting area (low)						Not used	Not used
2F	MMC::LMWRADRL							
	Lower limit address of writable LM mounting area (high)							
30	MMC::LMWRADRL							
	Lower limit address of writable LM mounting area (low)						Not used	Not used
31	MMC::CHK1ASTS							
	I960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHK1A) Byte28-31 Detail

(35) I960 LM address over error

	0	1	2	3	4	5	6	7
28	Subcode x'31': I960 LM address over error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::LMADRLMT							
	Not used	Not used	Not used	Not used	Not used	Not used	Upper limit address of LM mounting area	
2E	MMC::LMADRLMT							
	Upper limit address of LM mounting area							
2F	MMC::ERWR							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	WR signal value
30	MMC::ERSTS0							
	Not used	Not used	Not used	CHK1A cause detected	CHK1B cause detected	LM, XR Access error in scanning	DRAM control signal error	Not used
31	MMC::CHK1ASTS							
	I960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHK1A) Byte28-31 Detail

(36) LANC LM write protect error

	0	1	2	3	4	5	6	7
28	Subcode x'32': LANC LM write protect error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::LMWRADRU							
	Upper limit address of writable LM mounting area (high)							
2E	MMC::LMWRADRU							
	Upper limit address of writable LM mounting area (low)						Not used	Not used
2F	MMC::LMWRADRL							
	Lower limit address of writable LM mounting area (high)							
30	MMC::LMWRADRL							
	Lower limit address of writable LM mounting area (low)						Not used	Not used
31	MMC::CHK1ASTS							
	I960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHK1A) Byte28-31 Detail

(37) LANC LM address over error

	0	1	2	3	4	5	6	7
28	Subcode x'33': LANC LM address over error							
29	MMC::ERADR							
	Address from L bus							
2A	MMC::ERADR							
	Address from L bus							
2B	MMC::ERADR							
	Address from L bus							
2C	MMC::ERADR							
	Address from L bus						Not used	Not used
2D	MMC::LMADRLMT							
	Not used	Not used	Not used	Not used	Not used	Not used	Upper limit address of LM mounting area	
2E	MMC::LMADRLMT							
	Upper limit address of LM mounting area							
2F	MMC::ERWR							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	
30	MMC::ERSTS0							
	Not used	Not used	Not used	CHK1A cause detected	CHK1B cause detected	LM, XR Access error in scanning	DRAM control signal error	Not used
31	MMC::CHK1ASTS							
	I960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHK1A) Byte28-31 Detail

(38) FM write protect error

	0	1	2	3	4	5	6	7
28	Subcode x'35': FM write protect error							
29	MMC::C1WSTS							
	Not used	Not used	Not used	Not used	Not used	I960 parity error was detected	LANC parity error was detected	CHK1A was detected in FM
2A	MMC::C1WSTS							
	CHK1A occurred	WCHK1 occurred	CHK1A occurred in MPCHK	CHK1A occurred at SRAM	CHK1A occurred at DRAM	WCHK1 occurred in MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
2B	MMC::FMERRSTS							
	Not used	Not used	Not used	Not used	Access to out of FM area	Write to FM write protect area	Parity error of FM CTL sequencer	VPPON signal error
2C	MMC::FMERRSTS							
	FMCS0 signal error	FMCS1 signal error	FMCS2 signal error	FMCS3 signal error	FMOE signal error	FMWE signal error	FMBDIR signal error	FMBENB signal error
2D	Not used							
2E	MMC::LAST1							
	Execution address before CHK1A occurred							
2F	MMC::LAST1							
	Execution address before CHK1A occurred							
30	MMC::LAST1							
	Execution address before CHK1A occurred							
31	MMC::LAST1							
	Execution address before CHK1A occurred				Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHK1A) Byte28-31 Detail

(39) FM address over error

	0	1	2	3	4	5	6	7
28	Subcode x'36': FM address over error							
29	MMC::C1WSTS							
	Not used	Not used	Not used	Not used	Not used	I960 parity error was detected	LANC parity error was detected	CHK1A was detected in FM
2A	MMC::C1WSTS							
	CHK1A occurred	WCHK1 occurred	CHK1A occurred in MPCHK	CHK1A occurred at SRAM	CHK1A occurred at DRAM	WCHK1 occurred in MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
2B	MMC::FMERRSTS							
	Not used	Not used	Not used	Not used	Access to out of FM area	Write to FM write protect area	Parity error of FM CTL sequencer	VPPON signal error
2C	MMC::FMERRSTS							
	FMCS0 signal error	FMCS1 signal error	FMCS2 signal error	FMCS3 signal error	FMOE signal error	FMWE signal error	FMBDIR signal error	FMBENB signal error
2D	Not used							
2E	MMC::LAST1							
	Execution address before CHK1A occurred							
2F	MMC::LAST1							
	Execution address before CHK1A occurred							
30	MMC::LAST1							
	Execution address before CHK1A occurred							
31	MMC::LAST1							
	Execution address before CHK1A occurred				Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHK1A) Byte28-31 Detail

(40) CHK1A

	0	1	2	3	4	5	6	7
28	Subcode x'FE': CHK1A undefined hardware reason							
29	MMC::C1WSTS							
	Not used	Not used	Not used	Not used	Not used	I960 parity error was detected	LANC parity error was detected	CHK1A was detected in FM
2A	MMC::C1WSTS							
	CHK1A occurred	WCHK1 occurred	CHK1A occurred in MPCHK	CHK1A occurred at SRAM	CHK1A occurred at DRAM	WCHK1 occurred in MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
2B	Not used							
2C	Not used							
2D	Not used							
2E	Not used							
2F	Not used							
30	Not used							
31	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 14/34 (CHK1A/WCHK1) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder addres (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Hardware information (See following pages)							
|								
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Sympton code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

Note : Failed processor number for WCHK1

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 14/34 (CHK1A/WCHK1/Fetch error) (2/5)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT No.							
	'01'							
41	MMC::ERRSTS							
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42	MMC::C1WSTS							
	Not used	Not used	Not used	Not used	Not used	i960 parity error	LANC parity error	CHK1A at FM
43	MMC::C1WSTS							
	CHK1A detected	WCHK1 detected	CHK1A at MPCHK	CHK1A at SRAM	CHK1A at DRAM	WCHK1 at MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
44	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
45	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
46	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
47	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						
48	MMC::ERSTS0							
	Not used	Not used	Not used	CHK1A cause detected	CHK1B cause detected	LM, XR Access error in scanning	DRAM control signal error	Not used
49	MMC::DRAMCTRLERR							
	Not used	Not used	DRAM control signal RAMADR error	DRAM control signal RAS error	DRAM control signal BAS error	DRAM control signal CAS error	DRAM control signal WE error	DRAM control signal DQM error
4A	MMC::FERADR							
	Address from L bus (fetch)							
4B	MMC::ERADR							
	Address from L bus (fetch)							
4C	MMC::ERADR							
	Address from L bus (fetch)							
4D	MMC::ERADR							
	Address from L bus (fetch)						Not used	Not used
4E	MMC::FERBYT							
	Not used	Not used	DRAM control signal RAMADR error	DRAM control signal RAS error	DRAM control signal BAS error	DRAM control signal CAS error	DRAM control signal WE error	DRAM control signal DQM error
4F	MMC::FERORD							
	Data before correction (fetch)							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 14/34 (CHK1A/WCHK1) (3/5)

	0	1	2	3	4	5	6	7
50		MMC::FERORD						
		Data before correction (fetch)						
51		MMC::FERORD						
		Data before correction (fetch)						
52		MMC::FERORD						
		Data before correction (fetch)						
53		MMC::FERORC						
		Check bit before correction (fetch)						
54		MMC::FERORC						
		Check bit before correction (fetch)						
55		MMC::FERRSYD						
		Syndrome before correction (fetch)						
56		MMC::FERRSYD						
		Syndrome before correction (fetch)						
57		Not used						
58		MMC: LAST1IP						
		Last address before CHK1A occurred						
59		MMC: LAST1IP						
		Last address before CHK1A occurred						
5A		MMC: LAST1IP						
		Last address before CHK1A occurred						
5B		MMC: LAST1IP						
		Last address before CHK1A occurred			Not used	Not used	Not used	Not used
5C		MMC: LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
5D		MMC: LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
5E		MMC: LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
5F		MMC: LAST2IP						
		Address one generation older than the last one before CHK1A occurred			Not used	Not used	Not used	Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 14/34 (CHK1A/WCHK1) (4/5)

	0	1	2	3	4	5	6	7
60	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1A occurred							
61	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1A occurred							
62	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1A occurred							
63	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1A occurred				Not used	Not used	Not used	Not used
64	MMC:: LAST4IP							
	Address three generations older than the last one before CHK1A occurred							
65	MMC:: LAST4IP							
	Address three generations older than the last one before CHK1A occurred							
66	MMC:: LAST4IP							
	Address three generations older than the last one before CHK1A occurred							
67	MMC:: LAST4IP							
	Address three generations older than the last one before CHK1A occurred				Not used	Not used	Not used	Not used
68	MMC:: LAST1							
	Execution address one generation older than the last one before CHK1A occurred							
69	MMC:: LAST1							
	Execution address one generation older than the last one before CHK1A occurred							
6A	MMC:: LAST1							
	Execution address one generation older than the last one before CHK1A occurred							
6B	MMC:: LAST1							
	Execution address one generation older than the last one before CHK1A occurred				Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address
6C	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred							
6D	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred							
6E	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred							
6F	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred				Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 14/34 (CHK1A/WCHK1) (5/5)

	0	1	2	3	4	5	6	7
70	MMC::FMERRSTS							
	Not used	Not used	Not used	Not used	Access to out of FM area	Write to FM write protect area	Parity error of FM CTL sequencer	VPPON signal error
71	MMC::FMERRSTS							
	FMCS0 signal error	FMCS1 signal error	FMCS2 signal error	FMCS3 signal error	FMOE signal error	FMWE signal error	FMBDIR signal error	FMBENB signal error
72	MMC::CECNT							
	Correctable error counter (for upper address bank)							
73	MMC::CECNT							
	Correctable error counter (for upper address bank)							
74	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHK1B at CHA/QDTA	CHK1B at SMP	CHK1B at MIC
75	MMC::CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2 CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
76	MMC::MPCERRSTS							
	Not used	Not used	WCHK1 at MPCHK	CHK1A at MPCHK	Timeout monitor timer parity error	A/B REG inconsistent check error	A/B REG write time-out	A/B REG access sequence error
77	Not used							
78	Not used							
79	MMC::DRAMC1BSTS							
	i960→LM access Correctable errors are over the specified time		I960 XR read incorrect address	I960 XR write incorrect address	Not used	Not used	Not used	Not used
	Bank 0	Bank 1						
7A	MMC::DRAMC1BSTS							
	LANC→LM access Correctable errors are over the specified time		LANC→LM access Uncorrectable error detected		LANC→XR incorrect address	Not used	Not used	Not used
	Bank 0	Bank 1	Bank 0	Bank 1				
7B	MMC::DRAMC1BSTS							
	Not used	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
7C	Not used							
7D	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
7E	MMC::MICCHK1STS							
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	MIC internal bus parity error	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
7F	MMC::MICCHK1STS							
	LAN hold timeout	Wait timeout	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus parity error	XR data parity error

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : WCHK1) Byte28-31 Detail

(41) I960 uncorrectable error

	0	1	2	3	4	5	6	7
28	Subcode x‘14’: Fetch uncorectable error							
29	MMC::C1WSTS							
	Error address in fetch to LM							
2A	MMC::FERADR							
	Error address in fetch to LM							
2B	MMC::FERADR							
	Error address in fetch to LM							
2C	MMC::FERADR							
	Error address in fetch to LM						Not used	Not used
2D	Not used							
2E	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
2F	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
30	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
31	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHK1A) Byte28-31 Detail

(42) Fetch uncorectable error

	0	1	2	3	4	5	6	7
28	Subcode x‘34’: Fetch uncorectable error							
29	MMC::C1WSTS							
	Error address in fetch to LM							
2A	MMC::FERADR							
	Error address in fetch to LM							
2B	MMC::FERADR							
	Error address in fetch to LM							
2C	MMC::FERADR							
	Error address in fetch to LM						Not used	Not used
2D	Not used							
2E	MMC::CHK1ASTS							
	Fetch Uncorrectable error		Write buffer in counter error	Write buffer dif counter error	Write buffer out counter error	Invalid BE error	Write data parity error	Byte write data parity error
	Bank 0	Bank 1						
2F	MMC::CHK1ASTS							
	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	Byte0 data parity error	MP read sequencer parity error	LANC read sequencer parity error	Read word counter error	Fetch buffer write pointer error
30	MMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
31	MMC::CHK1ASTS							
	i960→LM access Uncorrectable error		I960 → LM write protect	I960 → LM out of area	LM sequencer error	LM sequencer parity error	LANC→LM write protect	LANC→LM out of area
	Bank 0	Bank 1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 44/45 (CHA CHK1B) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder addres (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode (x‘44’/x‘45’)							
29	Hardware information (See following pages)							
|								
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Sympton code (x‘FF8E’ : LDEV type = 6587/x‘EF8E’ : LDEV type = 6586)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 44/45 (CHA CHK1B) (2/5)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT No.							
	’02’							
41	MMC::ERRSTS							
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
43	MMC::CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2 CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
44	MMC::CHK1BADRS							
	Address when CHK1B occurred							
45	MMC::CHK1BADRS							
	Address when CHK1B occurred							
46	MMC::CHK1BADRS							
	Address when CHK1B occurred							
47	MMC::CHK1BADRS							
	Address when CHK1B occurred						WR/RD flag in CHK1B	Command/ Data flag in CHK1B
48	MMC::CHK1BBE							
	Not used	Not used	Not used	Not used	I960BE0 in CHK1B	I960BE1 in CHK1B	I960BE2 in CHK1B	I960BE3 in CHK1B
49	MMC::MICPERSTS							
	Not used	Not used	Not used	Not used	Data parity err in MMC <00-07>	Data parity err in MMC <10-17>	Data parity err in MMC <20-27>	Data parity err in MMC <30-37>
4A	MMC::XRADRPERR							
	Not used	Not used	Not used	XR bus address parity error reset				
				<30-35, BE>	<Byte 0>	<Byte 1>	<Byte 2>	<Byte 3>
4B	MMC::XBUSDTPERR							
	Not used	Not used	Not used	Not used	XR bus data parity error <00-07>	XR bus data parity error <10-17>	XR bus data parity error <20-27>	XR bus data parity error <30-37>
4C	MMC::LAST1IP							
	Last address before CHK1A occured							
4D	MMC::LAST1IP							
	Last address before CHK1A occured							
4E	MMC::LAST1IP							
	Last address before CHK1A occurred							
4F	MMC::LAST1IP							
	Last address before CHK1A occurred				Not used	Not used	Not used	Not used

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 44/45 (CHA CHK1B) (3/5)

	0	1	2	3	4	5	6	7
50	MMC::LAST2IP							
	Address one generation older than the last one before CHK1A occurred							
51	MMC::LAST2IP							
	Address one generation older than the last one before CHK1A occurred							
52	MMC::LAST2IP							
	Address one generation older than the last one before CHK1A occurred							
53	MMC::LAST2IP							
	Address one generation older than the last one before CHK1A occurred				Not used	Not used	Not used	Not used
54	MMC::LAST1							
	Last execution address before CHK1A occurred							
55	MMC::LAST1							
	Last execution address before CHK1A occurred							
56	MMC::LAST1							
	Last execution address before CHK1A occurred							
57	MMC::LAST1							
	Last execution address before CHK1A occurred				Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address
58	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred							
59	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred							
5A	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred							
5B	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred				Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address
5C	MMC::LBUSPERR							
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>
5D	MMC::TIMERR							
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Not used
5E	MMC::CHK3STS							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CHK3 error in SMP, LSI
5F	MMC::RSTSTS							
	Not used	Not used	Micro CHK1B occurred	Micro CHK1A occurred	Micro MCNRST2 occurred	Micro MCNRST1 occurred	Micro MPRST occurred	Micro MNTRST occurred

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 44/45 (CHA CHK1B) (4/5)

	0	1	2	3	4	5	6	7
60	MMC::RSTSTS							
	Not used	Not used	SCAN mode set occurred	CHK1A occurred	WCHK1 occurred	SELRST occurred	SYSRST occurred	Power-on reset occurred
61	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
62	MPA::XWER							
	Access to not use address	Access to not use address	Access to not use address	Not used	Not used	Not used	Not used	XR byte access error
63	MPA::XWER							
	XR write address parity error				XR write data parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
64	MPA::XRER							
	Not used	Not used	Not used	Not used	XR read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3
65	MPA::CNT00/01ER							
	CNT#00 parity error				CNT#01 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
66	MPA::CNT02/03ER							
	CNT#02 parity error				CNT#03 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
67	MPA::CNT04/05ER							
	CNT#04 parity error				CNT#05 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
68	MPA::CNT06/07ER							
	CNT#06 parity error				CNT#07 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
69	MPA::CNT08/09ER							
	CNT#08 parity error				CNT#09 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
6A	MPA::CNT10/11ER							
	CNT#10 parity error				CNT#11 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
6B	MPA::CNT12/13ER							
	CNT#12 parity error				CNT#13 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
6C	MPA::CNT14ER							
	CNT#14 parity error				Not used	Not used	Not used	Not used
	Byte 0	Byte 1	Byte 2	Byte 3				
6D	MPA::CWER							
	Not used	Not used	Not used	Not used	Not used	Access to not use register	Access to not use register	Access to not use register
6E	MPA:: CWER							
	COM_IF write address parity error				COM_IF write data parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
6F	MPA::CRER							
	Not used	Not used	Not used	Not used	COM_IF read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 44/45 (CHA CHK1B) (5/5)

	0	1	2	3	4	5	6	7
70		MPA::MPID						
		PKID#			Not used	Not used	MPID#	
71		MPA::REV						
		Chip revision of MPA_LSI						
72								
		Not used						
73		XCLM::CHK1B						
	EXCHANGE Start area PNT underflow	SYSRST REQ AREA PNT underflow	REQIN REQ AREA PNT underflow	Not used	SVC Control ERR	SVC Counter Parity ERR	Not used	Not used
74		XCLM::XFC						
	Data XFR Enable Flag	Data XFR Execute	Not used	Not used	Not used	Inhibit CBP PNT INC	CACHE I/O mode	SSD mode
75		XCLM::XFC						
	Data transfer path	Data transfer path	Data transfer path	Data transfer path	504B sublock format	Not used	Not used	WR FBA mode
76		XCLM::FCHD1L						
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
77		XCLM::XFS0						
	Data transfer end	CCW Transfer end	WT Sync XFR	Always ‘1’	CHK2 occurred	CHK2A occurred	CHK2B occurred	CHK2C occurred
78		XCLM::XFS0						
	CHK2D occurred	TRUNCATION	HALT I/O	SEARCH DASD=CPU	SEARCH DASD>CPU	SEARCH DASD<CPU	I/O short in XFR	Micro ABORT XFR END
79		XCLM::XFS1						
	Not used	Not used	Not used	Not used	MICRO ABORT	ABORT by HW	Pseud CHK1	Pseud CHK2
7A		XCLM::XFS1						
	NEXT SEG ADR STATUS	Not used	Not used	Not used	Not used	NEXT SEG ADR WAIT	PFC Value0	Not used
7B		XCLM::CHK1B						
	IA0 PARITY ERROR	IA1 PARITY ERROR	IA2 PARITY ERROR	IA3 PARITY ERROR	ID0 PARITY ERROR	ID1 PARITY ERROR	ID2 PARITY ERROR	ID3 PARITY ERROR
7C		XCLM::CHK1B						
	OD0 PARITY ERROR	OD1 PARITY ERROR	OD2 PARITY ERROR	OD3 PARITY ERROR	Not used	Not used	CBF CHK1B	PK CHK1B
7D		XCLM::CK21						
	LCM Receive data Parity error	ADR Parity ERR in recv COMM data	Data Parity ERR in recv COMM data	SEQ Parity ERR in LCP COMM	Not used	Not used	Not used	Not used
7E		XCLM::CK22						
	LCMA data parity error	LCMB data parity error	LCMC data parity error	LCMD data parity error	LCME data parity error	LCMF data parity error	LCMG data parity error	LCMH data parity error
7F		XCLM::LSTA						
	LCP BUSY	LCP stop	LCP compare addr through	Tracer STOP	LINK failure	SET LCP WCHK1	SET LCP PATH DSBL	Serial/ Parallel flag

Copyright ©2000,2001, Hitachi, Ltd.

Format 8, Message E (Processor failure: CHA CHK1B)

	0	1	2	3	4	5	6	7
28	SubCode (x'45' : FICON CHK1B)							
29	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHK1B in CHA/ QDTA	CHK1B in MPA	CHK1B in MMC
2A	MMC::CHK1BSTS							
	XR0(ADP/ FCA/SCCA0) CHK1B	XR1(SCA1) CHK1B	XR2 CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in Dram Controller
2B	XLCM::CHK1B							
	IA0 PARITY ERROR	IA1 PARITY ERROR	IA2 PARITY ERROR	IA3 PARITY ERROR	ID0 PARITY ERROR	ID1 PARITY ERROR	ID2 PARITY ERROR	ID3 PARITY ERROR
2C	XLCM::CHK1B							
	OD0 PARITY ERROR	OD1 PARITY ERROR	OD2 PARITY ERROR	OD3 PARITY ERROR	Not used	Not used	CBF CHK1B	PL CHK1B
2D	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
2E	MMC::MICCHK1STS							
	XR decoder error (90)	XR decoder error (91)	MPCHK Counter Parity error	Parity error in MMC internal bus	MPU reset Counter Parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2F	MMC::MICCHK1STS							
	LAN Hold time-out	Wait time-out	XR decoder error	Not used	Not used	XR address Parity error	Local bus Data parity error	XR bus Data Parity error
30	MMC::XRADRSPER							
	XR bus address parity error set 14-17	XR bus address parity error set 24-27	XR bus address parity error set 30-35 BE1	XR bus address parity error set 30-35 BE0	XR bus address parity error (BYTE0-3)			
31	MMC::XBUSDTPER							
	Not used	Not used	Not used	Not used	XR bus Read data parity error <00-07>	XR bus Read data parity error <10-17>	XR bus Read data parity error <20-27>	XR bus Read data parity error <30-37>

Copyright ©2001, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHA CHK1B) Byte28-31 Detail

(1) ESCON CHK1B

	0	1	2	3	4	5	6	7
28	Subcode x'44': ESCON CHK1B							
29	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A	MMC::CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B	XLCM::CK1B							
	IA0 parity error	Not used	IA2 parity error	IA3 parity error	ID0 parity error	ID1 parity error	ID2 parity error	ID3 parity error
2C	XLCM::CK1B							
	OD0 parity error	OD1 parity error	OD2 parity error	OD3 parity error	Not used	Not used	CHK1B in CBF	CHK1B in PL
2D	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
2E	MMC::MICCHK1STS							
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2F	MMC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error
30	MMC::XRADRSPER							
	XR bus address parity error set				XR bus address parity error reset (Byte0-3)			
	14-17	24-27	30-35 BE1	30-35 BE0				
31	MMC::XBUSDTPER							
	Not used	Not used	Not used	Not used	XR bus data parity error <00-07>	XR bus data parity error <10-17>	XR bus data parity error <20-27>	XR bus data parity error <30-37>

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 42-43/52 (CHA CHK1B) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder addres (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Hardware information (See following pages)							
|								
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Sympton code (x‘FF8E’ : LDEV type = 6587/x‘EF8E’ : LDEV type = 6586)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 42-43/52(CHA CHK1B) (2/5)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT No.							
	'03'							
41	MMC::ERRSTS							
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
43	MMC::CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2 CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
44	MMC::CHK1BADRS							
	Address when CHK1B occurred							
45	MMC::CHK1BADRS							
	Address when CHK1B occurred							
46	MMC::CHK1BADRS							
	Address when CHK1B occurred							
47	MMC::CHK1BADRS							
	Address when CHK1B occurred						WR/RD flag in CHK1B	Command/ Data flag in CHK1B
48	MMC::CHK1BBE							
	Not used	Not used	Not used	Not used	I960BE0 in CHK1B	I960BE1 in CHK1B	I960BE2 in CHK1B	I960BE3 in CHK1B
49	MMC::MICPERSTS							
	Not used	Not used	Not used	Not used	Data parity err in MMC <00-07>	Data parity err in MMC <10-17>	Data parity err in MMC <20-27>	Data parity err in MMC <30-37>
4A	MMC::XRADRPERR							
	Not used	Not used	Not used	XR bus address parity error reset				
				<30-35, BE>	<Byte 0>	<Byte 1>	<Byte 2>	<Byte 3>
4B	MMC::XBUSDTPERR							
	Not used	Not used	Not used	Not used	XR bus data parity error <00-07>	XR bus data parity error <10-17>	XR bus data parity error <20-27>	XR bus data parity error <30-37>
4C	MMC::LAST1IP							
	Last address before CHK1A occured							
4D	MMC::LAST1IP							
	Last address before CHK1A occured							
4E	MMC::LAST1IP							
	Last address before CHK1A occurred							
4F	MMC::LAST1IP							
	Last address before CHK1A occurred				Not used	Not used	Not used	Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 42-43/52(CHA CHK1B) (3/5)

	0	1	2	3	4	5	6	7
50		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
51		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
52		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
53		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred			Not used	Not used	Not used	Not used
54		MMC::LAST1						
		Last execution address before CHK1A occurred						
55		MMC::LAST1						
		Last execution address before CHK1A occurred						
56		MMC::LAST1						
		Last execution address before CHK1A occurred						
57		MMC::LAST1						
		Last execution address before CHK1A occurred			Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address
58		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred						
59		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred						
5A		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred						
5B		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred			Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address
5C		MMC::LBUSPERR						
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>
5D		MMC::TIMERR						
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Not used
5E		MMC::CHK3STS						
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CHK3 error in SMP, LSI
5F		MMC::RSTSTS						
	Not used	Not used	Micro CHK1B occurred	Micro CHK1A occurred	Micro MCNRST2 occurred	Micro MCNRST1 occurred	Micro MPRST occurred	Micro MNTRST occurred

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 42-43/52 (CHA CHK1B) (4/5)

	0	1	2	3	4	5	6	7
60	MMC::RSTSTS							
	Not used	Not used	SCAN mode set occurred	CHK1A occurred	WCHK1 occurred	SELRST occurred	SYSRST occurred	Power-on reset occurred
61	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
62	MPA::XWER							
	Access to not use address	Access to not use address	Access to not use address	Not used	Not used	Not used	Not used	XR byte access error
63	MPA::XWER							
	XR write address parity error				XR write data parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
64	MPA::XRER							
	Not used	Not used	Not used	Not used	XR read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3
65	MPA::CNT00/01ER							
	CNT#00 parity error				CNT#01 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
66	MPA::CNT02/03ER							
	CNT#02 parity error				CNT#03 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
67	MPA::CNT04/05ER							
	CNT#04 parity error				CNT#05 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
68	MPA::CNT06/07ER							
	CNT#06 parity error				CNT#07 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
69	MPA::CNT08/09ER							
	CNT#08 parity error				CNT#09 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
6A	MPA::CNT10/11ER							
	CNT#10 parity error				CNT#11 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
6B	MPA::CNT12/13ER							
	CNT#12 parity error				CNT#13 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
6C	MPA::CNT14ER							
	CNT#14 parity error				Not used	Not used	Not used	Not used
	Byte 0	Byte 1	Byte 2	Byte 3				
6D	MPA::CWER							
	Not used	Not used	Not used	Not used	Not used	Access to not use register	Access to not use register	Access to not use register
6E	MPA:: CWER							
	COM_IF write address parity error				COM_IF write data parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
6F	MPA::CRER							
	Not used	Not used	Not used	Not used	COM_IF read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 42-43/52 (CHA CHK1B) (5/5)

	0	1	2	3	4	5	6	7
70	MPA::MPID							
	PKID#				Not used	Not used	MPID#	
71	MPA::REV							
	Chip revision of MPA_LSI							
72	Not used							
73	Not used							
74	LPA::PNLCK2A							
	LBUS write parity error	LBUS read parity error	LBUS time over	Not used	Not used	Not used	Not used	Not used
75	LPA::PNCSTA							
	PCI local bus data parity error	Devsel timing	Devsel timing	Not used	Target abort occurred	Master abort occurred	PCI local bus address parity error	PCI local bus parity error
76	LPA::PNISTAT							
	PLDB bit 31,32 sum data	Data transferring circuit end in LPA LSI	Assert detected data transferring in FBUS	LPA LSI assert	CHK2 occurred #0	CHK2 occurred #1	CHK2 occurred #2	CHK2 occurred #3
77	LPA::PNISTAT							
	CHK2 occurred #4	Not used	Not used	Not used	Not used	Not used	Not used	Not used
78	Not used							
79	Not used							
7A	Not used							
7B	Not used							
7C	Not used							
7D	Not used							
7E	Not used							
7F	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHA CHK1B) Byte28-31 Detail

(2) MPA CHK1B

	0	1	2	3	4	5	6	7
28	Subcode x'42': MPA CHK1B							
29	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A	MMC::CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
2C	MPA::XWER							
	Access to not use address	Access to not use address	Access to not use address	Not used	Not used	Not used	Not used	XR byte access error
2D	MPA::XWER							
	XR write address parity error				XR write data parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
2E	MPA::XRER							
	Not used	Not used	Not used	Not used	XR read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3
2F	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
30	MMC::MICCHK1STS							
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
31	MMC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHA CHK1B) Byte28-31 Detail

(3) LPA CHK1B

	0	1	2	3	4	5	6	7
28	Subcode x'43': LPA CHK1B							
29	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A	MMC::CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B	LPA::PNLCK2A							
	LBUS write parity error	LBUS read parity error	LBUS time over	Not used	Not used	Not used	Not used	Not used
2C	Not used							
2D	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
2E	MMC::MICCHK1STS							
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2F	MMC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (29A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error
30	MMC::XRADRSPER							
	XR bus address parity error set				XR bus address parity error reset			
	14-17	24-27	30-35 BE1	30-35 BE0	Byte0	Byte1	Byte2	Byte3
31	MMC::XBUSDTPER							
	Not used	Not used	Not used	Not used	XR bus data parity error			
					<00-07>	<10-17>	<20-27>	<30-37>

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHA CHK1B) Byte28-31 Detail

(4) MPA CHK1B

	0	1	2	3	4	5	6	7
28	Subcode x'52': MPA CHK1B							
29	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A	MMC::CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
2C	MPA::XWER							
	Access to not use address	Access to not use address	Access to not use address	Not used	Not used	Not used	Not used	XR byte access error
2D	MPA::XWER							
	XR write address parity error				XR write data parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
2E	MPA::XRER							
	Not used	Not used	Not used	Not used	XR read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3
2F	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
30	MMC::MICCHK1STS							
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
31	MMC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 48-49/58-5B/FF (CHK1B) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder addres (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Hardware information (See following pages)							
|								
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Sympton code (x‘FF8E’ : LDEV type = 6587/x‘EF8E’ : LDEV type = 6586)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 48-49/58-5B/FF (CHK1B) (2/5)

	0	1	2	3	4	5	6	7
40		FREE AREA FORMAT No.						
		'04'						
41		MMC::ERRSTS						
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42		MMC::CHK1BSTS						
	Not used	Not used	Not used	Not used	Not used	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
43		MMC::CHK1BSTS						
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2 CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
44		MMC::CHK1BADRS						
		Address when CHK1B occurred						
45		MMC::CHK1BADRS						
		Address when CHK1B occurred						
46		MMC::CHK1BADRS						
		Address when CHK1B occurred						
47		MMC::CHK1BADRS						
		Address when CHK1B occurred					WR/RD flag in CHK1B	Command/ Data flag in CHK1B
48		MMC::CHK1BBE						
	Not used	Not used	Not used	Not used	I960BE0 in CHK1B	I960BE1 in CHK1B	I960BE2 in CHK1B	I960BE3 in CHK1B
49		MMC::MICPERSTS						
	Not used	Not used	Not used	Not used	Data parity err in MMC <00-07>	Data parity err in MMC <10-17>	Data parity err in MMC <20-27>	Data parity err in MMC <30-37>
4A		MMC::XRADRPERR						
	Not used	Not used	Not used	XR bus address parity error reset				
				<30-35, BE>	<Byte 0>	<Byte 1>	<Byte 2>	<Byte 3>
4B		MMC::XBUSDTPERR						
	Not used	Not used	Not used	Not used	XR bus data parity error <00-07>	XR bus data parity error <10-17>	XR bus data parity error <20-27>	XR bus data parity error <30-37>
4C		MMC::LAST1IP						
		Last address before CHK1A occured						
4D		MMC::LAST1IP						
		Last address before CHK1A occured						
4E		MMC::LAST1IP						
		Last address before CHK1A occurred						
4F		MMC::LAST1IP						
		Last address before CHK1A occurred			Not used	Not used	Not used	Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 48-49/58-5B/FF (CHK1B) (3/5)

	0	1	2	3	4	5	6	7
50	MMC::LAST2IP							
	Address one generation older than the last one before CHK1A occurred							
51	MMC::LAST2IP							
	Address one generation older than the last one before CHK1A occurred							
52	MMC::LAST2IP							
	Address one generation older than the last one before CHK1A occurred							
53	MMC::LAST2IP							
	Address one generation older than the last one before CHK1A occurred				Not used	Not used	Not used	Not used
54	MMC::LAST1							
	Last execution address before CHK1A occurred							
55	MMC::LAST1							
	Last execution address before CHK1A occurred							
56	MMC::LAST1							
	Last execution address before CHK1A occurred							
57	MMC::LAST1							
	Last execution address before CHK1A occurred				Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address
58	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred							
59	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred							
5A	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred							
5B	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred				Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address
5C	MMC::LBUSPERR							
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>
5D	MMC::TIMERR							
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Not used
5E	MMC::CHK3STS							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CHK3 error in SMP, LSI
5F	MMC::RSTSTS							
	Not used	Not used	Micro CHK1B occurred	Micro CHK1A occurred	Micro MCNRST2 occurred	Micro MCNRST1 occurred	Micro MPRST occurred	Micro MNTRST occurred

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 48-49/58-5B/FF (CHK1B) (4/5)

	0	1	2	3	4	5	6	7
60	MMC::RSTSTS							
	Not used	Not used	SCAN mode set occurred	CHK1A occurred	WCHK1 occurred	SELRST occurred	SYSRST occurred	Power-on reset occurred
61	MMC::DRAMC1BSTS							
	960→LM access Correctable errors are over the specified time		I960 XR read incorrect address	I960 XR write incorrect address	Not used	Not used	Not used	Not used
	Bank 0	Bank 1						
62	MMC::DRAMC1BSTS							
	LANC→LM access Correctable errors are over the specified time		LANC→LM access Uncorrectable error detected		LANC→XR incorrect address	Not used	Not used	Not used
	Bank 0	Bank 1	Bank 0	Bank 1				
63	MMC::DRAMC1BSTS							
	Not used	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
64	MMC::ERADR							
	Address from L bus							
65	MMC::ERADR							
	Address from L bus							
66	MMC::ERADR							
	Address from L bus							
67	MMC::ERADR							
	Address from L bus						Not used	Not used
68	MMC::ERBYT							
	Not used	Not used	DRAM control signal RAMADR error	DRAM control signal RAS error	DRAM control signal BAS error	DRAM control signal CAS error	DRAM control signal WE error	DRAM control signal DQM error
69	MMC::ERORD							
	Data before correction							
6A	MMC::ERORD							
	Data before correction							
6B	MMC::ERORD							
	Data before correction							
6C	MMC::ERORD							
	Data before correction							
6D	MMC::ERORC							
	Check bit before correction							
6E	MMC::ERORC							
	Check bit before correction							
6F	MPA::ERCRD							
	Data after correction							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 48-49/58-5B/FF (CHK1B) (5/5)

	0	1	2	3	4	5	6	7
70		MPA::ERCRD						
		Data after correction						
71		MPA::ERCRD						
		Data after correction						
72		MPA::ERCRD						
		Data after correction						
73		MPA::ERCRC						
		Check bit after correction						
74		MPA::ERCRC						
		Check bit after correction						
75		MMC::ERRSYD						
		Syndrome before correction						
76		MMC::ERRSYD						
		Syndrome before correction						
77		MMC::ERWA						
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	WR signal value
78		MMC::CECNT						
		Correctable error counter(Low)						
79		MMC::CECNT						
		Correctable error counter(High)						
7A		MMC::RCVINT						
	Not used	Not used	Not used	CLPON signal monitor bit	SCP0 signal monitor bit	SCP1 signal monitor bit	DRR MP0 signal monitor bit	DRR MP1 signal monitor bit
7B		MMC::RCVINT						
	SYSRST signal monitor bit	SELRST signal monitor bit	CHK1A signal monitor bit	CHK1B signal monitor bit	SMP signal monitor bit	LAN/SI0 signal monitor bit	CHA/DRR signal monitor bit	ADP/SCA0 signal monitor bit
7C		MMC::RCVINT						
	Not used	CHK3 signal monitor bit	Not used	SCA1 signal monitor bit	SCA2 signal monitor bit	SCA3 signal monitor bit	SCA4 signal monitor bit	SCA5 signal monitor bit
7D		MMC::RCVINT						
	TIMER0 signal monitor bit	TIMER1 signal monitor bit	TIMER2 signal monitor bit	TIMER3 signal monitor bit	TIMER4 signal monitor bit	TIMER5 signal monitor bit	TIMER6 signal monitor bit	SYNC STOP signal monitor bit
7E		MPA::MPASTS						
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
7F		LPA::PNLCK2A						
	LBUS write parity error	LBUS read parity error	LBUS time over	Not used	Not used	Not used	Not used	Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHA CHK1B) Byte28-31 Detail

(5) MMC CHK1B

	0	1	2	3	4	5	6	7
28		Subcode x'48': MMC CHK1B						
29		MMC::CHK1BSTS						
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A		MMC:: CHK1BSTS						
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B		MMC::MICCHK1STS						
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
2C		MMC::MICCHK1STS						
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2D		MMC::MICCHK1STS						
	LAN hold time-out	Wait time-out	XR decoder error (29A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error
2E		MMC::MPCERRSTS						
	Not used	Not used	WCHK1 at MPCHK	CHK1A at MPCHK	Timeout monitor timer parity error	A/B REG inconsistent check error	A/B REG write time-out	A/B REG access sequence error
2F		MMC::MMCPERR						
	Not used	Not used	Not used	Not used	Data parity err in MMC <00-07>	Data parity err in MMC <10-17>	Data parity err in MMC <20-27>	Data parity err in MMC <30-37>
30		MMC::TIMERR						
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Not used
31		MMC::LBUSPER						
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHA CHK1B) Byte28-31 Detail

(6) MMC DRAM CHK1B

	0	1	2	3	4	5	6	7
28	Subcode x'49': MMC DRAM CHK1B							
29	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A	MMC:: CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B	MMC::DRAMC1BSTS							
	i960→LM access Correctable errors are over the specified time		I960 XR read incorrect address	I960 XR write incorrect address	Not used	Not used	Not used	Not used
	Bank 0	Bank 1						
2C	MMC::DRAMC1BSTS							
	LANC→LM access Correctable errors are over the specified time		LANC→LM access Uncorrectable error detected		LANC→XR incorrect address	Not used	Not used	Not used
	Bank 0	Bank 1	Bank 0	Bank 1				
2D	MMC::DRAMC1BSTS							
	Parity error at refresh addr reg	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
2E	MMC::ERADR							
	Address from L bus							
2F	MMC::ERADR							
	Address from L bus							
30	MMC::ERADR							
	Address from L bus							
31	MMC::ERADR							
	Address from L bus						Not used	Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHA CHK1B) Byte28-31 Detail

(7) MMC CHK1B

	0	1	2	3	4	5	6	7
28		Subcode x'58': MMC CHK1B						
29		MMC::CHK1BSTS						
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A		MMC:: CHK1BSTS						
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B		MMC::MICCHK1STS						
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
2C		MMC::MICCHK1STS						
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2D		MMC::MICCHK1STS						
	LAN hold time-out	Wait time-out	XR decoder error (29A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error
2E		MMC::MPCERRSTS						
	Not used	Not used	WCHK1 at MPCHK	CHK1A at MPCHK	Timeout monitor timer parity error	A/B REG inconsistent check error	A/B REG write time-out	A/B REG access sequence error
2F		MMC::MMCPERR						
	Not used	Not used	Not used	Not used	Data parity err in MMC <00-07>	Data parity err in MMC <10-17>	Data parity err in MMC <20-27>	Data parity err in MMC <30-37>
30		MMC::TIMERR						
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Not used
31		MMC::LBUSPER						
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHA CHK1B) Byte28-31 Detail

(8) MMC DRAM CHK1B

	0	1	2	3	4	5	6	7
28	Subcode x'59': MMC DRAM CHK1B							
29	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A	MMC:: CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B	MMC::DRAMC1BSTS							
	i960→LM access Correctable errors are over the specified time		I960 XR read incorrect address	I960 XR write incorrect address	Not used	Not used	Not used	Not used
	Bank 0	Bank 1						
2C	MMC::DRAMC1BSTS							
	LANC→LM access Correctable errors are over the specified time		LANC→LM access Uncorrectable error detected		LANC→XR incorrect address	Not used	Not used	Not used
	Bank 0	Bank 1	Bank 0	Bank 1				
2D	MMC::DRAMC1BSTS							
	Parity error at refresh addr reg	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
2E	MMC::ERADR							
	Address from L bus							
2F	MMC::ERADR							
	Address from L bus							
30	MMC::ERADR							
	Address from L bus							
31	MMC::ERADR							
	Address from L bus						Not used	Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHA CHK1B) Byte28-31 Detail

(9) I960 read data parity error

	0	1	2	3	4	5	6	7
28	Subcode x'5A': I960 read data parity error							
29	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A	MMC:: CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B	MMC::MICCHK1STS							
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2C	MMC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (29A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error
2D	MMC::MPCERRSTS							
	Not used	Not used	WCHK1 at MPCHK	CHK1A at MPCHK	Timeout monitor timer parity error	A/B REG inconsistent check error	A/B REG write time-out	A/B REG access sequence error
2E	MMC::DRAMC1BSTS							
	i960→LM access Correctable errors are over the specified time		I960 XR read incorrect address	I960 XR write incorrect address	Not used	Not used	Not used	Not used
	Bank 0	Bank 1						
2F	MMC::DRAMC1BSTS							
	LANC→LM access Correctable errors are over the specified time		LANC→LM access Uncorrectable error detected		LANC→XR incorrect address	Not used	Not used	Not used
	Bank 0	Bank 1	Bank 0	Bank 1				
30	MMC::DRAMC1BSTS							
	Parity error at refresh addr reg	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
31	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHA CHK1B) Byte28-31 Detail

(10) LANC read data parity error

	0	1	2	3	4	5	6	7
28	Subcode x'5B': LANC read data parity error							
29	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A	MMC:: CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B	MMC::MICCHK1STS							
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2C	MMC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (29A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error
2D	MMC::MPCERRSTS							
	Not used	Not used	WCHK1 at MPCHK	CHK1A at MPCHK	Timeout monitor timer parity error	A/B REG inconsistent check error	A/B REG write time-out	A/B REG access sequence error
2E	MMC::DRAMC1BSTS							
	i960→LM access Correctable errors are over the specified time		I960 XR read incorrect address	I960 XR write incorrect address	Not used	Not used	Not used	Not used
	Bank 0	Bank 1						
2F	MMC::DRAMC1BSTS							
	LANC→LM access Correctable errors are over the specified time		LANC→LM access Uncorrectable error detected		LANC→XR incorrect address	Not used	Not used	Not used
	Bank 0	Bank 1	Bank 0	Bank 1				
30	MMC::DRAMC1BSTS							
	Parity error at refresh addr reg	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
31	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHA CHK1B) Byte28-31 Detail

(11) CHK1B

	0	1	2	3	4	5	6	7
28	Subcode x'FF': CHK1B undefined hardware reason							
29	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/DRR	CHK1B in SMP	CHK1B in MIC
2A	MMC::CHK1BSTS							
	XR0(SCA#0) CHK1B	XR1(SCA#1) CHK1B	XR2(SCA#2) CHK1B	XR3(SCA#3) CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B	Not used							
2C	Not used							
2D	Not used							
2E	Not used							
2F	Not used							
30	Not used							
31	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 4A (CHA CHK1B) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder addres (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode (x‘45’ ~ x‘46’/x‘55’ ~ x‘58’)							
29	Hardware information (See following pages)							
|								
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Sympton code (x‘FF8E’ : LDEV type = 6587/x‘EF8E’ : LDEV type = 6586)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 4A (CHK1B) (2/5)

	0	1	2	3	4	5	6	7
40		FREE AREA FORMAT No.						
		'05'						
41		MMC::ERRSTS						
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42		MMC::CHK1BSTS						
	Not used	Not used	Not used	Not used	Not used	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
43		MMC::CHK1BSTS						
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2 CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
44		MMC::CHK1BADRS						
		Address when CHK1B occurred						
45		MMC::CHK1BADRS						
		Address when CHK1B occurred						
46		MMC::CHK1BADRS						
		Address when CHK1B occurred						
47		MMC::CHK1BADRS						
		Address when CHK1B occurred					WR/RD flag in CHK1B	Command/ Data flag in CHK1B
48		MMC::CHK1BBE						
	Not used	Not used	Not used	Not used	I960BE0 in CHK1B	I960BE1 in CHK1B	I960BE2 in CHK1B	I960BE3 in CHK1B
49		MMC::MICPERSTS						
	Not used	Not used	Not used	Not used	Data parity err in MMC <00-07>	Data parity err in MMC <10-17>	Data parity err in MMC <20-27>	Data parity err in MMC <30-37>
4A		MMC::XRADRPERR						
	Not used	Not used	Not used	XR bus address parity error reset				
				<30-35, BE>	<Byte 0>	<Byte 1>	<Byte 2>	<Byte 3>
4B		MMC::XBUSDTPERR						
	Not used	Not used	Not used	Not used	XR bus data parity error <00-07>	XR bus data parity error <10-17>	XR bus data parity error <20-27>	XR bus data parity error <30-37>
4C		MMC::LAST1IP						
		Last address before CHK1A occured						
4D		MMC::LAST1IP						
		Last address before CHK1A occured						
4E		MMC::LAST1IP						
		Last address before CHK1A occurred						
4F		MMC::LAST1IP						
		Last address before CHK1A occurred			Not used	Not used	Not used	Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 4A (CHK1B) (3/5)

	0	1	2	3	4	5	6	7
50		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
51		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
52		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
53		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred			Not used	Not used	Not used	Not used
54		MMC::LAST1						
		Last execution address before CHK1A occurred						
55		MMC::LAST1						
		Last execution address before CHK1A occurred						
56		MMC::LAST1						
		Last execution address before CHK1A occurred						
57		MMC::LAST1						
		Last execution address before CHK1A occurred			Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address
58		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred						
59		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred						
5A		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred						
5B		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred			Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address
5C		MMC::LBUSPERR						
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>
5D		MMC::TIMERR						
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Not used
5E		MMC::CHK3STS						
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CHK3 error in SMP, LSI
5F		MMC::RSTSTS						
	Not used	Not used	Micro CHK1B occurred	Micro CHK1A occurred	Micro MCNRST2 occurred	Micro MCNRST1 occurred	Micro MPRST occurred	Micro MNTRST occurred

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 4A (CHK1B) (4/5)

	0	1	2	3	4	5	6	7
60	MMC::RSTSTS							
	Not used	Not used	SCAN mode set occurred	CHK1A occurred	WCHK1 occurred	SELRST occurred	SYSRST occurred	Power-on reset occurred
61	MMC::DRAMC1BSTS							
	960→LM access Correctable errors are over the specified time		I960 XR read incorrect address	I960 XR write incorrect address	Not used	Not used	Not used	Not used
	Bank 0	Bank 1						
62	MMC::DRAMC1BSTS							
	LANC→LM access Correctable errors are over the specified time		LANC→LM access Uncorrectable error detected		LANC→XR incorrect address	Not used	Not used	Not used
	Bank 0	Bank 1	Bank 0	Bank 1				
63	MMC::DRAMC1BSTS							
	Not used	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
64	MMC::FERADR							
	Address from L bus (fetch)							
65	MMC::FERADR							
	Address from L bus (fetch)							
66	MMC::FERADR							
	Address from L bus (fetch)							
67	MMC::FERADR							
	Address from L bus (fetch)						Not used	Not used
68	MMC::FERBYT							
	Not used	Not used	DRAM control signal RAMADR error	DRAM control signal RAS error	DRAM control signal BAS error	DRAM control signal CAS error	DRAM control signal WE error	DRAM control signal DQM error
69	MMC::FERORD							
	Data before correction (fetch)							
6A	MMC::FERORD							
	Data before correction (fetch)							
6B	MMC::FERORD							
	Data before correction (fetch)							
6C	MMC::FERORD							
	Data before correction (fetch)							
6D	MMC::FERORC							
	Check bit before correction (fetch)							
6E	MMC::FERORC							
	Check bit before correction (fetch)							
6F	MPA::FERCRD							
	Data after correction (fetch)							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 4A (CHK1B) (5/5)

	0	1	2	3	4	5	6	7
70		MPA::FERCRD						
		Data after correction (fetch)						
71		MPA::FERCRD						
		Data after correction (fetch)						
72		MPA::FERCRD						
		Data after correction (fetch)						
73		MPA::FERCRC						
		Check bit after correction (fetch)						
74		MPA::FERCRC						
		Check bit after correction (fetch)						
75		MMC::FERRSYD						
		Syndrome before correction (fetch)						
76		MMC::FERRSYD						
		Syndrome before correction (fetch)						
77		MMC::ERWA						
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	WR signal value
78		MMC::CECNT						
		Correctable error counter(Low)						
79		MMC::CECNT						
		Correctable error counter(High)						
7A		MMC::RCVINT						
	Not used	Not used	Not used	CLPON signal monitor bit	SCP0 signal monitor bit	SCP1 signal monitor bit	DRR MP0 signal monitor bit	DRR MP1 signal monitor bit
7B		MMC::RCVINT						
	SYSRST signal monitor bit	SELRST signal monitor bit	CHK1A signal monitor bit	CHK1B signal monitor bit	SMP signal monitor bit	LAN/SI0 signal monitor bit	CHA/DRR signal monitor bit	ADP/SCA0 signal monitor bit
7C		MMC::RCVINT						
	Not used	CHK3 signal monitor bit	Not used	SCA1 signal monitor bit	SCA2 signal monitor bit	SCA3 signal monitor bit	SCA4 signal monitor bit	SCA5 signal monitor bit
7D		MMC::RCVINT						
	TIMER0 signal monitor bit	TIMER1 signal monitor bit	TIMER2 signal monitor bit	TIMER3 signal monitor bit	TIMER4 signal monitor bit	TIMER5 signal monitor bit	TIMER6 signal monitor bit	SYNC STOP signal monitor bit
7E		MPA::MPASTS						
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
7F		LPA::PNLCK2A						
	LBUS write parity error	LBUS read parity error	LBUS time over	Not used	Not used	Not used	Not used	Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : CHA CHK1B) Byte28-31 Detail

(12) MMC FETCH CHK1B

	0	1	2	3	4	5	6	7
28	Subcode x'4A': MMC FETCH CHK1B							
29	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A	MMC:: CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B	MMC::DRAMC1BSTS							
	i960→LM access Correctable errors are over the specified time		I960 XR read incorrect address	I960 XR write incorrect address	Not used	Not used	Not used	Not used
	Bank 0	Bank 1						
2C	MMC::DRAMC1BSTS							
	LANC→LM access Correctable errors are over the specified time		LANC→LM access Uncorrectable error detected		LANC→XR incorrect address	Not used	Not used	Not used
	Bank 0	Bank 1	Bank 0	Bank 1				
2D	MMC::DRAMC1BSTS							
	Parity error at refresh addr reg	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
2E	MMC::FERADR							
	Error address in fetch to LM							
2F	MMC::FERADR							
	Error address in fetch to LM							
30	MMC::FERADR							
	Error address in fetch to LM							
31	MMC::FERADR							
	Error address in fetch to LM						Not used	Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 60-63/70-73(DKA CHK1B) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder addres (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Hardware information (See following pages)							
|								
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Sympton code (x‘FF8E’ : LDEV type = 6587/x‘EF8E’ : LDEV type = 6586)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 60-63/70-73(DKA CHK1B) (2/5)

	0	1	2	3	4	5	6	7
40		FREE AREA FORMAT No.						
		'06'						
41		MMC::ERRSTS						
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42		MMC::CHK1BSTS						
	Not used	Not used	Not used	Not used	Not used	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
43		MMC::CHK1BSTS						
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2 CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
44		MMC::CHK1BADRS						
		Address when CHK1B occurred						
45		MMC::CHK1BADRS						
		Address when CHK1B occurred						
46		MMC::CHK1BADRS						
		Address when CHK1B occurred						
47		MMC::CHK1BADRS						
		Address when CHK1B occurred					WR/RD flag in CHK1B	Command/ Data flag in CHK1B
48		MMC::CHK1BBE						
	Not used	Not used	Not used	Not used	I960BE0 in CHK1B	I960BE1 in CHK1B	I960BE2 in CHK1B	I960BE3 in CHK1B
49		MMC::MICPERSTS						
	Not used	Not used	Not used	Not used	Data parity err in MMC <00-07>	Data parity err in MMC <10-17>	Data parity err in MMC <20-27>	Data parity err in MMC <30-37>
4A		MMC::XRADRPERR						
	Not used	Not used	Not used	XR bus address parity error reset				
				<30-35, BE>	<Byte 0>	<Byte 1>	<Byte 2>	<Byte 3>
4B		MMC::XBUSDTPERR						
	Not used	Not used	Not used	Not used	XR bus data parity error <00-07>	XR bus data parity error <10-17>	XR bus data parity error <20-27>	XR bus data parity error <30-37>
4C		MMC::LAST1IP						
		Last address before CHK1A occured						
4D		MMC::LAST1IP						
		Last address before CHK1A occured						
4E		MMC::LAST1IP						
		Last address before CHK1A occurred						
4F		MMC::LAST1IP						
		Last address before CHK1A occurred			Not used	Not used	Not used	Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 60-63/70-73(DKA CHK1B) (3/5)

	0	1	2	3	4	5	6	7
50		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
51		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
52		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
53		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred			Not used	Not used	Not used	Not used
54		MMC::LAST1						
		Last execution address before CHK1A occurred						
55		MMC::LAST1						
		Last execution address before CHK1A occurred						
56		MMC::LAST1						
		Last execution address before CHK1A occurred						
57		MMC::LAST1						
		Last execution address before CHK1A occurred			Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address
58		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred						
59		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred						
5A		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred						
5B		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred			Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address
5C		MMC::LBUSPERR						
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>
5D		MMC::TIMERR						
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Not used
5E		MMC::CHK3STS						
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CHK3 error in SMP, LSI
5F		MMC::RSTSTS						
	Not used	Not used	Micro CHK1B occurred	Micro CHK1A occurred	Micro MCNRST2 occurred	Micro MCNRST1 occurred	Micro MPRST occurred	Micro MNTRST occurred

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 60-63/70-73(DKA CHK1B) (4/5)

	0	1	2	3	4	5	6	7
60	MMC::RSTSTS							
	Not used	Not used	SCAN mode set occurred	CHK1A occurred	WCHK1 occurred	SELRST occurred	SYSRST occurred	Power-on reset occurred
61	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
62	MPA::XWER							
	Access to not use address	Access to not use address	Access to not use address	Not used	Not used	Not used	Not used	XR byte access error
63	MPA::XWER							
	XR write address parity error				XR write data parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
64	MPA::XRER							
	Not used	Not used	Not used	Not used	XR read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3
65	MPA::CNT00/01ER							
	CNT#00 parity error				CNT#01 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
66	MPA::CNT02/03ER							
	CNT#02 parity error				CNT#03 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
67	MPA::CNT04/05ER							
	CNT#04 parity error				CNT#05 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
68	MPA::CNT06/07ER							
	CNT#06 parity error				CNT#07 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
69	MPA::CNT08/09ER							
	CNT#08 parity error				CNT#09 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
6A	MPA::CNT10/11ER							
	CNT#10 parity error				CNT#11 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
6B	MPA::CNT12/13ER							
	CNT#12 parity error				CNT#13 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
6C	MPA::CNT14ER							
	CNT#14 parity error				Not used	Not used	Not used	Not used
	Byte 0	Byte 1	Byte 2	Byte 3				
6D	MPA::CWER							
	Not used	Not used	Not used	Not used	Not used	Access to not use register	Access to not use register	Access to not use register
6E	MPA:: CWER							
	COM_IF write address parity error				COM_IF write data parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
6F	MPA::CRER							
	Not used	Not used	Not used	Not used	COM_IF read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 60-63/70-73(DKA CHK1B) (5/5)

	0	1	2	3	4	5	6	7
70		MPA::MPID						
		PKID#			Not used	Not used	MPID#	
71		MPA::REV						
		Chip revision of MPA_LSI						
72		SCA0::SCHK1						
	XR ADR(H) parity error	XR ADR(L) parity error	Write data 0 parity error	Write data 1 parity error	Read data 0 parity error	Read data 1 parity error	Address decode error(H)	Address decode error(L)
73		SCA0::SCHK1						
	8 phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10 phase clock error	Not used	Not used	Not used
74		SCA0::SCHK11						
	SEG parameter error	SEG mode access error	XFC access error	Not used	Not used	Not used	Not used	Not used
75		SCA1::SCHK1						
	XR ADR(H) parity error	XR ADR(L) parity error	Write data 0 parity error	Write data 1 parity error	Read data 0 parity error	Read data 1 parity error	Address decode error(H)	Address decode error(L)
76		SCA1::SCHK1						
	8 phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10 phase clock error	Not used	Not used	Not used
77		SCA1::SCHK11						
	SEG parameter error	SEG mode access error	XFC access error	Not used	Not used	Not used	Not used	Not used
78		DDTA::ESTA9						
	Write to unused register	Write to read-only register	Set A at CMD-A execute	Set B at CMD-B execute	Set C at 64CMD execute	Address2 parity error	Address3 parity error	Byte access error
79		DDTA::ESTA9						
	Input DT0 parity error	Input DT0 parity error	Address DEC parity error	Output DT0 parity error	Output DT1 parity error	DRR4 clock phase error	CHSN4 clock phase error	CHSN6 clock phase error
7A		DDTA::DRSTS						
	Transfer end (A/64CMD)	Not used	(A/64CMD) Exec wait/ Executing	(A/64CMD) Data transferring	Transfer END B	Not used	Command B Exec wait/ Executing	Command B Data transferring
7B		DDTA::DRSTS						
	CHK2 occurred	CHK2 occurred at transferring data	CHK2 in DRR controller	CHK1B in CACHE /CARB	Arbiter/ timer error	CHK1B occurred	Forced data transferring end	Force error occurred
7C		DDTA::P0EST0						
	RX SEQ ERR	PRB RD-PNT P-ERR	RD DT-CNT P-ERR	RD DEF FLG-PNT P-ERR	RD DEF SEQ ERR	RD DEF-CNT P-ERR	WT DEF FLG-PNT P-ERR	WT DT-CNT R
7D		DDTA::P0EST0						
	WT DEF SEQ ERR	WT DEF-CNT P-ERR	PBF WAD-CNT P-ERR	PBF RAD-CNT P-ERR	Not used	Not used	Not used	‡ Not used
7E		DDTA::P1EST1						
	RX SEQ ERR	PRB RD-PNT P-ERR	RD DT-CNT P-ERR	RD DEF FLG-PNT P-ERR	RD DEF SEQ ERR	RD DEF-CNT P-ERR	WT DEF FLG-PNT P-ERR	WT DT-CNT R
7F		DDTA::P1EST1						
	WT DEF SEQ ERR	WT DEF-CNT P-ERR	PBF WAD-CNT P-ERR	PBF RAD-CNT P-ERR	Not used	Not used	Not used	‡ Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : DKA CHK1B) Byte28-31 Detail

(1) SCA0 CHK1B

	0	1	2	3	4	5	6	7
28		Subcode x'60': SCA0 CHK1B						
29		MMC::CHK1BSTS						
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A		MMC::CHK1BSTS						
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B		SCA0::SCHK1						
	XR ADR(H) parity error	XR ADR(L) parity error	Write data 0 parity error	Write data 1 parity error	Read data 0 parity error	Read data 1 parity error	Address decode error(H)	Address decode error(L)
2C		SCA0::SCHK1						
	8 phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10 phase clock error	Not used	Not used	Not used
2D		SCA0::SCHK11						
	SEG parameter error	SEG mode access error	XFC access error	Not used	Not used	Not used	Not used	Not used
2E		Not used						
2F		MMC::MICCHK1STS						
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
30		MMC::MICCHK1STS						
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
31		MMC::MICCHK1STS						
	LAN hold time-out	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure :DKA CHK1B) Byte28-31 Detail

(2) SCA1 CHK1B

	0	1	2	3	4	5	6	7
28		Subcode x'61': MMC CHK1B						
29		MMC::CHK1BSTS						
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A		MMC::CHK1BSTS						
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B		SCA1::SCHK1						
	XR ADR(H) parity error	XR ADR(L) parity error	Write data 0 parity error	Write data 1 parity error	Read data 0 parity error	Read data 1 parity error	Address decode error(H)	Address decode error(L)
2C		SCA1::SCHK1						
	8 phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10 phase clock error	Not used	Not used	Not used
2D		SCA1::SCHK11						
	SEG parameter error	SEG mode access error	XFC access error	Not used	Not used	Not used	Not used	Not used
2E		Not used						
2F		MMC::MICCHK1STS						
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
30		MMC::MICCHK1STS						
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
31		MMC::MICCHK1STS						
	LAN hold time-out	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : DKA CHK1B) Byte28-31 Detail

(3) MPA CHK1B

	0	1	2	3	4	5	6	7
28	Subcode x'62': MPA CHK1B							
29	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A	MMC::CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
2C	MPA::XWER							
	Access to not use address	Access to not use address	Access to not use address	Not used	Not used	Not used	Not used	XR byte access error
2D	MPA::XWER							
	XR write address parity error				XR write data parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
2E	MPA::XRER							
	Not used	Not used	Not used	Not used	XR read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3
2F	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
30	MMC::MICCHK1STS							
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
31	MMC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : DKA CHK1B) Byte28-31 Detail

(4) DDTA CHK1B

	0	1	2	3	4	5	6	7
28		Subcode x'63': DDTA CHK1B						
29		MMC::CHK1BSTS						
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A		MMC::CHK1BSTS						
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B		DDTA::DRSTS						
	Transfer end (A/64CMD)	Not used	(A/64CMD) Exec wait/ Executing	(A/64CMD) Data transferring	Transfer END B	Not used	Command B Exec wait/ Executing	Command B Data transferring
2C		DDTA::DRSTS						
	CHK2 occurred	CHK2 occurred at transferring data	CHK2 in DRR controller	CHK1B in CACHE /CARB	Arbiter/ timer error	CHK1B occurred	Forced data transferring end	Force error occurred
2D		DDTA::ERR						
	DRR control error	P0 control error	P1 control error	DRR DT error	P0 DT error	P1 DT error	P0 CARB/ CMA error	P1 CARB/ CMA error
2E		DDTA::ERR						
	P0 error occurred	P1 error occurred	DT error occurred	Time over error occurred	ST0 Valid	ST1 Valid	P0 use flag (Not error)	P1 use flag (Not error)
2F		Not used						
30		DDTA::ESTA9						
	Write to unused register	Write to read-only register	Set A at CMD-A execute	Set B at CMD-B execute	Set C at 64CMD execute	Address2 parity error	Address3 parity error	Byte access error
31		DDTA::ESTA9						
	Input DT0 parity error	Input DT0 parity error	Address DEC parity error	Output DT0 parity error	Output DT1 parity error	DRR4 clock phase error	CHSN4 clock phase error	CHSN6 clock phase error

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : DKA CHK1B) Byte28-31 Detail

(5) SCA0 CHK1B

	0	1	2	3	4	5	6	7
28		Subcode x'70': SCA0 CHK1B						
29		MMC::CHK1BSTS						
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A		MMC::CHK1BSTS						
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B		SCA0::SCHK1						
	XR ADR(H) parity error	XR ADR(L) parity error	Write data 0 parity error	Write data 1 parity error	Read data 0 parity error	Read data 1 parity error	Address decode error(H)	Address decode error(L)
2C		SCA0::SCHK1						
	8 phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10 phase clock error	Not used	Not used	Not used
2D		SCA0::SCHK11						
	SEG parameter error	SEG mode access error	XFC access error	Not used	Not used	Not used	Not used	Not used
2E		Not used						
2F		MMC::MICCHK1STS						
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
30		MMC::MICCHK1STS						
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
31		MMC::MICCHK1STS						
	LAN hold time-out	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure :DKA CHK1B) Byte28-31 Detail

(6) SCA1 CHK1B

	0	1	2	3	4	5	6	7
28		Subcode x'71': MMC CHK1B						
29		MMC::CHK1BSTS						
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A		MMC::CHK1BSTS						
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B		SCA1::SCHK1						
	XR ADR(H) parity error	XR ADR(L) parity error	Write data 0 parity error	Write data 1 parity error	Read data 0 parity error	Read data 1 parity error	Address decode error(H)	Address decode error(L)
2C		SCA1::SCHK1						
	8 phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10 phase clock error	Not used	Not used	Not used
2D		SCA1::SCHK11						
	SEG parameter error	SEG mode access error	XFC access error	Not used	Not used	Not used	Not used	Not used
2E		Not used						
2F		MMC::MICCHK1STS						
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
30		MMC::MICCHK1STS						
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
31		MMC::MICCHK1STS						
	LAN hold time-out	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : DKA CHK1B) Byte28-31 Detail

(7) MPA CHK1B

	0	1	2	3	4	5	6	7
28	Subcode x'72': MPA CHK1B							
29	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A	MMC::CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
2C	MPA::XWER							
	Access to not use address	Access to not use address	Access to not use address	Not used	Not used	Not used	Not used	XR byte access error
2D	MPA::XWER							
	XR write address parity error				XR write data parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
2E	MPA::XRER							
	Not used	Not used	Not used	Not used	XR read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3
2F	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
30	MMC::MICCHK1STS							
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
31	MMC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : DKA CHK1B) Byte28-31 Detail

(8) DDTA CHK1B

	0	1	2	3	4	5	6	7
28		Subcode x'73': DDTA CHK1B						
29		MMC::CHK1BSTS						
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A		MMC::CHK1BSTS						
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B		DDTA::DRSTS						
	Transfer end (A/64CMD)	Not used	(A/64CMD) Exec wait/ Executing	(A/64CMD) Data transferring	Transfer END B	Not used	Command B Exec wait/ Executing	Command B Data transferring
2C		DDTA::DRSTS						
	CHK2 occurred	CHK2 occurred at transferring data	CHK2 in DRR controller	CHK1B in CACHE /CARB	Arbiter/ timer error	CHK1B occurred	Forced data transferring end	Force error occurred
2D		DDTA::ERR						
	DRR control error	P0 control error	P1 control error	DRR DT error	P0 DT error	P1 DT error	P0 CARB/ CMA error	P1 CARB/ CMA error
2E		DDTA::ERR						
	P0 error occurred	P1 error occurred	DT error occurred	Time over error occurred	ST0 Valid	ST1 Valid	P0 use flag (Not error)	P1 use flag (Not error)
2F		Not used						
30		DDTA::ESTA9						
	Write to unused register	Write to read-only register	Set A at CMD-A execute	Set B at CMD-B execute	Set C at 64CMD execute	Address2 parity error	Address3 parity error	Byte access error
31		DDTA::ESTA9						
	Input DT0 parity error	Input DT0 parity error	Address DEC parity error	Output DT0 parity error	Output DT1 parity error	DRR4 clock phase error	CHSN4 clock phase error	CHSN6 clock phase error

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 68-69/78-7B (DKA CHK1B) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder addres (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Hardware information (See following pages)							
|								
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Sympton code (x‘FF8E’ : LDEV type = 6587/x‘EF8E’ : LDEV type = 6586)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 68-69/78-7B (DKA CHK1B)(2/5)

	0	1	2	3	4	5	6	7
40		FREE AREA FORMAT No.						
		'07'						
41		MMC::ERRSTS						
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42		MMC::CHK1BSTS						
	Not used	Not used	Not used	Not used	Not used	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
43		MMC::CHK1BSTS						
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2 CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
44		MMC::CHK1BADRS						
		Address when CHK1B occurred						
45		MMC::CHK1BADRS						
		Address when CHK1B occurred						
46		MMC::CHK1BADRS						
		Address when CHK1B occurred						
47		MMC::CHK1BADRS						
		Address when CHK1B occurred					WR/RD flag in CHK1B	Command/ Data flag in CHK1B
48		MMC::CHK1BBE						
	Not used	Not used	Not used	Not used	I960BE0 in CHK1B	I960BE1 in CHK1B	I960BE2 in CHK1B	I960BE3 in CHK1B
49		MMC::MICPERSTS						
	Not used	Not used	Not used	Not used	Data parity err in MMC <00-07>	Data parity err in MMC <10-17>	Data parity err in MMC <20-27>	Data parity err in MMC <30-37>
4A		MMC::XRADRPERR						
	Not used	Not used	Not used	XR bus address parity error reset				
				<30-35, BE>	<Byte 0>	<Byte 1>	<Byte 2>	<Byte 3>
4B		MMC::XBUSDTPERR						
	Not used	Not used	Not used	Not used	XR bus data parity error <00-07>	XR bus data parity error <10-17>	XR bus data parity error <20-27>	XR bus data parity error <30-37>
4C		MMC::LAST1IP						
		Last address before CHK1A occured						
4D		MMC::LAST1IP						
		Last address before CHK1A occured						
4E		MMC::LAST1IP						
		Last address before CHK1A occurred						
4F		MMC::LAST1IP						
		Last address before CHK1A occurred			Not used	Not used	Not used	Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 68-69/78-7B(DKA CHK1B) (3/5)

	0	1	2	3	4	5	6	7
50		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
51		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
52		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
53		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred			Not used	Not used	Not used	Not used
54		MMC::LAST1						
		Last execution address before CHK1A occurred						
55		MMC::LAST1						
		Last execution address before CHK1A occurred						
56		MMC::LAST1						
		Last execution address before CHK1A occurred						
57		MMC::LAST1						
		Last execution address before CHK1A occurred			Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address
58		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred						
59		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred						
5A		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred						
5B		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred			Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address
5C		MMC::LBUSPERR						
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>
5D		MMC::TIMERR						
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Not used
5E		MMC::CHK3STS						
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CHK3 error in SMP, LSI
5F		MMC::RSTSTS						
	Not used	Not used	Micro CHK1B occurred	Micro CHK1A occurred	Micro MCNRST2 occurred	Micro MCNRST1 occurred	Micro MPRST occurred	Micro MNTRST occurred

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 68-69/78-7B(DKA CHK1B) (4/5)

	0	1	2	3	4	5	6	7
60	MMC::RSTSTS							
	Not used	Not used	SCAN mode set occurred	CHK1A occurred	WCHK1 occurred	SELRST occurred	SYSRST occurred	Power-on reset occurred
61	MMC::DRAMC1BSTS							
	960→LM access Correctable errors are over the specified time		I960 XR read incorrect address	I960 XR write incorrect address	Not used	Not used	Not used	Not used
	Bank 0	Bank 1						
62	MMC::DRAMC1BSTS							
	LANC→LM access Correctable errors are over the specified time		LANC→LM access Uncorrectable error detected		LANC→XR incorrect address	Not used	Not used	Not used
	Bank 0	Bank 1	Bank 0	Bank 1				
63	MMC::DRAMC1BSTS							
	Not used	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
64	MMC::ERADR							
	Address from L bus							
65	MMC::ERADR							
	Address from L bus							
66	MMC::ERADR							
	Address from L bus							
67	MMC::ERADR							
	Address from L bus						Not used	Not used
68	MMC::ERBYT							
	Not used	Not used	DRAM control signal RAMADR error	DRAM control signal RAS error	DRAM control signal BAS error	DRAM control signal CAS error	DRAM control signal WE error	DRAM control signal DQM error
69	MMC::ERORD							
	Data before correction							
6A	MMC::ERORD							
	Data before correction							
6B	MMC::ERORD							
	Data before correction							
6C	MMC::ERORD							
	Data before correction							
6D	MMC::ERORC							
	Check bit before correction							
6E	MMC::ERORC							
	Check bit before correction							
6F	MPA::ERCRD							
	Data after correction							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 68-69/78-7B (DKA CHK1B) (5/5)

	0	1	2	3	4	5	6	7
70		MPA::ERCRD						
		Data after correction						
71		MPA::ERCRD						
		Data after correction						
72		MPA::ERCRD						
		Data after correction						
73		MPA::ERCRC						
		Check bit after correction						
74		MPA::ERCRC						
		Check bit after correction						
75		MMC::ERRSYD						
		Syndrome before correction						
76		MMC::ERRSYD						
		Syndrome before correction						
77		MMC::ERWA						
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	WR signal value
78		MMC::CECNT						
		Correctable error counter(Low)						
79		MMC::CECNT						
		Correctable error counter(High)						
7A		MMC::RCVINT						
	Not used	Not used	Not used	CLPON signal monitor bit	SCP0 signal monitor bit	SCP1 signal monitor bit	DRR MP0 signal monitor bit	DRR MP1 signal monitor bit
7B		MMC::RCVINT						
	SYSRST signal monitor bit	SELRST signal monitor bit	CHK1A signal monitor bit	CHK1B signal monitor bit	SMP signal monitor bit	LAN/SI0 signal monitor bit	CHA/DRR signal monitor bit	ADP/SCA0 signal monitor bit
7C		MMC::RCVINT						
	Not used	CHK3 signal monitor bit	Not used	SCA1 signal monitor bit	SCA2 signal monitor bit	SCA3 signal monitor bit	SCA4 signal monitor bit	SCA5 signal monitor bit
7D		MMC::RCVINT						
	TIMER0 signal monitor bit	TIMER1 signal monitor bit	TIMER2 signal monitor bit	TIMER3 signal monitor bit	TIMER4 signal monitor bit	TIMER5 signal monitor bit	TIMER6 signal monitor bit	SYNC STOP signal monitor bit
7E		Not used						
		Not used						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : DKA CHK1B) Byte28-31 Detail

(9) MMC CHK1B

	0	1	2	3	4	5	6	7
28		Subcode x'68': MMC CHK1B						
29		MMC::CHK1BSTS						
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A		MMC:: CHK1BSTS						
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B		MMC::MICCHK1STS						
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
2C		MMC::MICCHK1STS						
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2D		MMC::MICCHK1STS						
	LAN hold time-out	Wait time-out	XR decoder error (29A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error
2E		MMC::MPCERRSTS						
	Not used	Not used	WCHK1 at MPCHK	CHK1A at MPCHK	Timeout monitor timer parity error	A/B REG inconsistent check error	A/B REG write time-out	A/B REG access sequence error
2F		MMC::MMCPERR						
	Not used	Not used	Not used	Not used	Data parity err in MMC <00-07>	Data parity err in MMC <10-17>	Data parity err in MMC <20-27>	Data parity err in MMC <30-37>
30		MMC::TIMERR						
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Not used
31		MMC::LBUSPER						
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : DKA CHK1B) Byte28-31 Detail

(10) MMC DRAM CHK1B

	0	1	2	3	4	5	6	7
28	Subcode x'69': MMC DRAM CHK1B							
29	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A	MMC:: CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B	MMC::DRAMC1BSTS							
	i960→LM access Correctable errors are over the specified time		I960 XR read incorrect address	I960 XR write incorrect address	Not used	Not used	Not used	Not used
	Bank 0	Bank 1						
2C	MMC::DRAMC1BSTS							
	LANC→LM access Correctable errors are over the specified time		LANC→LM access Uncorrectable error detected		LANC→XR incorrect address	Not used	Not used	Not used
	Bank 0	Bank 1	Bank 0	Bank 1				
2D	MMC::DRAMC1BSTS							
	Parity error at refresh addr reg	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
2E	MMC::ERADR							
	Address from L bus							
2F	MMC::ERADR							
	Address from L bus							
30	MMC::ERADR							
	Address from L bus							
31	MMC::ERADR							
	Address from L bus						Not used	Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : DKA CHK1B) Byte28-31 Detail

(11) MMC CHK1B

	0	1	2	3	4	5	6	7
28		Subcode x'78': MMC CHK1B						
29		MMC::CHK1BSTS						
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A		MMC:: CHK1BSTS						
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B		MMC::MICCHK1STS						
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
2C		MMC::MICCHK1STS						
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2D		MMC::MICCHK1STS						
	LAN hold time-out	Wait time-out	XR decoder error (29A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error
2E		MMC::MPCERRSTS						
	Not used	Not used	WCHK1 at MPCHK	CHK1A at MPCHK	Timeout monitor timer parity error	A/B REG inconsistent check error	A/B REG write time-out	A/B REG access sequence error
2F		MMC::MMCPERR						
	Not used	Not used	Not used	Not used	Data parity err in MMC <00-07>	Data parity err in MMC <10-17>	Data parity err in MMC <20-27>	Data parity err in MMC <30-37>
30		MMC::TIMERR						
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Not used
31		MMC::LBUSPER						
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : DKA CHK1B) Byte28-31 Detail

(12) MMC DRAM CHK1B

	0	1	2	3	4	5	6	7
28	Subcode x'79': MMC DRAM CHK1B							
29	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A	MMC:: CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B	MMC::DRAMC1BSTS							
	i960→LM access Correctable errors are over the specified time		I960 XR read incorrect address	I960 XR write incorrect address	Not used	Not used	Not used	Not used
	Bank 0	Bank 1						
2C	MMC::DRAMC1BSTS							
	LANC→LM access Correctable errors are over the specified time		LANC→LM access Uncorrectable error detected		LANC→XR incorrect address	Not used	Not used	Not used
	Bank 0	Bank 1	Bank 0	Bank 1				
2D	MMC::DRAMC1BSTS							
	Parity error at refresh addr reg	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
2E	MMC::ERADR							
	Address from L bus							
2F	MMC::ERADR							
	Address from L bus							
30	MMC::ERADR							
	Address from L bus							
31	MMC::ERADR							
	Address from L bus						Not used	Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : DKA CHK1B) Byte28-31 Detail

(13) I960 read data parity error

	0	1	2	3	4	5	6	7
28	Subcode x'7A': I960 read data parity error							
29	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A	MMC:: CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B	MMC::MICCHK1STS							
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2C	MMC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (29A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error
2D	MMC::MPCERRSTS							
	Not used	Not used	WCHK1 at MPCHK	CHK1A at MPCHK	Timeout monitor timer parity error	A/B REG inconsistent check error	A/B REG write time-out	A/B REG access sequence error
2E	MMC::DRAMC1BSTS							
	i960→LM access Correctable errors are over the specified time		I960 XR read incorrect address	I960 XR write incorrect address	Not used	Not used	Not used	Not used
	Bank 0	Bank 1						
2F	MMC::DRAMC1BSTS							
	LANC→LM access Correctable errors are over the specified time		LANC→LM access Uncorrectable error detected		LANC→XR incorrect address	Not used	Not used	Not used
	Bank 0	Bank 1	Bank 0	Bank 1				
30	MMC::DRAMC1BSTS							
	Parity error at refresh addr reg	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
31	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : DKA CHK1B) Byte28-31 Detail

(14) LANC read data parity error

	0	1	2	3	4	5	6	7
28	Subcode x'7B': LANC read data parity error							
29	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A	MMC:: CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B	MMC::MICCHK1STS							
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2C	MMC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (29A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error
2D	MMC::MPCERRSTS							
	Not used	Not used	WCHK1 at MPCHK	CHK1A at MPCHK	Timeout monitor timer parity error	A/B REG inconsistent check error	A/B REG write time-out	A/B REG access sequence error
2E	MMC::DRAMC1BSTS							
	i960→LM access Correctable errors are over the specified time		I960 XR read incorrect address	I960 XR write incorrect address	Not used	Not used	Not used	Not used
	Bank 0	Bank 1						
2F	MMC::DRAMC1BSTS							
	LANC→LM access Correctable errors are over the specified time		LANC→LM access Uncorrectable error detected		LANC→XR incorrect address	Not used	Not used	Not used
	Bank 0	Bank 1	Bank 0	Bank 1				
30	MMC::DRAMC1BSTS							
	Parity error at refresh addr reg	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
31	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 6A (DKA CHK1B) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder addres (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Hardware information (See following pages)							
|								
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Sympton code (x‘FF8E’ : LDEV type = 6587/x‘EF8E’ : LDEV type = 6586)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 6A (DKA CHK1B)(2/5)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT No.							
	’08’							
41	MMC::ERRSTS							
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
43	MMC::CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2 CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
44	MMC::CHK1BADRS							
	Address when CHK1B occurred							
45	MMC::CHK1BADRS							
	Address when CHK1B occurred							
46	MMC::CHK1BADRS							
	Address when CHK1B occurred							
47	MMC::CHK1BADRS							
	Address when CHK1B occurred						WR/RD flag in CHK1B	Command/ Data flag in CHK1B
48	MMC::CHK1BBE							
	Not used	Not used	Not used	Not used	I960BE0 in CHK1B	I960BE1 in CHK1B	I960BE2 in CHK1B	I960BE3 in CHK1B
49	MMC::MICPERSTS							
	Not used	Not used	Not used	Not used	Data parity err in MMC <00-07>	Data parity err in MMC <10-17>	Data parity err in MMC <20-27>	Data parity err in MMC <30-37>
4A	MMC::XRADRPERR							
	Not used	Not used	Not used	XR bus address parity error reset				
				<30-35, BE>	<Byte 0>	<Byte 1>	<Byte 2>	<Byte 3>
4B	MMC::XBUSDTPERR							
	Not used	Not used	Not used	Not used	XR bus data parity error <00-07>	XR bus data parity error <10-17>	XR bus data parity error <20-27>	XR bus data parity error <30-37>
4C	MMC::LAST1IP							
	Last address before CHK1A occured							
4D	MMC::LAST1IP							
	Last address before CHK1A occured							
4E	MMC::LAST1IP							
	Last address before CHK1A occurred							
4F	MMC::LAST1IP							
	Last address before CHK1A occurred				Not used	Not used	Not used	Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 6A(DKA CHK1B) (3/5)

	0	1	2	3	4	5	6	7
50		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
51		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
52		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
53		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred			Not used	Not used	Not used	Not used
54		MMC::LAST1						
		Last execution address before CHK1A occurred						
55		MMC::LAST1						
		Last execution address before CHK1A occurred						
56		MMC::LAST1						
		Last execution address before CHK1A occurred						
57		MMC::LAST1						
		Last execution address before CHK1A occurred			Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address
58		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred						
59		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred						
5A		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred						
5B		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred			Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address
5C		MMC::LBUSPERR						
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>
5D		MMC::TIMERR						
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Not used
5E		MMC::CHK3STS						
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CHK3 error in SMP, LSI
5F		MMC::RSTSTS						
	Not used	Not used	Micro CHK1B occurred	Micro CHK1A occurred	Micro MCNRST2 occurred	Micro MCNRST1 occurred	Micro MPRST occurred	Micro MNTRST occurred

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 6A(DKA CHK1B) (4/5)

	0	1	2	3	4	5	6	7
60	MMC::RSTSTS							
	Not used	Not used	SCAN mode set occurred	CHK1A occurred	WCHK1 occurred	SELRST occurred	SYSRST occurred	Power-on reset occurred
61	MMC::DRAMC1BSTS							
	960→LM access Correctable errors are over the specified time		I960 XR read incorrect address	I960 XR write incorrect address	Not used	Not used	Not used	Not used
	Bank 0	Bank 1						
62	MMC::DRAMC1BSTS							
	LANC→LM access Correctable errors are over the specified time		LANC→LM access Uncorrectable error detected		LANC→XR incorrect address	Not used	Not used	Not used
	Bank 0	Bank 1	Bank 0	Bank 1				
63	MMC::DRAMC1BSTS							
	Not used	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
64	MMC::FERADR							
	Address from L bus (fetch)							
65	MMC::FERADR							
	Address from L bus (fetch)							
66	MMC::FERADR							
	Address from L bus (fetch)							
67	MMC::FERADR							
	Address from L bus (fetch)						Not used	Not used
68	MMC::FERBYT							
	Not used	Not used	DRAM control signal RAMADR error	DRAM control signal RAS error	DRAM control signal BAS error	DRAM control signal CAS error	DRAM control signal WE error	DRAM control signal DQM error
69	MMC::FERORD							
	Data before correction (fetch)							
6A	MMC::FERORD							
	Data before correction (fetch)							
6B	MMC::FERORD							
	Data before correction (fetch)							
6C	MMC::FERORD							
	Data before correction (fetch)							
6D	MMC::FERORC							
	Check bit before correction (fetch)							
6E	MMC::FERORC							
	Check bit before correction (fetch)							
6F	MPA::FERCRD							
	Data after correction (fetch)							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 6A (DKA CHK1B) (5/5)

	0	1	2	3	4	5	6	7
70		MPA::FERCRD						
		Data after correction (fetch)						
71		MPA::FERCRD						
		Data after correction (fetch)						
72		MPA::FERCRD						
		Data after correction (fetch)						
73		MPA::FERCRC						
		Check bit after correction (fetch)						
74		MPA::FERCRC						
		Check bit after correction (fetch)						
75		MMC::FERRSYD						
		Syndrome before correction (fetch)						
76		MMC::FERRSYD						
		Syndrome before correction (fetch)						
77		MMC::ERWA						
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	WR signal value
78		MMC::CECNT						
		Correctable error counter(Low)						
79		MMC::CECNT						
		Correctable error counter(High)						
7A		MMC::RCVINT						
	Not used	Not used	Not used	CLPON signal monitor bit	SCP0 signal monitor bit	SCP1 signal monitor bit	DRR MP0 signal monitor bit	DRR MP1 signal monitor bit
7B		MMC::RCVINT						
	SYSRST signal monitor bit	SELRST signal monitor bit	CHK1A signal monitor bit	CHK1B signal monitor bit	SMP signal monitor bit	LAN/SI0 signal monitor bit	CHA/DRR signal monitor bit	ADP/SCA0 signal monitor bit
7C		MMC::RCVINT						
	Not used	CHK3 signal monitor bit	Not used	SCA1 signal monitor bit	SCA2 signal monitor bit	SCA3 signal monitor bit	SCA4 signal monitor bit	SCA5 signal monitor bit
7D		MMC::RCVINT						
	TIMER0 signal monitor bit	TIMER1 signal monitor bit	TIMER2 signal monitor bit	TIMER3 signal monitor bit	TIMER4 signal monitor bit	TIMER5 signal monitor bit	TIMER6 signal monitor bit	SYNC STOP signal monitor bit
7E		Not used						
7F		Not used						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : DKA CHK1B) Byte28-31 Detail

(15) MMC FETCH CHK1B

	0	1	2	3	4	5	6	7
28	Subcode x'6A': MMC FETCH CHK1B							
29	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A	MMC:: CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B	MMC::DRAMC1BSTS							
	i960→LM access Correctable errors are over the specified time		I960 XR read incorrect address	I960 XR write incorrect address	Not used	Not used	Not used	Not used
	Bank 0	Bank 1						
2C	MMC::DRAMC1BSTS							
	LANC→LM access Correctable errors are over the specified time		LANC→LM access Uncorrectable error detected		LANC→XR incorrect address	Not used	Not used	Not used
	Bank 0	Bank 1	Bank 0	Bank 1				
2D	MMC::DRAMC1BSTS							
	Parity error at refresh addr reg	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
2E	MMC::FERADR							
	Error address in fetch to LM							
2F	MMC::FERADR							
	Error address in fetch to LM							
30	MMC::FERADR							
	Error address in fetch to LM							
31	MMC::FERADR							
	Error address in fetch to LM						Not used	Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 64-65/74-75(DKA CHK1B) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder addres (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Hardware information (See following pages)							
|								
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Sympton code (x‘FF8E’ : LDEV type = 6587/x‘EF8E’ : LDEV type = 6586)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 64-65/74-75(DKA CHK1B) (2/5)

	0	1	2	3	4	5	6	7
40		FREE AREA FORMAT No.						
		'09'						
41		MMC::ERRSTS						
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42		MMC::CHK1BSTS						
	Not used	Not used	Not used	Not used	Not used	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
43		MMC::CHK1BSTS						
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2 CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
44		MMC::CHK1BADRS						
		Address when CHK1B occurred						
45		MMC::CHK1BADRS						
		Address when CHK1B occurred						
46		MMC::CHK1BADRS						
		Address when CHK1B occurred						
47		MMC::CHK1BADRS						
		Address when CHK1B occurred					WR/RD flag in CHK1B	Command/ Data flag in CHK1B
48		MMC::CHK1BBE						
	Not used	Not used	Not used	Not used	I960BE0 in CHK1B	I960BE1 in CHK1B	I960BE2 in CHK1B	I960BE3 in CHK1B
49		MMC::MICPERSTS						
	Not used	Not used	Not used	Not used	Data parity err in MMC <00-07>	Data parity err in MMC <10-17>	Data parity err in MMC <20-27>	Data parity err in MMC <30-37>
4A		MMC::XRADRPERR						
	Not used	Not used	Not used	XR bus address parity error reset				
				<30-35, BE>	<Byte 0>	<Byte 1>	<Byte 2>	<Byte 3>
4B		MMC::XBUSDTPERR						
	Not used	Not used	Not used	Not used	XR bus data parity error <00-07>	XR bus data parity error <10-17>	XR bus data parity error <20-27>	XR bus data parity error <30-37>
4C		MMC::LAST1IP						
		Last address before CHK1A occured						
4D		MMC::LAST1IP						
		Last address before CHK1A occured						
4E		MMC::LAST1IP						
		Last address before CHK1A occurred						
4F		MMC::LAST1IP						
		Last address before CHK1A occurred			Not used	Not used	Not used	Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 64-65/74-75(DKA CHK1B) (3/5)

	0	1	2	3	4	5	6	7
50		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
51		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
52		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred						
53		MMC::LAST2IP						
		Address one generation older than the last one before CHK1A occurred			Not used	Not used	Not used	Not used
54		MMC::LAST1						
		Last execution address before CHK1A occurred						
55		MMC::LAST1						
		Last execution address before CHK1A occurred						
56		MMC::LAST1						
		Last execution address before CHK1A occurred						
57		MMC::LAST1						
		Last execution address before CHK1A occurred			Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address
58		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred						
59		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred						
5A		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred						
5B		MMC::LAST2						
		Execution address one generation older than the last one before CHK1A occurred			Not used	Not used	CHK1A occurred in LAN OP	Fetch attribute of last exec address
5C		MMC::LBUSPERR						
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>
5D		MMC::TIMERR						
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Not used
5E		MMC::CHK3STS						
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CHK3 error in SMP, LSI
5F		MMC::RSTSTS						
	Not used	Not used	Micro CHK1B occurred	Micro CHK1A occurred	Micro MCNRST2 occurred	Micro MCNRST1 occurred	Micro MPRST occurred	Micro MNTRST occurred

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 64-65/74-75(DKA CHK1B) (4/5)

	0	1	2	3	4	5	6	7
60	MMC::RSTSTS							
	Not used	Not used	SCAN mode set occurred	CHK1A occurred	WCHK1 occurred	SELRST occurred	SYSRST occurred	Power-on reset occurred
61	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
62	MPA::XWER							
	Access to not use address	Access to not use address	Access to not use address	Not used	Not used	Not used	Not used	XR byte access error
63	MPA::XWER							
	XR write address parity error				XR write data parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
64	MPA::XRER							
	Not used	Not used	Not used	Not used	XR read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3
65	MPA::CNT00/01ER							
	CNT#00 parity error				CNT#01 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
66	MPA::CNT02/03ER							
	CNT#02 parity error				CNT#03 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
67	MPA::CNT04/05ER							
	CNT#04 parity error				CNT#05 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
68	MPA::CNT06/07ER							
	CNT#06 parity error				CNT#07 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
69	MPA::CNT08/09ER							
	CNT#08 parity error				CNT#09 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
6A	MPA::CNT10/11ER							
	CNT#10 parity error				CNT#11 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
6B	MPA::CNT12/13ER							
	CNT#12 parity error				CNT#13 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
6C	MPA::CNT14ER							
	CNT#14 parity error				Not used	Not used	Not used	Not used
	Byte 0	Byte 1	Byte 2	Byte 3				
6D	MPA::CWER							
	Not used	Not used	Not used	Not used	Not used	Access to not use register	Access to not use register	Access to not use register
6E	MPA:: CWER							
	COM_IF write address parity error				COM_IF write data parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
6F	MPA::CRER							
	Not used	Not used	Not used	Not used	COM_IF read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = 64-65/74-75(DKA CHK1B) (5/5)

	0	1	2	3	4	5	6	7
70	MPA::MPID							
	PKID#				Not used	Not used	MPID#	
71	MPA::REV							
72	Not used							
73	Not used							
74	FCA::FCHK10							
	XR read data parity error				33MHz clock error	25MHz clock error	SEQ10 error	SEQ19 error
	Byte0	Byte1	Byte2	Byte3				
75	FCA::FCHK10							
	TLM read data parity error	PCI S error	PCI P error	Diagnose CHK1 occurred	PCI Devsel timeout	PCI TLM read address counter parity error	PCI target abort	PCI target ready
76	FCA::FCHK10							
	XR address parity error				XR write data parity error			
	Byte0	Byte1	Byte2	Byte3	Byte0	Byte1	Byte2	Byte3
77	FCA::FCHK10							
	TLM address counter parity error	ELM write address counter parity error	Not used	Not used	Not used	Not used	Not used	Not used
78	QDTA::ESTA9							
	Write to unused register	Write to read-only register	Set A at CMD-A execute	Set B at CMD-B execute	Set C at 64CMD execute	Address2 parity error	Address3 parity error	Byte access error
79	QDTA::ESTA9							
	Input DT0 parity error	Input DT0 parity error	Address DEC parity error	Output DT0 parity error	Output DT1 parity error	DRR4 clock phase error	CHSN4 clock phase error	CHSN6 clock phase error
7A	QDTA::DRSTS							
	Transfer end (A/64CMD)	Not used	(A/64CMD) Exec wait/ Executing	(A/64CMD) Data transferring	Transfer END B	Not used	Command B Exec wait/ Executing	Command B Data transferring
7B	QDTA::DRSTS							
	CHK2 occurred	CHK2 occurred at transferring data	CHK2 in DRR controller	CHK1B in CACHE /CARB	Arbiter/ timer error	CHK1B occurred	Forced data transferring end	Force error occurred
7C	QDTA::P0EST0							
	RX SEQ ERR	PRB RD-PNT P-ERR	RD DT-CNT P-ERR	RD DEF FLG-PNT P-ERR	RD DEF SEQ ERR	RD DEF-CNT P-ERR	WT DEF FLG-PNT P-ERR	WT DT-CNT R
7D	QDTA::P0EST0							
	WT DEF SEQ ERR	WT DEF-CNT P-ERR	PBF WAD-CNT P-ERR	PBF RAD-CNT P-ERR	Not used	Not used	Not used	‡ Not used
7E	QDTA::P1EST1							
	RX SEQ ERR	PRB RD-PNT P-ERR	RD DT-CNT P-ERR	RD DEF FLG-PNT P-ERR	RD DEF SEQ ERR	RD DEF-CNT P-ERR	WT DEF FLG-PNT P-ERR	WT DT-CNT R
7F	QDTA::P1EST1							
	WT DEF SEQ ERR	WT DEF-CNT P-ERR	PBF WAD-CNT P-ERR	PBF RAD-CNT P-ERR	Not used	Not used	Not used	‡ Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : DKA CHK1B) Byte28-31 Detail

(16) FCA CHK1B

	0	1	2	3	4	5	6	7
28	Subcode x'64': FCA CHK1B							
29	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHK1B in CHA/QDTA	CHK1B in MPA	CHK1B in MMC
2A	MMC::CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2 CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B	FCA::FCHK10							
	XR read data parity error				33MHz clock error	25MHz clock error	SEQ10 error	SEQ19 error
	Byte0	Byte1	Byte2	Byte3				
2C	FCA::FCHK10							
	TLM read data parity error	PCI S error	PCI P error	Diagnose CHK1 occurred	PCI Devsel timeout	PCI TLM read address counter parity error	PCI target abort	PCI target ready
2D	FCA::FCHK10							
	XR address parity error				XR write data parity error			
	Byte0	Byte1	Byte2	Byte3	Byte0	Byte1	Byte2	Byte3
2E	FCA::FCHK10							
	TLM address counter parity error	ELM write address counter parity error	Not used	Not used	Not used	Not used	Not used	Not used
2F	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
30	MMC::MICCHK1STS							
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
31	MMC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : DKA CHK1B) Byte28-31 Detail

(17) QDTA CHK1B

	0	1	2	3	4	5	6	7
28		Subcode x'63': QDTA CHK1B						
29		MMC::CHK1BSTS						
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A		MMC::CHK1BSTS						
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B		QDTA::DRSTS						
	Transfer end (A/64CMD)	Not used	(A/64CMD) Exec wait/ Executing	(A/64CMD) Data transferring	Transfer END B	Not used	Command B Exec wait/ Executing	Command B Data transferring
2C		QDTA::DRSTS						
	CHK2 occurred	CHK2 occurred at transferring data	CHK2 in DRR controller	CHK1B in CACHE /CARB	Arbiter/ timer error	CHK1B occurred	Forced data transferring end	Force error occurred
2D		QDTA::ERR						
	DRR control error	P0 control error	P1 control error	DRR DT error	P0 DT error	P1 DT error	P0 CARB/ CMA error	P1 CARB/ CMA error
2E		QDTA::ERR						
	P0 error occurred	P1 error occurred	DT error occurred	Time over error occurred	ST0 Valid	ST1 Valid	P0 use flag (Not error)	P1 use flag (Not error)
2F		Not used						
30		QDTA::ESTA9						
	Write to unused register	Write to read-only register	Set A at CMD-A execute	Set B at CMD-B execute	Set C at 64CMD execute	Address2 parity error	Address3 parity error	Byte access error
31		QDTA::ESTA9						
	Input DT0 parity error	Input DT0 parity error	Address DEC parity error	Output DT0 parity error	Output DT1 parity error	DRR4 clock phase error	CHSN4 clock phase error	CHSN6 clock phase error

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : DKA CHK1B) Byte28-31 Detail

(18) FCA CHK1B

	0	1	2	3	4	5	6	7
28	Subcode x'74': FCA CHK1B							
29	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHK1B in CHA/QDTA	CHK1B in MPA	CHK1B in MMC
2A	MMC::CHK1BSTS							
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2 CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B	FCA::FCHK10							
	XR read data parity error				33MHz clock error	25MHz clock error	SEQ10 error	SEQ19 error
	Byte0	Byte1	Byte2	Byte3				
2C	FCA::FCHK10							
	TLM read data parity error	PCI S error	PCI P error	Diagnose CHK1 occurred	PCI Devsel timeout	PCI TLM read address counter parity error	PCI target abort	PCI target ready
2D	FCA::FCHK10							
	XR address parity error				XR write data parity error			
	Byte0	Byte1	Byte2	Byte3	Byte0	Byte1	Byte2	Byte3
2E	FCA::FCHK10							
	TLM address counter parity error	ELM write address counter parity error	Not used	Not used	Not used	Not used	Not used	Not used
2F	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
30	MMC::MICCHK1STS							
	XR decoder error (90)	XR decoder error (91)	MPCHK counter parity error	Parity error in MIC internal bus	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
31	MMC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Processor failure : DKA CHK1B) Byte28-31 Detail

(19) QDTA CHK1B

	0	1	2	3	4	5	6	7
28		Subcode x'73': QDTA CHK1B						
29		MMC::CHK1BSTS						
	Not used	Not used	Not used	Not used	CHK1B in SRAM controller	CHK1B in CHA/QDTA	CHK1B in SMP	CHK1B in MIC
2A		MMC::CHK1BSTS						
	XR0(SCA#0 FCA/ADP) CHK1B	XR1(SCA#1) CHK1B	XR2CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	CHK1B in DRAM controller
2B		QDTA::DRSTS						
	Transfer end (A/64CMD)	Not used	(A/64CMD) Exec wait/ Executing	(A/64CMD) Data transferring	Transfer END B	Not used	Command B Exec wait/ Executing	Command B Data transferring
2C		QDTA::DRSTS						
	CHK2 occurred	CHK2 occurred at transferring data	CHK2 in DRR controller	CHK1B in CACHE /CARB	Arbiter/ timer error	CHK1B occurred	Forced data transferring end	Force error occurred
2D		QDTA::ERR						
	DRR control error	P0 control error	P1 control error	DRR DT error	P0 DT error	P1 DT error	P0 CARB/ CMA error	P1 CARB/ CMA error
2E		QDTA::ERR						
	P0 error occurred	P1 error occurred	DT error occurred	Time over error occurred	ST0 Valid	ST1 Valid	P0 use flag (Not error)	P1 use flag (Not error)
2F		Not used						
30		QDTA::ESTA9						
	Write to unused register	Write to read-only register	Set A at CMD-A execute	Set B at CMD-B execute	Set C at 64CMD execute	Address2 parity error	Address3 parity error	Byte access error
31		QDTA::ESTA9						
	Input DT0 parity error	Input DT0 parity error	Address DEC parity error	Output DT0 parity error	Output DT1 parity error	DRR4 clock phase error	CHSN4 clock phase error	CHSN6 clock phase error

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = F0 (Microprogram detected WCHK1) (1/1)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode (x‘F0’)							
29	Hardware information (See following pages)							
31								
32	Module ID (See following pages)							
33	Routine ID (See following pages)							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Sympton code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)							
37	(This information is not fixed until DKC reports SSB to HOST.)							
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							
40	Free area							
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Micro WCHK1) Byte28-31 Detail

(1) Byte28 = F0 : Micro WCHK1 (Note 1)

	0	1	2	3	4	5	6	7
28	Subcode : x‘F0’ : Micro WCHK1							
29	Not used							
2A	Failure section information							
2B								
2C	Bus mode information							
2D	Shared memory data informatin							
2E								
2F								
30	CHK3 status information							
31	Master error information							
32	Module ID (Note 2)							
33	Routine ID (Note 2)							

(Note 1) This format is soecfied by byte 32 and 33.

(Note 2) Module ID : x‘32’ : Error procedure aid
Routine ID : x‘51’ : CHK3 in initializing
x‘52’ : CHK3 in scanning
x‘53’ : Unknown CHK3
x‘54’ : CHK3 threshold exceeded
x‘55’ : CHK3 in main recovery process
x‘56’ : CHK3 in slave proces
x‘57’ : Other function failed in CHK3 process
x‘58’ : Reconstruction failed in CHK3 process
x‘59’ : Making SSB failed in CHK3 interruption process
x‘5A’ : Making CHK3 SIM failed
x‘5B’ : Making SSB failed in CHK3 error process
x‘5C’ : System down in CHK3 process
x‘5D’ : MP down because reset CHK3 impossibly

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Micro WCHK1) Byte28-31 Detail

(2) Byte28 = F0 : Micro WCHK1 (Note 1)

	0	1	2	3	4	5	6	7
28	Subcode : x‘F0’ : Micro WCHK1							
29	Not used							
2A	Not used							
2B	Not used							
2C	Not used							
2D	Not used							
2E	Not used							
2F	Not used							
30	Not used							
31	Not used							
32	Module ID (Note 2)							
33	Routine ID (Note 2)							

(Note 1) This format is soecfied by byte 32 and 33.

(Note 2) Module ID : x‘32’ : Error procedure aid
Routine ID : x‘81’ : Unknown CHA CHK3
x‘82’ : Unknown DKA CHK3
x‘F1’ : CHK1A threshold exdeeded
x‘F4’ : CHK1B threshold exceeded
x‘F7’ :None MP
x‘F8’ :No logical error information when pseudo-WCHK1 detected
x‘FB’ : CHK1A detected (execte REBOOT)

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Micro WCHK1) Byte28-31 Detail

(3) Byte28 = F0 : Micro WCHK1 (Note 1)

	0	1	2	3	4	5	6	7
28	Subcode : x‘F0’ : Micro WCHK1							
29	Not used							
2A	Return value of arbiter process							
2B								
2C								
2D								
2E								
2F	Not used							
30	Not used							
31	Not used							
32	Module ID (Note 2)							
33	Routine ID (Note 2)							

(Note 1) This format is soecfied by byte 32 and 33.

(Note 2) Module ID : x‘32’ : Error procedure aid
Routine ID : x‘C1’ : Arbiter process failed in cluster failure

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Micro WCHK1) Byte28-31 Detail

(4) Byte28 = F0 : Micro WCHK1 (Note 1)

	0	1	2	3	4	5	6	7
28	Subcode : x‘F0’ : Micro WCHK1							
29	Not used							
2A	Access test bit map (initial value)							
2B								
2C								
2D								
2E	Access test bit map for succeeded section							
2F								
30								
31								
32	Module ID (Note 2)							
33	Routine ID (Note 2)							

(Note 1) This format is soecfied by byte 32 and 33.

(Note 2) Module ID : x‘32’ : Error procedure aid
Routine ID : x‘C2’ : No last path in cluster failure

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Micro WCHK1) Byte28-31 Detail

(5) Byte28 = F0 : Micro WCHK1 (Note 1)

	0	1	2	3	4	5	6	7
28	Subcode : x‘F0’ : Micro WCHK1							
29	Not used							
2A	Interruption information							
2B								
2C								
2D								
2E	CHK1B status information							
2F								
30								
31	Master error information							
32	Module ID (Note 2)							
33	Routine ID (Note 2)							

(Note 1) This format is soecfied by byte 32 and 33.

(Note 2) Module ID : x‘32’ : Error procedure aid
Routine ID : x‘F5’ : CHK1B in CHK3
x‘F6’ : No error CHK3
x‘F9’ : Reser CHK3 impossibly

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Micro WCHK1) Byte28-31 Detail

(6) Byte28 = F0 : Micro WCHK1 (Note 1)

	0	1	2	3	4	5	6	7
28	Subcode : x‘F0’ : Micro WCHK1							
29	Not used							
2A	INITYPER (x‘49 4E 49 54 59 45 52’)							
2B								
2C								
2D								
2E								
2F								
30								
31								
32	Module ID (Note 2)							
33	Routine ID (Note 2)							

(Note 1) This format is soecfied by byte 32 and 33.

(Note 2) Module ID : x‘80’ : CHA/DKA kernael
Routine ID : x‘00’ : Invalid reset cause

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Micro WCHK1) Byte28-31 Detail

(7) Byte28 = F0 : Micro WCHK1 (Note 1)

	0	1	2	3	4	5	6	7
28	Subcode : x‘F0’ : Micro WCHK1							
29	Not used							
2A	WCHK1 type code							
2B	Reserved							
2C	Initialize interface information							
2D								
2E	Reset type code							
2F								
30	1st reset type code							
31	Reset SSB type code							
32	Module ID (Note 2)							
33	Routine ID (Note 2)							

(Note 1) This format is soecfied by byte 32 and 33.

(Note 2) Module ID : x‘16’ : Reset
Routine ID : x‘27’ : CHK1B in initializing
Routine ID : x‘28’ : Force Reset in initializing
Routine ID : x‘29’ : Initernal Reset in initializing
Routine ID : x‘2f’ : CHK3 in initializing
Routine ID : x‘32’ : Logical Inconsistency Reset in initializing
Routine ID : x‘33’ : Live Ins in initializing
Routine ID : x‘34’ : Power Failure Reset in initializing
Routine ID : x‘37’ : Fault Reset in initializing
Routine ID : x‘60’ : Internal Reset Loop in Resetting
Routine ID : x‘61’ : Logical Inconsistency Reset Loop in Resetting
Routine ID : x‘62’ : CHK1B Loop in Resetting
Routine ID : x‘63’ : CHK3 Loop in Resetting
Routine ID : x‘64’ : CHK1B unrecoverable
Routine ID : x‘65’ : Fault Reset Loop in Resetting
Routine ID : x‘66’ : CHK2A Reset
Routine ID : x‘8e’ : Force WCHK1 (by another MP)

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Micro WCHK1) Byte28-31 Detail

(8) Byte32 33 = x‘B4D0’ : TPC : FOP force WCHK1

	0	1	2	3	4	5	6	7
28	Subcode : x‘F0’ : Micro WCHK1							
29	Not used							
2A	Not used							
2B	Not used							
2C	Not used							
2D	Not used							
2E	Not used							
2F	Not used							
30	Not used							
31	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Micro WCHK1) Byte28-31 Detail

(9) Byte32 33 = x‘B4D1’ : TPC : FOP force WCHK1

	0	1	2	3	4	5	6	7
28	Subcode : x‘F0’ : Micro WCHK1							
29	Not used							
2A	Not used							
2B	Not used							
2C	FOP Detected error code							
2D								
2E	Not used							
2F	Not used							
30	Not used							
31	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 = X0 & Byte28 = F1 (Microprogram CHK1A) (1/1)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode (x‘F0’)							
29	Hardware information (See following pages)							
31								
32	Module ID (See following pages)							
33	Routine ID (See following pages)							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Sympton code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)							
37	(This information is not fixed until DKC reports SSB to HOST.)							
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							
40	Free area							
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E (Microprogram CHK1A) Byte28-31 Detail

(1) Byte32·33 = x‘165X’ : Microprogram simulated CHK1A for error recovery by REBOOT.

	0	1	2	3	4	5	6	7
28	Subcode : x‘F1’ : Microprogram CHK1A							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK:: ERADR							
	Address (1) from L bus							
2B	RCHK:: ERADR							
	Address (2) from L bus							
2C	RCHK:: ERADR							
	Address (3) from L bus						Not used	Not used
2D	RCHK::LMADRLMT							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Upper limit address of LM
2E	RCHK::LMADRLMT							
	Upper limit address of LM mounting area (lower order)				Not used	Not used	Not used	Not used
2F	RCHK::ERSTS0							
	Inconsist in i960 wrote operation	Not used	MIC READYI timeout	CHK1A cause detected	CHK1B cause detected	Scan→ LM/XR access error	Not used	Not used
30	RCHK::SCANER							
	Scan→Uncorrectable error in LM		Not used	Scan→out of LM area	Scan→ Invalid read XR address	Scan→ Invalid write XR address	Not used	Not used
	Bank0	Bank1						
31	RCHK::CHK1ASTS							
	i960→Uncorrectable error in LM		I960→WR protected LM area	i960→Out of mount LM area	Not used	Not used	LANC→WR protected LM area	LANC→Out of mount LM area
	Bank0	Bank1						

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 : bit4-7 = 1 (Selective Reset) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘8’)				Message (x‘E’)			
28	Not used (‘00’)							
29	DCN status							
	Force device busy	Channel connect request	Command chain execute	Path reserve	Stack status	Sense pending	Long Busy (Command process)	Processor connect
2A	DCN status							
	Single path mode	Gurant path mode	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	Garant path MP
2B	DCN flag							
	RST NTF/ RST ALG SSB PND	Pin Data pending	(RSV)	(RSV)	ODE pending	RSQ pending	SCI/SCE pending	PCH pending
2C	LCT initiation cause							
	0:Ready 1:Not ready	0:Disable 1:Enable	0:No SNS 1:64SNS pending	0:Mount 1:Not mount	0:No RST ALG LPN 1:Exist	0:No SYS RST LPN 1:Exist	0:No stack 1:Exist	0:No wait SNS 1:Exist
2D	LCT initiation cause							
	0:No wait-RI 1:Exist	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	0:Others 1:DEV BSY JOB

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 : bit4-7 = 1 (Selective Reset) (2/3)

	0	1	2	3	4	5	6	7
2E	Command interface flag							
	Pending exist	SCE(RSP)	(RSV)	(RSV)	ODE pending	RSQ pending	SCI pending	PCH pending
2F	Command code							
30	Internal SSB log number							
31								
32	Related reset detailed log number							
33								
34	PCB number				Message code (x‘1’)			
35	SSID (low) of self subsystem							
36	Sympton code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)*							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							
40	Not used							
41	Not used							
42	Initialize interface information							
43								
44	Reset type code							
45								
46	1st reset type code							
47	Reset SSB type code							
48	Reset type code for making SSB							
49	Self CHK1A diference code							
4A	Multi reset type code							
4B								
4C	Interrupted address							
4D								
4E								
4F								
50	Interrupted opration code							
51								
52								
53								
54	Current LDEV number							
55								
56	Current LPN number							
57								
58	Initiation cause code							
59								
5A	Command interface							
5B	DSB (from LCT)							
5C	sys status							
5D	REQ ID (from LCT)							
5E	JCB ID (from LCT)							
5F								
60	wchklmpbitmap (from LCT)							
61								
62								
63								

* : This information is not fixed until DKC reports SSB to HOST.

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 : bit4-7 = 1 (Selective Reset) (3/3)

	0	1	2	3	4	5	6	7
64		jcb id						
65								
66		req id						
67		Job type code						
68		job status						
69		Executing processor number						
6A		Initiation cause code						
6B		Initiation detail code						
6C		Command code						
6D		Channel sequence						
6E		Reserved						
6F								
70		DCN (wldcn1l)						
71								
72								
73								
74		DCN (wldcn2l)						
75								
76								
77								
78		Not used						
79								
7A								
7B								
7C		SLV-DCN (slvdcnr)						
7D								
7E								
7F								

Copyright ©2000, Hitachi, Ltd.

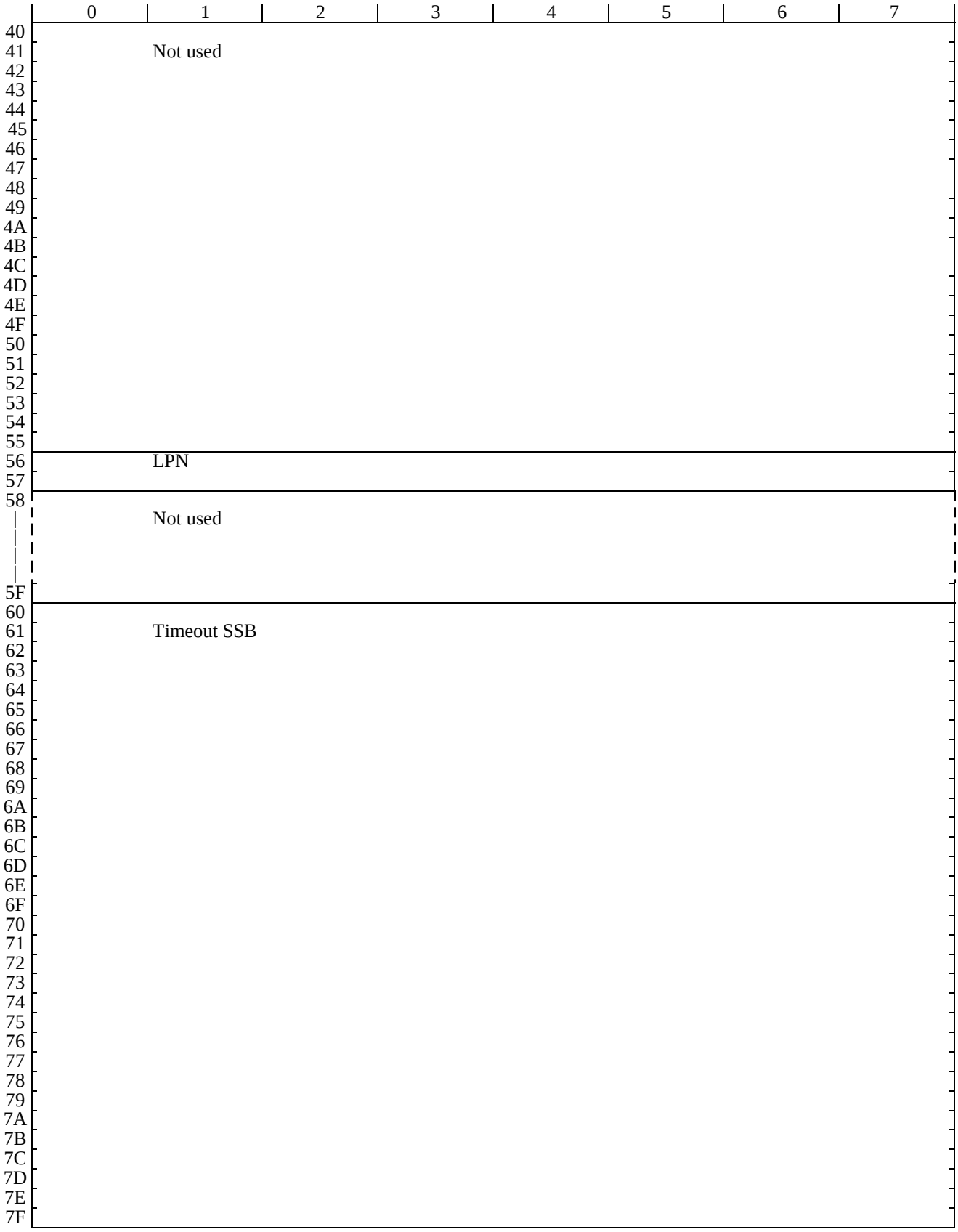
Byte27 = 8E & Byte34 : bit4-7 = 3 (wait SENSE Timeout) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘8’)				Message (x‘E’)			
28	Not used (‘00’)							
29	Not used (‘00’)							
2A	24-byte format	Basic SSB			32-byte format	Basic SSB		
2B								
2C						Exception code		
2D		F/M						
2E		System error code				System error code		
2F								
30	Reset internal SSB number							
31								
32	Detail log number for RESET							
33								
34	PCB number				Message code (x‘3’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)*							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not usde (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 : bit4-7 = 3 (Wait SENSE Timeout) (2/2)



Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 : bit4-7 = 5 (CHK1B Reset) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘8’)				Message (x‘E’)			
28	Related internal SSB log number							
29								
2A	Not used							
2B	Not used							
2C	Old PSW							
2D								
2E								
2F								
30	Internal SSB log number (RESET)							
31								
32	Related RESET detail log number							
33								
34	PCB number				Message code (x‘5’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)*							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not usde (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 : bit4-7 = 5 (CHK1B Reset) (2/2)

	0	1	2	3	4	5	6	7
40		Not used						
41		Not used						
42		Initialize interface information						
43								
44		Reset type code						
45								
46		1st reset type code						
47		Reset SSB type code						
48		Reset type code for making SSB						
49		Self CHK1A difference code						
4A		Multi reset type code						
4B								
4C		Interrupted address						
4D								
4E								
4F								
50		Interrupted opration code						
51								
52								
53								
54		Current LDEV number						
55								
56		Current LPN number						
57								
58		Initiation cause code						
59								
5A		Command interface						
5B		DSB (from LCT)						
5C		sys status						
5D		REQ ID (from LCT)						
5E		JCB ID (form LCT)						
5F								
60		wchklmpbitmap (from LCT)						
61								
62								
63								
64		jcb id						
65								
66		req id						
67		Job type code						
68		job status						
69		Executing processor number						
6A		Initiation cause code						
6B		Initiation detail code						
6C		Command code						
6D		Channel sequence						
6E		Reserved						
6F								
70		DCN						
77								
78		Not used						
79								
7A								
7B								
7C		SLV-DCN (slvdcnr)						
7D								
7E								
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 : bit4-7 = 6 (DKC Internal Reset) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘8’)				Message (x‘E’)			
28	Not used							
29								
2A								
2B								
2C	Old PSW							
2D								
2E								
2F								
30	Internal SSB log number							
31								
32	Reset detail log number							
33								
34	PCB number				Message code (x‘6’)			
35	SSID (Low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)*							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not usde (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 : bit4-7 = 6 (DKC Internal Reset) (2/2)

	0	1	2	3	4	5	6	7
40		Not used						
41		Not used						
42		Initialize interface information						
43								
44		Reset type code						
45								
46		1st reset type code						
47		Reset SSB type code						
48		Reset type code for making SSB						
49		Self CHK1A difference code						
4A		Multi reset type code						
4B								
4C		Interrupted address						
4D								
4E								
4F								
50		Interrupted opration code						
51								
52								
53								
54		Current LDEV number						
55								
56		Current LPN						
57								
58		Initiation cause code						
59								
5A		Command interface						
5B		DSB (from LCT)						
5C		sys status						
5D		REQ ID (from LCT)						
5E		JCB ID (form LCT)						
5F								
60		wchklmpbitmap (from LCT)						
61								
62								
63								
64		jcb id						
65								
66		req id						
67		Job type code						
68		job status						
69		Executing processor number						
6A		Initiation cause code						
6B		Initiation detail code						
6C		Command code						
6D		Channel sequence						
6E		Reserved						
6F								
70		DCN						
77								
78		Not used						
79								
7A								
7B								
7C		SLV-DCN (slvdcnr)						
7D								
7E								
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 : bit4-7 = 7 (LCP Internal Reset) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘8’)				Message (x‘E’)			
28	Not used							
29	Not used							
2A	Internal Sel ective Reset cause							
2B								
2C	For Hotline	Old PSW			For INT SEL RST	LCP error code		
2D								
2E						x‘00’		
2F						x‘00’		
30	Internal SSB log number							
31								
32	Reset detail log number							
33								
34	PCB number				Message code (x‘7’)			
35	SSID (Low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)*							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not usde (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 : bit4-7 = 7 (LCP Internal Reset) (2/2)

	0	1	2	3	4	5	6	7
40		Not used						
41		Not used						
42		Initialize interface information						
43								
44		Reset type code						
45								
46		1st reset type code						
47		Reset SSB type code						
48		Reset type code for making SSB						
49		Self CHK1A difference code						
4A		Multi reset type code						
4B								
4C		Interrupted address						
4D								
4E								
4F								
50		Interrupted opration code						
51								
52								
53								
54		Current LDEV number						
55								
56		Current LPN						
57								
58		Initiation cause code						
59								
5A		Command interface						
5B		DSB (from LCT)						
5C		sys status						
5D		REQ ID (from LCT)						
5E		JCB ID (form LCT)						
5F								
60		wchklmpbitmap (from LCT)						
61								
62								
63								
64		jcb id						
65								
66		req id						
67		Job type code						
68		job status						
69		Executing processor number						
6A		Initiation cause code						
6B		Initiation detail code						
6C		Command code						
6D		Channel sequence						
6E		Reserved						
6F								
70		DCN						
77								
78		Not used						
79								
7A								
7B								
7C		SLV-DCN (slvdcnr)						
7D								
7E								
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 : bit4-7 = 8 (Force Reset) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘8’)				Message (x‘E’)			
28	Not used							
29	Not used							
2A	Not used							
2B	Not used							
2C	Old PSW							
2D								
2E								
2F								
30	Internal SSB log number (RESET)							
31								
32	Reset detail log number							
33								
34	PCB number				Message code (x‘8’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)*							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not usde (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 : bit4-7 = 8 (Foece Reset) (2/2)

	0	1	2	3	4	5	6	7
40		Not used						
41		Not used						
42		Initialize interface information						
43								
44		Reset type code						
45								
46		1st reset type code						
47		Reset SSB type code						
48		Reset type code for making SSB						
49		Self CHK1A difference code						
4A		Multi reset type code						
4B								
4C		Interrupted address						
4D								
4E								
4F								
50		Interrupted opration code						
51								
52								
53								
54		Current LDEV number						
55								
56		Current LPN						
57								
58		Initiation cause code						
59								
5A		Command interface						
5B		DSB (from LCT)						
5C		sys status						
5D		REQ ID (from LCT)						
5E		JCB ID (form LCT)						
5F								
60		wchklmpbitmap (from LCT)						
61								
62								
63								
64		jcb id						
65								
66		req id						
67		Job type code						
68		job status						
69		Executing processor number						
6A		Initiation cause code						
6B		Initiation detail code						
6C		Command code						
6D		Channel sequence						
6E		Reserved						
6F								
70		DCN						
77								
78		Not used						
79								
7A								
7B								
7C		SLV-DCN (slvdcnr)						
7D								
7E								
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 : bit4-7 = 9 (Logical Inconsistency Reset) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘8’)				Message (x‘E’)			
28	Not used							
29								
2A								
2B								
2C	OLD PSW (Interruption source address)							
2D								
2E								
2F								
30	Internal SSB log number							
31								
32	Reset detail log number							
33								
34	PCB number				Message code (x‘9’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)*							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not usde (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8E & Byte34 : bit4-7 = 9 (Logical Inconsistency Reset) (2/2)

	0	1	2	3	4	5	6	7
40		Not used						
41		Not used						
42		Initialize interface information						
43								
44		Reset type code						
45								
46		1st reset type code						
47		Reset SSB type code						
48		Reset type code for making SSB						
49		Self CHK1A difference code						
4A		Multi reset type code						
4B								
4C		Interrupted address						
4D								
4E								
4F								
50		Interrupted opration code						
51								
52								
53								
54		Current LDEV number						
55								
56		Current LPN						
57								
58		Initiation cause code						
59								
5A		Command interface						
5B		DSB (from LCT)						
5C		sys status						
5D		REQ ID (from LCT)						
5E		JCB ID (form LCT)						
5F								
60		wchklmpbitmap (from LCT)						
61								
62								
63								
64		jcb id						
65								
66		req id						
67		Job type code						
68		job status						
69		Executing processor number						
6A		Initiation cause code						
6B		Initiation detail code						
6C		Command code						
6D		Channel sequence						
6E		Reserved						
6F								
70		DCN						
77								
78		Fault reason code						
79								
7A								
7B								
7C		SLV-DCN (slvdcnr)						
7D								
7E								
7F								

Copyright ©2000, Hitachi, Ltd.

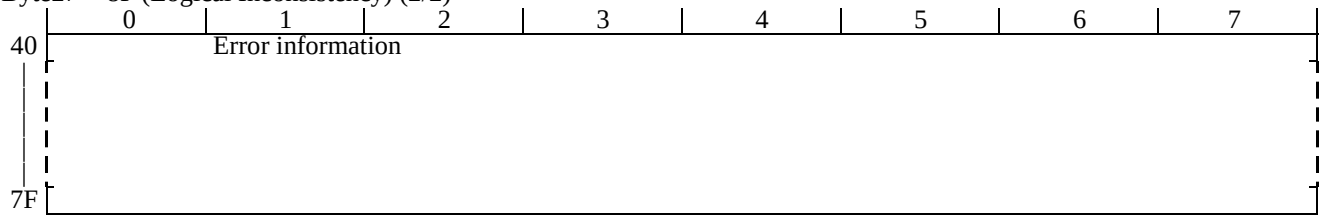
Byte27 = 8F (Logical Inconsistency) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘8’)				Message (x‘F’)			
28	Module ID							
29	Routine ID							
2A	Error information							
2B								
2C								
2D								
2E								
2F								
30								
31								
32								
33								
34	PCB number				Not used (x‘00’)			
35	SSID(low) of self subsystem							
36	Symptom code (x‘FF8F’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)*							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not usde (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Copyright ©2000, Hitachi, Ltd.

Byte27 = 8F (Logical Inconsistency) (2/2)



Copyright ©2000, Hitachi, Ltd.

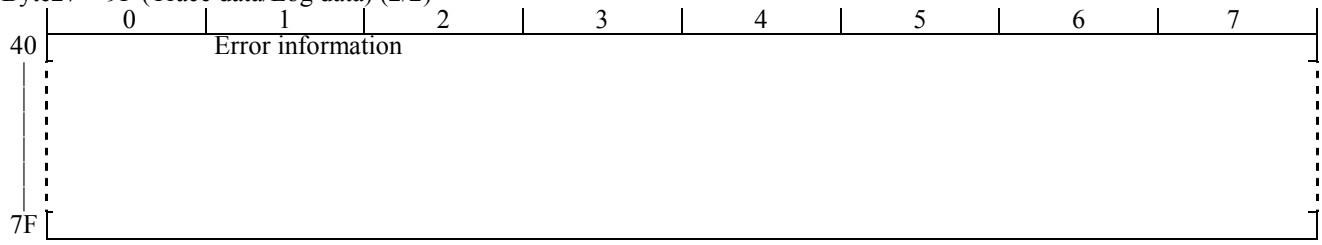
Byte27 = 9F (Trace data/Log data) (1/2)

All of F/M = 9F SSB informations are no problem on DKC performance.

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘9’)				Message (x‘F’)			
28	Module ID (Note 3)							
29	Routine ID (Note 3)							
2A	Error information							
2B								
2C								
2D								
2E								
2F								
30								
31								
32								
33								
34	PCB number				Not used (x‘00’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF9F’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not usde (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000,2003, Hitachi, Ltd.

Byte27 = 9F (Trace data/Log data) (2/2)



(Note 1)

The pare of system error code x‘AE5A’ (Drive not Ready) and x‘A772’ are reported even when one of the following processes has completed successfully. These indicate the PDEV spin down executed correctly and do not mean the error condition. Please ignore them.

- PDEV replace
- DKU Inline execution at Installation or at PDEV expansion.

(Note 2)

System error code x‘AE5B’ (Unit Attention) is reported even after one of the following processes has completed successfully. It indicates the PDEV was reset correctly and does not mean the error condition. Please ignore it.

- DKA replace
- DKA expansion
- PDEV expansion
- DKA micro-program exchange
- PDEV micro-program exchange

(Note3)

The details information of every Module ID & Routine ID

•Module ID & Routine ID=0xC3A5 ; The Specified R-VOL of HRC is still Online from the HOST.
(Add Pair operation from the host was rejected)

Check the SSB.LOG on SVP of the specified MCU. SSB containing EC=C3A5 on the specified R-VOL number should be logged.

(1) Analyze the SSB.LOG

Refer to the case of Byte27=0X(X≠8/A) for the way of tracing an on-line host.
But, only the Byte position of BitMap information is different. Refer to Byte100(0x64)-103(0x67) of SSB for the BitMap information.

Copyright ©2000,2003, Hitachi, Ltd.

Byte27 = EC (Envirnment Monitor Detected DKC Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘E’)				Message (x‘C’)			
28	Error detection code (Note 1)							
29	Error detection code (Note 2)							
2A	Error reason code (Note 3)							
2B								
2C	Reserved area							
2D								
2E								
2F								
30								
31								
32								
33								
34	PCB number (don’t care)				Message code (don’t care)			
35	SSID(low) of self subsystem (don’t care)							
36	Symptom code (x‘FFEC’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not usde							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = EC (Environment Monitor Detected DKC Failure) (2/2)

	0	1	2	3	4	5	6	7
40	Error Detection Code 1 (Note 1)							
41	Error Detection Code 2 (Note 2)							
42	Error Detection Code 3 (Note 3)							
43								
|	Not used							
7F								

(Note 1)Error Detection Code

Code	Detection
10	DKCMN1
20	DKCMN2
1A	DKCMN1
2A	DKCMN2
11	DKUMN-R1F
21	DKUMN-R1R
12	DKUMN-R2F
22	DKUMN-R2R
13	DKUMN-R3F
23	DKUMN-R3R
15	DKUMN-L1F
25	DKUMN-L1R
16	DKUMN-L2F
26	DKUMN-L2R
17	DKUMN-L3F
27	DKUMN-L3R

(Note 2)Error Component Code

Code	Component	Code	Component
10	Logic 1	61	HDU-R31
11	Logic 2	62	HDU-R32
20	HDU-R10(HDU-0)	63	HDU-R33
21	HDU-R11(HDU-1)	64	HDU-R34
22	HDU-R12(HDU-2)	65	HDU-R35
23	HDU-R13(HDU-3)	66	HDU-R36
24	HDU-R14	67	HDU-R37
25	HDU-R15	70	HDU-L30
26	HDU-R16	71	HDU-L31
27	HDU-R17	72	HDU-L32
30	HDU-L10	73	HDU-L33
31	HDU-L11	74	HDU-L34
32	HDU-L12	75	HDU-L35
33	HDU-L13	76	HDU-L36
34	HDU-L14	77	HDU-L37
35	HDU-L15	A0	DKCMN1
36	HDU-L16	A1	DKCMN2
37	HDU-L17	A2	SSVP
40	HDU-R20	A3	CE Panel
41	HDU-R21	B0	DKUMN-R1F(DKUMN1)
42	HDU-R22	B1	DKUMN-R1R(DKUMN2)
43	HDU-R23	B2	DKUMN-L1F
44	HDU-R24	B3	DKUMN-L1R
45	HDU-R25	B4	DKUMN-R2F
46	HDU-R26	B5	DKUMN-R2R
47	HDU-R27	B6	DKUMN-L2F
50	HDU-L20	B7	DKUMN-L2R
51	HDU-L21	B8	DKUMN-R3F
52	HDU-L22	B9	DKUMN-R3R
53	HDU-L23	BA	DKUMN-L3F
54	HDU-L24	BB	DKUMN-L3R
55	HDU-L25	D0	ACBOX-R10
56	HDU-L26	D1	ACBOX-R11
57	HDU-L27	E0	DKC AcBox1
60	HDU-R30	E1	DKC AcBox2

Copyright ©2000,2002, Hitachi, Ltd.

(Note 3) Error Reason Code

Code	Reason
10	Abnormal Temperature (over 60°C) is detected in the front side.
11	Abnormal Temperature (over 60°C) is detected in the Back side.
12	Abnormal Temperature (over 40°C) is detected in the front side.
13	Abnormal Temperature (over 40°C) is detected in the Back side.
20	5V voltage has dropped below 80%
21	3V voltage has dropped below 80%
22	12V voltage has dropped below 80%
30	Voltage for shared memory has dropped below 80%
31	Voltage for cache memory has dropped below 80%
40	5/3V PS(A) Box abnormality has been detected.
41	5/3V PS(B) Box abnormality has been detected.
42	3V PS(A) Box abnormality has been detected.
43	3V PS(B) Box abnormality has been detected.
44	3V PS(C) Box abnormality has been detected.
45	3V PS(D) Box abnormality has been detected.
46	SUB PS Box abnormality has been detected.
4A	HDU MPS-0 abnormality has been detected.
4B	HDU MPS-1 abnormality has been detected.
50	Battery 0 abnormality has been detected.
51	Battery 1 abnormality has been detected.
52	Battery 2 abnormality has been detected.
5A	Battery 0 abnormality has been detected. (DIAG)
5B	Battery 1 abnormality has been detected. (DIAG)
5C	Battery 2 abnormality has been detected. (DIAG)
60	AC power off/interruption of breaker box occurred.
70	Low rotation speed of FAN has been detected.
81	JP for DKC voltage alarm inhibit remains
83	JP for HDU-0-HDU-3 voltage alarm inhibit remains
84	JP for HDU-4-HDU-7 voltage alarm inhibit remains
85	JP for SVP P/S Off/On inhibit remains
90	Environment monitor register access error.
91	Environment monitor register BUSY error.
92	Environment monitor register DIAG mode error.
A0	Environment monitors disagree error occurred.
A1	Environment monitors disagree error of P/S occurred.

Copyright ©2000,2002, Hitachi, Ltd.

Byte27 = EE (Envirnment Monitor Detected DKU Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘E’)				Message (x‘E’)			
28	Error detection code (Note 1)							
29	Error detection code (Note 2)							
2A	Error reason code (Note 3)							
2B								
2C	Reserved area							
2D								
2E								
2F								
30								
31								
32								
33								
34	PCB number (don’t care)				Message code (don’t care)			
35	SSID (low) of self subsystem (don’t care)							
36	Symptom code (x‘FFEE’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not usde							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = EE (Environment Monitor Detected DKU Failure) (2/2)

	0	1	2	3	4	5	6	7
40	Error Detection Code 1 (Note 1)							
41	Error Detection Code 2 (Note 2)							
42	Error Detection Code 3 (Note 3)							
43								
|	Not used							
7F								

(Note 1)Error Detection Code

Code	Detection
10	DKCMN1
20	DKCMN2
1A	DKCMN1
2A	DKCMN2
11	DKUMN-R1F
21	DKUMN-R1R
12	DKUMN-R2F
22	DKUMN-R2R
13	DKUMN-R3F
23	DKUMN-R3R
15	DKUMN-L1F
25	DKUMN-L1R
16	DKUMN-L2F
26	DKUMN-L2R
17	DKUMN-L3F
27	DKUMN-L3R

(Note 2)Error Component Code

Code	Component	Code	Component
10	Logic 1	61	HDU-R31
11	Logic 2	62	HDU-R32
20	HDU-R10(HDU-0)	63	HDU-R33
21	HDU-R11(HDU-1)	64	HDU-R34
22	HDU-R12(HDU-2)	65	HDU-R35
23	HDU-R13(HDU-3)	66	HDU-R36
24	HDU-R14	67	HDU-R37
25	HDU-R15	70	HDU-L30
26	HDU-R16	71	HDU-L31
27	HDU-R17	72	HDU-L32
30	HDU-L10	73	HDU-L33
31	HDU-L11	74	HDU-L34
32	HDU-L12	75	HDU-L35
33	HDU-L13	76	HDU-L36
34	HDU-L14	77	HDU-L37
35	HDU-L15	A0	DKCMN1
36	HDU-L16	A1	DKCMN2
37	HDU-L17	A2	SSVP
40	HDU-R20	A3	CE Panel
41	HDU-R21	B0	DKUMN-R1F(DKUMN1)
42	HDU-R22	B1	DKUMN-R1R(DKUMN2)
43	HDU-R23	B2	DKUMN-L1F
44	HDU-R24	B3	DKUMN-L1R
45	HDU-R25	B4	DKUMN-R2F
46	HDU-R26	B5	DKUMN-R2R
47	HDU-R27	B6	DKUMN-L2F
50	HDU-L20	B7	DKUMN-L2R
51	HDU-L21	B8	DKUMN-R3F
52	HDU-L22	B9	DKUMN-R3R
53	HDU-L23	BA	DKUMN-L3F
54	HDU-L24	BB	DKUMN-L3R
55	HDU-L25	D0	ACBOX-R10
56	HDU-L26	D1	ACBOX-R11
57	HDU-L27	E0	DKC AcBox1
60	HDU-R30	E1	DKC AcBox2

Copyright ©2000,2002, Hitachi, Ltd.

(Note 3) Error Reason Code

Code	Reason
10	Abnormal Temperature (over 60°C) is detected in the front side.
11	Abnormal Temperature (over 60°C) is detected in the Back side.
12	Abnormal Temperature (over 40°C) is detected in the front side.
13	Abnormal Temperature (over 40°C) is detected in the Back side.
20	5V voltage has dropped below 80%
21	3V voltage has dropped below 80%
22	12V voltage has dropped below 80%
30	Voltage for shared memory has dropped below 80%
31	Voltage for cache memory has dropped below 80%
40	5/3V PS(A) Box abnormality has been detected.
41	5/3V PS(B) Box abnormality has been detected.
42	3V PS(A) Box abnormality has been detected.
43	3V PS(B) Box abnormality has been detected.
44	3V PS(C) Box abnormality has been detected.
45	3V PS(D) Box abnormality has been detected.
46	SUB PS Box abnormality has been detected.
4A	HDU MPS-0 abnormality has been detected.
4B	HDU MPS-1 abnormality has been detected.
50	Battery 0 abnormality has been detected.
51	Battery 1 abnormality has been detected.
52	Battery 2 abnormality has been detected.
5A	Battery 0 abnormality has been detected. (DIAG)
5B	Battery 1 abnormality has been detected. (DIAG)
5C	Battery 2 abnormality has been detected. (DIAG)
60	AC power off/interruption of breaker box occurred.
70	Low rotation speed of FAN has been detected.
81	JP for DKC voltage alarm inhibit remains
83	JP for HDU-0-HDU-3 voltage alarm inhibit remains
84	JP for HDU-4-HDU-7 voltage alarm inhibit remains
85	JP for SVP P/S Off/On inhibit remains
90	Environment monitor register access error.
91	Environment monitor register BUSY error.
92	Environment monitor register DIAG mode error.
A0	Environment monitors disagree error occurred.
A1	Environment monitors disagree error of P/S occurred.

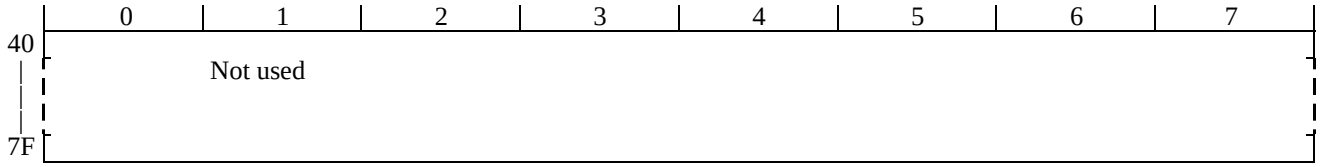
Copyright ©2000,2002, Hitachi, Ltd.

Byte27 = F0 (Operation Terminated) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘F’)				Message (x‘E’)			
28	Not used (x‘00’)							
29	Not used (x‘00’)							
2A	Not used (x‘00’)							
2B	Hardware level (Note 1)							
2C								
2D	SSID of mate subsystem (x‘0000’ for EDCC)							
2E								
2F	Maker code & Manufacture code (x‘00’)							
30	Not used (x‘00’)							
31	Module ID							
32	Routine ID							
33	PCB number				Message code (x‘0’)			
34	SSID of self subsystem							
35								
36	Symptom code (x‘FFF0’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘1D’)							
3A	Configuration information							
3B								
3C	Not usde (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = F0 (Openation Terminated) (2/2)



(Note 1) Hardware level

Bit0 : Hardware level flag

For bit0=0

Bit 1	:	Not used
Bit 2 ~ 3	:	SP number
Bit 4 ~ 5	:	CHLs per Cluster
		00 : 4
		01 : 8
		10 : Not used
		11 : Not used
Bit 6	:	NVS
		0 : Without NVS
		1 : With NVS
Bit 7	:	Not used
Bit 8 ~ 10	:	Cache size
		000 : Non cache
		001 : 256MB
		010 : 512MB
		011 : 768MB
		100 : 1024MP
		101 : 1280MP
		110 : 1536MP
		111 : Over 1536MB
Bit11 ~ 13	:	Cluster hardware level
Bit14 ~ 15	:	Cache/NVS hardware level

For bit0=1

Bit 1	:	Not used
Bit 2 ~ 3	:	SP number
Bit 4 ~ 5	:	CHLs per Cluster
		0000 : Parallel=4, Serial=0
		0001 : Parallel=8, Serial=0
		0010 : Parallel=4, Serial=2
		0100 : Parallel=4, Serial=4
		0110 : Parallel=0, Serial=2
		1000 : Parallel=0, Serial=4
		1010 : Parallel=0, Serial=8
		1100 : Parallel=0, Serial=8
Bit 8	:	DUAL FRAME
		0 : DUAL FRAME
		1 : MODULAR POWER
Bit 9 ~ 11	:	Cache size
		000 : Non cache
		001 : 256MB
		010 : 512MB
		011 : 768MB
		100 : 1024MB
		101 : 1280MB
		110 : 1536MB
		111 : Over 1536MB
Bit12 ~ 13	:	Cluster hardware level
Bit14 ~ 15	:	Cache/NVS hardware level

Copyright ©2000, Hitachi, Ltd.

Byte27 = F1 (Micro-program Detected Cache Failure) (1/2)

	0	1	2	3	4	5	6	7	
00	Time stamp								
05									
06	Format Message								
07	PCB type		Processor ID (Note)						
08	System error code								
09									
0A	JCB ID								
0B									
0C	REQ ID								
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log	
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0	
0F	SEMI-SYNC	RCU SIM	0	0		RCU#			
10	LDEV number								
11									
12	CDEV#								
13	RDEV#								
14	RCU LDEV number								
15									
16	SSB log number								
17									
18	Related failure log number								
19									
1A	Related SIM log number								
1B									
1C	Related SSB log number								
1D									
1E	(Reserved)								
1F	SCB								
20	Basic SSB								
21									
22									
23	Count								
24	Device address								
25	Cylinder addres (low)								
26	Cylinder address (high)				Head address				
27	Format (x‘F’)				Message (x‘1’)				
28	Queue transition in progress (Side A)	Queue transition in progress (Side B)	Free SGCB queue operation in progress	Free SLCB queue operation in progress	Free GRPT queue operation in progress	Not used			
29	Not used								*
	VDEV number								*
2A	Queue type								*
	VDEV number		Slot number						*
2B	Queue number								*
	Slot number								*
2C	Queue number								*
	Slot number								*
2D	SSID of mate subsystem (x‘0000’ for EDCC)								
2E									
2F	Maker code & Manufacture code (x‘00’)								
30	Not used (x‘00’)								

* : When byte 28, bit2-4 = 000, upper value is valid.
: When byte 28, bit2-4 ≠ 000, lower value is valid.

Copyright ©2000, Hitachi, Ltd.

Byte27 = F1 (Micro-program Detected Cache Failure) (2/2)

	0	1	2	3	4	5	6	7
31	Module ID							
32	Routine ID							
33	PCB number				Message code (x‘0’)			
34	SSID of self subsystem							
35								
36	Symptom code (x‘FFF1’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not usde (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							
40	Error information							
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = F2 (CACHE CHK2)

	0	1	2	3	4	5	6	7
00	Time Stamp							
|								
05								
06	Format Message							
07	P/K Type		Processer ID					
08	System Error Code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	HOST Report	SVP Report	Force Log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	PORT#		RCU#			
10	LDEV#							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV#							
15								
16	Internal SSB Log Number							
17								
18	Related Failure Log Number							
19								
1A	Related SIM Log Number							
1B								
1C	Related SSB Log Number							
1D								
1E	(Reserved)							
1F	SCB							
20	Inf valid	Err Code						
21	Segment Number							
22	Filemark	ECM	ILI	Reserved	Sense Key			
23	Information Bytes							
24								
25								
26								
27	Format (x‘F’)				Message (x‘2’)			
28	SubCode							
29	Detail Information (See Following Pages.)							
|								
2C								
2D	SSID for Other Subsystem (x‘0000’ for EDCC)							
2E								
2F	Maker Code						Factory Code	
30	Detail Information (See Following Pages.)							
31	Module ID							
32	Routine ID							
33	P/K ID				Err Code (Don’t Care)			
34	SSID for Self Subsystem							
35								
36	Symptom Code (x‘FF89’:LDEV Type=DKU87I / x‘EF89’: LDEV Type=DKU86I)							
37								
38	Log and Message Control (x‘00’)							
39	Program Action Control (x‘00’)							
3A	Configuration Information							
3B								
3C	Not Used							
3D	Cylinder Address							
3E								
3F	Head Address							
40	Detail Information (See Following Pages.)							
|								
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = F2 (CACHE CHK2) Byte28-31 Detail

	0	1	2	3	4	5	6	7
28	SubCode							
	Error Detected: ‘1’ = P PATH ERR(DTA) ‘2’ = P or C PATH ERR(DTA) ‘3’ = P PATH ERR(CSW) ‘4’ = P or C PATH ERR(CSW) ‘5’ = C PATH ERR(CSW) ‘7’ = C PATH ERR(CMA) ‘8’ = CACHE BOARD ERR ‘9’ = CACHE MEMORY ERR				CARB BOARD ERR ‘0’ = NO ‘1’ = YES	CMA BOARD ERR ‘0’ = NO ‘1’ = YES	CARB REG LOG RESULT ‘0’ = OK ‘1’ = NG	CMA REG LOG RESULT ‘0’ = OK ‘1’ = NG
29	Transfer Information							
	Transfer P/K Type and Master Path ‘0’ = ESCON CHA ‘4’ = FIBRE CHA(PMA) ‘5’ = FIBRE CHA(DMA) ‘7’ = FIBRE DKA(FCA) ‘8’ = FIBRE DKA(DRR)				Transfer Mode 0’ = NORMAL WRITE ‘1’ = NORMAL READ ‘2’ = 2SLAVE WRITE ‘3’ = CACHE COPY(CtoC) ‘4’ = CACHE COPY(CinC)			
2A	Using Path Code							
	XFR P PATH# ‘0’ = P#0 ‘1’ = P#1	LOG P PATH# ‘0’=ORIGIN ‘1’=OTHER	(RSV)	(RSV)	SLAVE#1 CACHE P/K# (‘0’ - ‘3’)		SLAVE#2 CACHE P/K# (‘0’ - ‘3’)	
2B	STATUS0(SLAVE 1) byte0							
	STATUS0 ERR	STATUS0 CARB ERR	STATUS0 CMA ERR	STATUS0 Reserved	STATUS0 CMA STATUS NG	STATUS0 CMA FIFO MODE	STATUS0 CMA WARNING	STATUS0 Reserved
2C	STATUS1(SLAVE 2) byte0							
	STATUS1 ERR	STATUS1 CARB ERR	STATUS1 CMA ERR	STATUS1 Reserved	STATUS1 CMA STATUS NG	STATUS1 CMA FIFO MODE	STATUS1 CMA WARNING	STATUS1 Reserved

30	STATUS0(SLAVE 1) byte1			
	STATUS0 Reserved	STATUS0 PATH ID# (‘0’ - ‘7’)	STATUS0 Reserved	STATUS0 Answer CACHE# (‘0’ - ‘3’)

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(1) Byte29 bit0 - 3 = 0 and Byte31 = 58/59 (1/4)

	0	1	2	3	4	5	6	7
40	STATUS1(SLAVE 2) byte1							
	STATUS1 Reserved	STATUS1 PATH ID			STATUS1 Reserved		STATUS1 CACHE P/K#	
41	STATUS0(SLAVE 1) byte2							
	STS0 CARB PXDR INDPE	STS0 CARB PXLRCE	STS0 CARB PXDR OUTDPE	STS0 CARB PXOR INDPE	STS0 CARB PXTME	STS0 CARB ABTE	STS0 CARB PXHE	STS0 CARB PXMAE
42	STATUS0(SLAVE 1) byte3							
	STS0 CARB CXOR INDPE	STS0 CARB CXDR INDPE	STS0 CARB CXLRCE	STS0 CARB CXDR OUTDPE	STS0 CARB CXTME	STS0 CARB CXHE	STS0 CARB Reserved	STS0 CARB Reserved
43	STATUS0(SLAVE 1) byte4							
	STS0 CMA BOARD DISABLE	STS0 CMA MEM NOT RDY	STS0 CMA MODULE DISABLE	STS0 CMA MEM BACKUP MODE	STS0 CMA DIAG UMNT	STS0 CMA SP UMNT	STS0 CMA REG CODE ERR	STS0 CMA INVLD COM
44	STATUS0(SLAVE 1) byte5							
	STS0 CMA PKID PEER	STS0 CMA GSLRCER	STS0 CMA DT PKT ER	STS0 CMA CMD PKT ER	STS0 CMA MODULE ER	STS0 CMA HCTL ER	STS0 CMA MCTL ER	STS0 CMA BRD ER
45	STATUS0(SLAVE 2) byte2							
	STS1 CARB PXDR INDPE	STS1 CARB PXLRCE	STS1 CARB PXDR OUTDPE	STS1 CARB PXOR INDPE	STS1 CARB PXTME	STS1 CARB ABTE	STS1 CARB PXHE	STS1 CARB PXMAE
46	STATUS0(SLAVE 2) byte3							
	STS1 CARB CXOR INDPE	STS1 CARB CXDR INDPE	STS1 CARB CXLRCE	STS1 CARB CXDR OUTDPE	STS1 CARB CXTME	STS1 CARB CXHE	STS1 CARB Reserved	STS1 CARB Reserved
47	STATUS0(SLAVE 2) byte4							
	STS1 CMA BOARD DISABLE	STS1 CMA MEM NOT RDY	STS1 CMA MODULE DISABLE	STS1 CMA MEM BACKUP MODE	STS1 CMA DIAG UMNT	STS1 CMA SP UMNT	STS1 CMA REG CODE ERR	STS1 CMA INVLD COM
48	STATUS0(SLAVE 2) byte5							
	STS1 CMA PKID PEER	STS1 CMA GSLRCER	STS1 CMA DT PKT ER	STS1 CMA CMD PKT ER	STS1 CMA MODULE ER	STS1 CMA HCTL ER	STS1 CMA MCTL ER	STS1 CMA BRD ER
49	CMA:: ADDRESSERR1 / DATAERR1							
	SLAVE1 ADR PARITY ERR	SLAVE1 CMD PARITY ERR	SLAVE1 ADR/CMD 0 PARITY ERR	SLAVE1 ADR/CMD 1 PARITY ERR	ADR/CMD PLRC ERR	WRITE DATA PARITY ERR	WRITE LOOP DATA PARITY ERR	WRITE DATA PLRC ERR
4A	CMA::ADDRESSERR1							
	SLAVE1 LEN ZERO	SLAVE1 LEN BNDER	SLAVE1 LEN OVER	SLAVE1 CMD CNSTER	CP CMD ERR	NOT SEL ERR	END-CODE ERR	ENT OFF
4B	CMA::ADDRESSERR2							
	SLAVE2 ADR PARITY ERR	SLAVE2 CMD PARITY ERR	SLAVE2 ADR/CMD 0 PARITY ERR	SLAVE2 ADR/CMD 1 PARITY ERR	END-CODE PARITY ERR	(RSV)	(RSV)	(RSV)
4C	CMA::ADDRESSERR2							
	SLAVE2 LEN ZERO	SLAVE2 LEN BNDER	SLAVE2 LEN OVER	SLAVE2 CMD CNSTER	INVL CMD ERR	ONE SLAVE ERR	PATH ERR	HEAD TIME OUT
4D	CMA::DATAERR1							
	PLRC ERR	PAD ERR	WRITE DATA0 PARITY ERR	WRITE DATA1 PARITY ERR	TX PLRC ERR	TX PAD ERR	TX BYTE0 PARITY ERR	TX BYTE1 PARITY ERR
4E	CMA::DATAERR2							
	WRITE SLRC ERR	READ SLRC ERR	MEM UNCORRECT ERR	MEM CORRECT ERR	MEM DATA ERR	REG PATH ERR	MEM WRITE UNDER RUN ERR	(RSV)
4F	CMA::PORTBRDERR1							
	TIME OUT CNT1(M) PARITY ERR	TIME OUT CNT2(M) PARITY ERR	TIME OUT CNT1(PR) PARITY ERR	TIME OUT CNT2(PR) PARITY ERR	HSEQ PARITY ERR	RXSEQ PARITY ERR	TXSEQ PARITY ERR	FIFO READ DATA LEN ERR

Copyright ©2000, Hitachi, Ltd.

Byte27 = F2 (CACHE CHK2) Byte40-7F Detail

(1) Byte29 bit0 - 3 = 0 and Byte31 = 58/59 (2/4)

	0	1	2	3	4	5	6	7
50	CMA::PORTBRDERR1							
	FIFO WRITE DATA LEN ERR	FIFO READ PNT PARITY ERR	FIFO WRITE PNT PARITY ERR	PR PARITY ERR	MCT PARITY ERR	CMCT PARITY ERR	(RSV)	PCNV ERR
51	CMA::PORTBRDERR2 / BOARDEXPTERR							
	DATA TIME OUT	ARB TIME OUT	HCTL-MCTL I/F ERR	HTCL-RCTL I/F ERR	MCTL HARD ERR	PATH CLOCK ERR	MEM CLOCK ERR	RCTL HARD ERR
52	CMA::SETUPERR / BOARDEXPTERR							
	BOARD DISABLE	MEM NOT RDY	MODULE DISABLE	BACK UP BUSY	DIAG UNMATCH	SP UNMATCH	REG CODE ERR	PKID PARITY ERR
53	CMA::BOARDERR0 / BOARDERR2							
	READ ECC UNCORRECT ERR	READ ECC CORRECT ERR	WRITE ECC CORRECT ERR	REGCLT ADR CNT PARITY ERR	REGCLT TF CNT PARITY ERR	REGCLT CNT OVER	(RSV)	(RSV)
54	CMA::BOARDERR1							
	CTL LOOP PARITY CHK 000 ERR	CTL LOOP PARITY CHK 001 ERR	CTL LOOP PARITY CHK 002 ERR	CTL LOOP PARITY CHK 003 ERR	CTL LOOP PARITY CHK 010 ERR	CTL LOOP PARITY CHK 011 ERR	CTL LOOP PARITY CHK 012 ERR	CTL LOOP PARITY CHK 013 ERR
55	CMA::BOARDERR1							
	CTL LOOP PARITY CHK 100 ERR	CTL LOOP PARITY CHK 101 ERR	CTL LOOP PARITY CHK 102 ERR	CTL LOOP PARITY CHK 103 ERR	CTL LOOP PARITY CHK 110 ERR	CTL LOOP PARITY CHK 111 ERR	CTL LOOP PARITY CHK 112 ERR	CTL LOOP PARITY CHK 113 ERR
56	CMA::BOARDERR2							
	PORT ADR ERR	PORT CNT	PORT PLRC ERR	PORT WRITE DATA PARITY ERR	OTHER PORT ADR ERR	OTHER PORT CNT	OTHER PORT PLRC ERR	OTHER PORT WRITE DATA PARITY ERR
57	CMA::BOARDERR3 / PSCTL							
	MCTL MAINSEQ ERR	MCTL INISEQ ERR	MCTL PWDSEQ ERR	MCTL REFSEQ ERR	MCTL REGSEQ ERR	MCTL MEMSEQ ERR	(RSV)	CACHE P/K PS DOWN
58	CMA::BOARDERR4 / PD_SROM							
	PATH CLOCK ERR	MEM CLOCK ERR	(RSV)	PDCTL ERR	(RSV)	(RSV)	SCK ERR	SDA ERR
59	CMA::PD_SROM							
	SEQ1 ERR	SEQ2 ERR	(RSV)	WRITE DATA PARITY ERR	ACNT ERR	TCNT ERR	BCNT ERR	TIME ERR
5A	CMA::BOARDERR3							
	MCTL TIMECNT ERR	MCTL IREFCNT ERR	MCTL SELFCNT ERR	(RSV)	MCTL TFCNT ERR	ARB ERR	(RSV)	GTL INI TIMER PARITY ERR
5B	CMA::BOARDERR4							
	MEM ADR CNT ERR	ADR CTL ERR	ADR CNT OVER	ADR PARITY ERR	TAG ERR	ECC HARD ERR	REF CNT ERR	REF TIME OUT
5C	CMA::MODULEERR							
	MG#0 ECC UNCORRECT ERR	MG#1 ECC UNCORRECT ERR	MG#2 ECC UNCORRECT ERR	MG#3 ECC UNCORRECT ERR	MG#4 ECC UNCORRECT ERR	MG#5 ECC UNCORRECT ERR	MG#6 ECC UNCORRECT ERR	MG#7 ECC UNCORRECT ERR
5D	CMA::MODULEERR							
	MG#8 ECC UNCORRECT ERR	MG#9 ECC UNCORRECT ERR	MG#10 ECC UNCORRECT ERR	MG#11 ECC UNCORRECT ERR	MG#12 ECC UNCORRECT ERR	MG#13 ECC UNCORRECT ERR	MG#14 ECC UNCORRECT ERR	MG#15 ECC UNCORRECT ERR
5E	CMA::MEMADLOGCAS							
	Error Access CAS Address (Low)							
5F	CARB::PnERR0							
	Pn DR IN DATA PARITY ERR	Pn PATH LRC ERR	Pn PATH END-CODE ERR	Pn PATH SLRC ERR	Pn DR OUT DATA ERR	Pn OR IN DATA PARITY ERR	Pn WR1 TIMER TIME OUT	CLK ERR

Copyright ©2000, Hitachi, Ltd.

Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(1) Byte29 bit0 - 3 = 0 and Byte31 = 58/59 (3/4)

	0	1	2	3	4	5	6	7
60	CARB::PnERR0							
	ABT CMP ERR	ABT SEQ PARITY ERR	Pn SEQA PARITY ERR	Pn IP-CX DR PNT PARITY ERR	Pn SEQA TRF CNT PARITY ERR	Pn SEQB PARITY ERR	CXDR-P0OR PNT PARITY ERR	P0DR-CXOR PNT PARITY ERR
61	CARB::PnERR1							
	Pn SEQB TRF CNT PARITY ERR	Pn SEQD PARITY ERR	Pn SYNC0 CNT PARITY ERR	Pn SYNC1 CNT PARITY ERR	Pn WR1 TIMER PARITY ERR	Pn MICRO ERR	Pn I/O ACS ERR	T6 PARITY ERR
62	CARB::CxERR0							
	Cx OR IN DATA PARITY ERR	Cx DR IN DATA PARITY ERR	Cx PLRC ERR	Cx END-CODE ERR	Cx SLRC ERR	Cx DR OUT DATA PARITY ERR	(RSV)	(RSV)
63	CARB::CxERR0							
	Cx DR1 TIMER TIME OUT	Cx DR2 TIMER TIME OUT	Cx WR2 TIMER TIME OUT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
64	CARB::CxERR1							
	Cx SEQC PARITY ERR	Cx TRF CNT PARITY ERR	Cx DR PNT PARITY ERR	Cx SEQD PARITY ERR	Cx IP PNT0 PARITY ERR	Cx IP PNT1 PARITY ERR	(RSV)	(RSV)
65	CARB::CxERR1							
	Cx RD1 TIMER PARITY ERR	Cx RD2 TIMER PARITY ERR	Cx WT2 TIMER PARITY ERR	Cx STM CNT PARITY ERR	Cx SCM CNT PARITY ERR	(RSV)	(RSV)	(RSV)
66	CARB::CyERR0							
	Cy OR IN DATA PARITY ERR	Cy DR IN DATA PARITY ERR	Cy PLRC ERR	Cy END-CODE ERR	Cy SLRC ERR	Cy DR OUT DATA PARITY ERR	(RSV)	(RSV)
67	CARB::CyERR0							
	Cy DR1 TIMER TIME OUT	Cy DR2 TIMER TIME OUT	Cy WR2 TIMER TIME OUT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
68	CARB::CyERR1							
	Cy SEQC PARITY ERR	Cy TRF CNT PARITY ERR	Cy DR PNT PARITY ERR	Cy SEQD PARITY ERR	Cy IP PNT0 PARITY ERR	Cy IP PNT1 PARITY ERR	(RSV)	(RSV)
69	CARB::CxERR1							
	Cy RD1 TIMER PARITY ERR	Cy RD2 TIMER PARITY ERR	Cy WT2 TIMER PARITY ERR	Cy STM CNT PARITY ERR	Cy SCM CNT PARITY ERR	(RSV)	(RSV)	(RSV)
6A	CHA::CNFSN0							
	(RSV)	PKID#			FORCE PATHSEL	(RSV)	BFRTN	PATHX
6B	CHA::LPEN							
	C PATH#00 ENABLE	C PATH#01 ENABLE	C PATH#02 ENABLE	C PATH#03 ENABLE	C PATH#10 ENABLE	C PATH#11 ENABLE	C PATH#12 ENABLE	C PATH#13 ENABLE
6C	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6D	CHA::MONITOR							
	MODE_1F	XCLM_2F	(RSV)	(RSV)	(RSV)	P0 SYNC ERR	P1 SYNC ERR	P2 SYNC ERR
6E	CMA::LASTXFRPATH / IMPZREF0							
	(RSV)	(RSV)	P0 USE FLAG	P1 USE FLAG	(RSV)	(RSV)	(RSV)	IMP Setting VALID
6F	CHA::IMPZREF0							
	IMP Setting Value for HIGH-LEVEL of LSI_UP Side				IMP Setting Value for LOW-LEVEL of LSI_UP Side			

Copyright ©2000, Hitachi, Ltd.

Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(1) Byte29 bit0 - 3 = 0 and Byte31 = 58/59 (4/4)

	0	1	2	3	4	5	6	7
70		CHA_CHK2ASTS						
	WRBF RD ADR PNT PARITY ERR	RDBF WT ADR PNT PARITY ERR	SC CNT PARITY ERR	LOS CNT PARITY ERR	HARD TIMER PARITY ERR	WRBF PLRC ERR	HSN ADR PARITY ERR	WRBF OUT DT PARITY ERR
71		CHA_CHK2ASTS						
	P0 Receive PARITY ERR	P1 Receive PARITY ERR	X0 Receive PARITY ERR	X1 Receive PARITY ERR	ADRM PARITY ERR	ADRS PARITY ERR	ADRP PARITY ERR	CMD PARITY ERR
72		CHA_CHK2ASTS						
	XFR CNT PARITY ERR	ILPRM0	ILPRM1	ILPRM2	ILPRM3	ILPRM4	ILPRM5	ILPRM6
73		CHA_CHK2ASTS						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
74		CHA_CHK2CSTS						
	TIME OUT0	TIME OUT1	TIME OUT2	HSN RD PLRC ERR	STATUS0 PLRC ERR	STATUS1 PLRC ERR	HSN RD PLRC-INV ERR	STATUS0 PLRC ERR
75		CHA_CHK2CSTS						
	STATUS1 PLRC ERR	HSN RD END-CODE ERR	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	(RSV)	(RSV)	STATUS0 PKID ERR	STATUS1 PKID ERR
76		CHA_CHK2CSTS						
	STATUS0 BYTE0/1 ERR	STATUS1 BYTE0/1 ERR	ACK ERR	ERRINT	LOS	P0 Send PARITY ERR	P1 Send PARITY ERR	X0 Send PARITY ERR
77		CHA_CHK2CSTS						
	X1 Send PARITY ERR	STATUS0 CARB PARITY ERR	STATUS0 CMA PARITY ERR	STATUS1 CARB PARITY ERR	STATUS1 CMA PARITY ERR	(RSV)	(RSV)	(RSV)
78		CHA_CHK2DSTS						
	STATUS0 ERR ON	STATUS1 ERR ON	CARB ERRINT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
79		CHA_MCSA00						
		Slave 1 Cache Transfet Address (BYTE0)						
7A		CHA_MCSA10						
		Slave 2 Cache Transfet Address (BYTE0)						
7B		CHA::CSPGR						
	Slave 1 REG ACCESS FLAG	Slave 1 CARB ACCESS FLAG	(RSV)	(RSV)	Slave 2 REG ACCESS FLAG	Slave 2 CARB ACCESS FLAG	(RSV)	(RSV)
7C		CHA_PCMD2						
	(RSV)	PK ID			Transfer Command			
7D		CHA::XFC0 / XFS0						
		Data Transger Path			CHK2A	CHK2B	CHK2C	CHK2D
7E		CHA_CHK2AST0						
	RDBF PLRC ERR	SLRC ERR	LA ERR	CBUF DT PARITY ERR	SEARCH ERR	SEARCH DT ERR	WRBF INPUT DT PARITY ERR	BYTE ALIGNMENT ERR
7F		CHA_CHK2AST0						
	LCM OUTPUT DT PARITY ERR	(RSV)	LA PARITY ERR	RDBF OUTPUT DT PARITY ERR	HSN PACKET LEN PARITY ERR	(RSV)	(RSV)	(RSV)

Copyright ©2000, Hitachi, Ltd.

Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(2) Byte29 bit0 - 3 = 0 and Byte31 ≠ 58/59 and Byte42 = 58/59

	0	1	2	3	4	5	6	7
40		Causal Key code						
41		Causal Format/Message						
42		Causal Module ID						
43		Causal Routine ID						
44		VDEV and slot number						
45								
46								
47								
48		Slot status						
49								
4A								
4B								
4C		Information of Micro Program						
4D								
4E								
4F								
50		Internal Siearch Parameter (Cylinder number)						
51								
52		Internal Siearch Parameter (Head number)						
53		Internal Siearch Parameter (Reacord number)						
54		Information of Micro Program						
55								
56								
57								
58								
59								
5A								
5B								
5C								
5D								
5E		Curent Command Code						
5F		Old Command Code						
60		Information of Micro Program						
61								
62								
63								
64								
65								
66								
67								
68								
69								
6A								
6B								
6C								
6D								
6E								
6F								
70								
71								
72								
73								
74								
75								
76								
77								
78								
79								
7A								
7B								
7C		Record number in CBUF						
7D		Key Length in CBUF						
7E		Data Length in CBUF						
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(3) Byte29 bit0 - 3 = 0 and Byte31 ≠ 58/59 and Byte42 ≠ 58/59

	0	1	2	3	4	5	6	7
40		Causal Key code						
41		Causal Format/Message						
42		Causal Module ID						
43		Causal Routine ID						
44		Information of Micro Program						
45								
46								
47								
48								
49								
4A								
4B								
4C								
4D								
4E								
4F								
50								
51								
52								
53								
54								
55								
56								
57								
58								
59								
5A								
5B								
5C								
5D								
5E		Curent Command Code						
5F		Old Command Code						
60		Information of Micro Program						
61								
62								
63								
64								
65								
66								
67								
68								
69								
6A								
6B								
6C								
6D								
6E								
6F								
70								
71								
72								
73								
74								
75								
76								
77								
78								
79								
7A								
7B								
7C								
7D								
7E								
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(2) Byte29 bit0 - 3 = 4 or 5 (1/4)

	0	1	2	3	4	5	6	7
40	STATUS1(SLAVE 2) byte1							
	STATUS1 Reserved	STATUS1 PATH ID			STATUS1 Reserved	STATUS1 CACHE P/K#		
41	STATUS0(SLAVE 1) byte2							
	STS0 CARB PXDR INDPE	STS0 CARB PXLRCE	STS0 CARB PXDR OUTDPE	STS0 CARB PXOR INDPE	STS0 CARB PXTME	STS0 CARB ABTE	STS0 CARB PXHE	STS0 CARB PXMAE
42	STATUS0(SLAVE 1) byte3							
	STS0 CARB CXOR INDPE	STS0 CARB CXDR INDPE	STS0 CARB CXLRCE	STS0 CARB CXDR OUTDPE	STS0 CARB CXTME	STS0 CARB CXHE	STS0 CARB Reserved	STS0 CARB Reserved
43	STATUS0(SLAVE 1) byte4							
	STS0 CMA BOARD DISABLE	STS0 CMA MEM NOT RDY	STS0 CMA MODULE DISABLE	STS0 CMA MEM BACKUP MODE	STS0 CMA DIAG UMNT	STS0 CMA SP UMNT	STS0 CMA REG CODE ERR	STS0 CMA INVLD COM
44	STATUS0(SLAVE 1) byte5							
	STS0 CMA PKID PEER	STS0 CMA GSLRCER	STS0 CMA DT PKT ER	STS0 CMA CMD PKT ER	STS0 CMA MODULE ER	STS0 CMA HCTL ER	STS0 CMA MCTL ER	STS0 CMA BRD ER
45	STATUS0(SLAVE 2) byte2							
	STS1 CARB PXDR INDPE	STS1 CARB PXLRCE	STS1 CARB PXDR OUTDPE	STS1 CARB PXOR INDPE	STS1 CARB PXTME	STS1 CARB ABTE	STS1 CARB PXHE	STS1 CARB PXMAE
46	STATUS0(SLAVE 2) byte3							
	STS1 CARB CXOR INDPE	STS1 CARB CXDR INDPE	STS1 CARB CXLRCE	STS1 CARB CXDR OUTDPE	STS1 CARB CXTME	STS1 CARB CXHE	STS1 CARB Reserved	STS1 CARB Reserved
47	STATUS0(SLAVE 2) byte4							
	STS1 CMA BOARD DISABLE	STS1 CMA MEM NOT RDY	STS1 CMA MODULE DISABLE	STS1 CMA MEM BACKUP MODE	STS1 CMA DIAG UMNT	STS1 CMA SP UMNT	STS1 CMA REG CODE ERR	STS1 CMA INVLD COM
48	STATUS0(SLAVE 2) byte5							
	STS1 CMA PKID PEER	STS1 CMA GSLRCER	STS1 CMA DT PKT ER	STS1 CMA CMD PKT ER	STS1 CMA MODULE ER	STS1 CMA HCTL ER	STS1 CMA MCTL ER	STS1 CMA BRD ER
49	CMA:: ADDRESSERR1 / DATAERR1							
	SLAVE1 ADR PARITY ERR	SLAVE1 CMD PARITY ERR	SLAVE1 ADR/CMD 0 PARITY ERR	SLAVE1 ADR/CMD 1 PARITY ERR	ADR/CMD PLRC ERR	WRITE DATA PARITY ERR	WRITE LOOP DATA PARITY ERR	WRITE DATA PLRC ERR
4A	CMA::ADDRESSERR1							
	SLAVE1 LEN ZERO	SLAVE1 LEN BNDER	SLAVE1 LEN OVER	SLAVE1 CMD CNSTER	CP CMD ERR	NOT SEL ERR	END-CODE ERR	ENT OFF
4B	CMA::ADDRESSERR2							
	SLAVE2 ADR PARITY ERR	SLAVE2 CMD PARITY ERR	SLAVE2 ADR/CMD 0 PARITY ERR	SLAVE2 ADR/CMD 1 PARITY ERR	END-CODE PARITY ERR	(RSV)	(RSV)	(RSV)
4C	CMA::ADDRESSERR2							
	SLAVE2 LEN ZERO	SLAVE2 LEN BNDER	SLAVE2 LEN OVER	SLAVE2 CMD CNSTER	INVL CMD ERR	ONE SLAVE ERR	PATH ERR	HEAD TIME OUT
4D	CMA::DATAERR1							
	PLRC ERR	PAD ERR	WRITE DATA0 PARITY ERR	WRITE DATA1 PARITY ERR	TX PLRC ERR	TX PAD ERR	TX BYTE0 PARITY ERR	TX BYTE1 PARITY ERR
4E	CMA::DATAERR2							
	WRITE SLRC ERR	READ SLRC ERR	MEM UNCORRECT ERR	MEM CORRECT ERR	MEM DATA ERR	REG PATH ERR	MEM WRITE UNDER RUN ERR	(RSV)
4F	CMA::PORTBRDERR1							
	TIME OUT CNT1(M) PARITY ERR	TIME OUT CNT2(M) PARITY ERR	TIME OUT CNT1(PR) PARITY ERR	TIME OUT CNT2(PR) PARITY ERR	HSEQ PARITY ERR	RXSEQ PARITY ERR	TXSEQ PARITY ERR	FIFO READ DATA LEN ERR

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(2) Byte29 bit0 - 3 = 4 or 5 (2/4)

	0	1	2	3	4	5	6	7
50		CMA::PORTBRDERR1						
	FIFO WRITE DATA LEN ERR	FIFO READ PNT PARITY ERR	FIFO WRITE PNT PARITY ERR	PR PARITY ERR	MCT PARITY ERR	CMCT PARITY ERR	(RSV)	PCNV ERR
51		CMA::PORTBRDERR2 / BOARDEXPTERR						
	DATA TIME OUT	ARB TIME OUT	HCTL-MCTL I/F ERR	HTCL-RCTL I/F ERR	MCTL HARD ERR	PATH CLOCK ERR	MEM CLOCK ERR	RCTL HARD ERR
52		CMA::SETUPERR / BOARDEXPTERR						
	BOARD DISABLE	MEM NOT RDY	MODULE DISABLE	BACK UP BUSY	DIAG UNMATCH	SP UNMATCH	REG CODE ERR	PKID PARITY ERR
53		CMA::BOARDERR0 / BOARDERR2						
	READ ECC UNCORRECT ERR	READ ECC CORRECT ERR	WRITE ECC CORRECT ERR	REGCLT ADR CNT PARITY ERR	REGCLT TF CNT PARITY ERR	REGCLT CNT OVER	(RSV)	(RSV)
54		CMA::BOARDERR1						
	CTL LOOP PARITY CHK 000 ERR	CTL LOOP PARITY CHK 001 ERR	CTL LOOP PARITY CHK 002 ERR	CTL LOOP PARITY CHK 003 ERR	CTL LOOP PARITY CHK 010 ERR	CTL LOOP PARITY CHK 011 ERR	CTL LOOP PARITY CHK 012 ERR	CTL LOOP PARITY CHK 013 ERR
55		CMA::BOARDERR1						
	CTL LOOP PARITY CHK 100 ERR	CTL LOOP PARITY CHK 101 ERR	CTL LOOP PARITY CHK 102 ERR	CTL LOOP PARITY CHK 103 ERR	CTL LOOP PARITY CHK 110 ERR	CTL LOOP PARITY CHK 111 ERR	CTL LOOP PARITY CHK 112 ERR	CTL LOOP PARITY CHK 113 ERR
56		CMA::BOARDERR2						
	PORT ADR ERR	PORT CNT	PORT PLRC ERR	PORT WRITE DATA PARITY ERR	OTHER PORT ADR ERR	OTHER PORT CNT	OTHER PORT PLRC ERR	OTHER PORT WRITE DATA PARITY ERR
57		CMA::BOARDERR3 / PSCTL						
	MCTL MAINSEQ ERR	MCTL INISEQ ERR	MCTL PWDSEQ ERR	MCTL REFSEQ ERR	MCTL REGSEQ ERR	MCTL MEMSEQ ERR	(RSV)	CACHE P/K PS DOWN
58		CMA::BOARDERR4 / PD_SROM						
	PATH CLOCK ERR	MEM CLOCK ERR	(RSV)	PDCTL ERR	(RSV)	(RSV)	SCK ERR	SDA ERR
59		CMA::PD_SROM						
	SEQ1 ERR	SEQ2 ERR	(RSV)	WRITE DATA PARITY ERR	ACNT ERR	TCNT ERR	BCNT ERR	TIME ERR
5A		CMA::BOARDERR3						
	MCTL TIMECNT ERR	MCTL IREFCNT ERR	MCTL SELFCNT ERR	(RSV)	MCTL TFCNT ERR	ARB ERR	(RSV)	GTL INI TIMER PARITY ERR
5B		CMA::BOARDERR4						
	MEM ADR CNT ERR	ADR CTL ERR	ADR CNT OVER	ADR PARITY ERR	TAG ERR	ECC HARD ERR	REF CNT ERR	REF TIME OUT
5C		CMA::MODULEERR						
	MG#0 ECC UNCORRECT ERR	MG#1 ECC UNCORRECT ERR	MG#2 ECC UNCORRECT ERR	MG#3 ECC UNCORRECT ERR	MG#4 ECC UNCORRECT ERR	MG#5 ECC UNCORRECT ERR	MG#6 ECC UNCORRECT ERR	MG#7 ECC UNCORRECT ERR
5D		CMA::MODULEERR						
	MG#8 ECC UNCORRECT ERR	MG#9 ECC UNCORRECT ERR	MG#10 ECC UNCORRECT ERR	MG#11 ECC UNCORRECT ERR	MG#12 ECC UNCORRECT ERR	MG#13 ECC UNCORRECT ERR	MG#14 ECC UNCORRECT ERR	MG#15 ECC UNCORRECT ERR
5E		CMA::MEMADLOGCAS						
		Error Access CAS Address (Low)						
5F		CARB::PnERR0						
	Pn DR IN DATA PARITY ERR	Pn PATH LRC ERR	Pn PATH END-CODE ERR	Pn PATH SLRC ERR	Pn DR OUT DATA ERR	Pn OR IN DATA PARITY ERR	Pn WR1 TIMER TIME OUT	CLK ERR

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(2) Byte29 bit0 - 3 = 4 or 5 (3/4)

	0	1	2	3	4	5	6	7
60	CARB::PnERR0							
	ABT CMP ERR	ABT SEQ PARITY ERR	Pn SEQA PARITY ERR	Pn IP-CX DR PNT PARITY ERR	Pn SEQA TRF CNT PARITY ERR	Pn SEQB PARITY ERR	CXDR-P0OR PNT PARITY ERR	P0DR-CXOR PNT PARITY ERR
61	CARB::PnERR1							
	Pn SEQB TRF CNT PARITY ERR	Pn SEQD PARITY ERR	Pn SYNC0 CNT PARITY ERR	Pn SYNC1 CNT PARITY ERR	Pn WR1 TIMER PARITY ERR	Pn MICRO ERR	Pn I/O ACS ERR	T6 PARITY ERR
62	CARB::CxERR0							
	Cx OR IN DATA PARITY ERR	Cx DR IN DATA PARITY ERR	Cx PLRC ERR	Cx END-CODE ERR	Cx SLRC ERR	Cx DR OUT DATA PARITY ERR	(RSV)	(RSV)
63	CARB::CxERR0							
	Cx DR1 TIMER TIME OUT	Cx DR2 TIMER TIME OUT	Cx WR2 TIMER TIME OUT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
64	CARB::CxERR1							
	Cx SEQC PARITY ERR	Cx TRF CNT PARITY ERR	Cx DR PNT PARITY ERR	Cx SEQD PARITY ERR	Cx IP PNT0 PARITY ERR	Cx IP PNT1 PARITY ERR	(RSV)	(RSV)
65	CARB::CxERR1							
	Cx RD1 TIMER PARITY ERR	Cx RD2 TIMER PARITY ERR	Cx WT2 TIMER PARITY ERR	Cx STM CNT PARITY ERR	Cx SCM CNT PARITY ERR	(RSV)	(RSV)	(RSV)
66	CARB::CyERR0							
	Cy OR IN DATA PARITY ERR	Cy DR IN DATA PARITY ERR	Cy PLRC ERR	Cy END-CODE ERR	Cy SLRC ERR	Cy DR OUT DATA PARITY ERR	(RSV)	(RSV)
67	CARB::CyERR0							
	Cy DR1 TIMER TIME OUT	Cy DR2 TIMER TIME OUT	Cy WR2 TIMER TIME OUT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
68	CARB::CyERR1							
	Cy SEQC PARITY ERR	Cy TRF CNT PARITY ERR	Cy DR PNT PARITY ERR	Cy SEQD PARITY ERR	Cy IP PNT0 PARITY ERR	Cy IP PNT1 PARITY ERR	(RSV)	(RSV)
69	CARB::CxERR1							
	Cy RD1 TIMER PARITY ERR	Cy RD2 TIMER PARITY ERR	Cy WT2 TIMER PARITY ERR	Cy STM CNT PARITY ERR	Cy SCM CNT PARITY ERR	(RSV)	(RSV)	(RSV)
6A	FDTA/M::HADR1UCNT							
	Slave 1 Cache Transfer Address (BYTE0)							
6B	FDTA/M::HADR1LCNT							
	Slave 1 Cache Transfer Address (BYTE1)							
6C	FDTA/M::HADR1LCNT							
	Slave 1 Cache Transfer Address (BYTE2)							
6D	FDTA/M::HADR1LCNT							
	Slave 1 Cache Transfer Address (BYTE3)							
6E	FDTA/M::HADR1LCNT							
	Slave 1 Cache Transfer Address (BYTE4)							
6F	FDTA/M::HADR2UCNT							
	Slave 2 Cache Transfer Address (BYTE0)							

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(2) Byte29 bit0 - 3 = 4 or 5 (4/4)

	0	1	2	3	4	5	6	7
70		FDTA/M::HADR2LCNT						
		Slave 2 Cache Transfer Address (BYTE1)						
71		FDTA/M::HADR2LCNT						
		Slave 2 Cache Transfer Address (BYTE2)						
72		FDTA/M::HADR2LCNT						
		Slave 2 Cache Transfer Address (BYTE3)						
73		FDTA/M::HADR2LCNT						
		Slave 2 Cache Transfer Address (BYTE4)						
74		FDTA/M::HCMD						
		Cache Transfer Command (BYTE0)						
75		FDTA/M::HCMD						
		Cache Transfer Command (BYTE1)						
76		FDTA/M::HxCHK2AST0						
	TX1 ERRINT	TX2 ERRINT	RX ERRINT	TX1 ERREND	TX2 ERREND	RX ERREND	PACK OFF ERR	HSNRDT PARITY ERR
77		FDTA/M::HxCHK2AST0						
	TX1 ENT LOOP BACK ERR	TX2 ENT LOOP BACK ERR	RX ENT LOOP BACK ERR	PRB PARITY ERR	(RSV)	(RSV)	RX PLRC PARITY ERR	RX LRC PARITY ERR
78		FDTA/M::HxCHK2AST0						
	(RSV)	(RSV)	TX1 TIME OUT	(RSV)	TX2 TIME OUT 0	TX2 TIME OUT 1	RX TIME OUT 0	RX TIME OUT 1
79		FDTA/M::DEBUGR						
	P0 ACK/ENT ERR	P1 ACK/ENT ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7A		FDTA/M::HCHK2AST1						
	STATUS1 END-CODE ERR0	STATUS1 END-CODE ERR1	STATUS1 END-CODE ERR2	STATUS1 END-CODE ERR3	STATUS1 INV-PLRC ERR0	STATUS1 INV-PLRC ERR1	STATUS1 CMP ERR0	STATUS1 CMP ERR1
7B		FDTA/M::HCHK2AST1						
	P0 USE FLG	P1 USE FLG	HSN STATUS FLG	STATUS1 PARITY ERR	(RSV)	STATUS1 PLRC ERR0	STATUS1 PLRC ERR1	STATUS1 PKID ERR
7C		FDTA/M::HCHK2AST2						
	STATUS2 END-CODE ERR0	STATUS2 END-CODE ERR1	STATUS2 END-CODE ERR2	STATUS2 END-CODE ERR3	STATUS2 INV-PLRC ERR0	STATUS2 INV-PLRC ERR1	STATUS2 CMP ERR0	STATUS2 CMP ERR1
7D		FDTA/M::HCHK2AST2						
	(RSV)	(RSV)	HSN STATUS FLG	STATUS2 PARITY ERR	(RSV)	STATUS2 PLRC ERR0	STATUS2 PLRC ERR1	STATUS2 PKID ERR
7E		FDTA/M::HCHK2CST2						
	(RSV)	(RSV)	PNTR0 PARITY ERR	PNTR1 PARITY ERR 0	SYNC CMP ERR0	SYNC CMP ERR1	SYNC CMP ERR2	SYNC CMP ERR3
7F		FDTA/M::CBEN						
	C PATH#00 ENABLE	C PATH#01 ENABLE	C PATH#02 ENABLE	C PATH#03 ENABLE	C PATH#10 ENABLE	C PATH#11 ENABLE	C PATH#12 ENABLE	C PATH#13 ENABLE

Copyright ©2000,2001, Hitachi, Ltd.

Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(3) Byte29 bit0 - 3 = 7 (1/4)

	0	1	2	3	4	5	6	7
40	STATUS1(SLAVE 2) byte1							
	STATUS1 Reserved	STATUS1 PATH ID			STATUS1 Reserved	STATUS1 CACHE P/K#		
41	STATUS0(SLAVE 1) byte2							
	STS0 CARB PXDR INDPE	STS0 CARB PXLRCE	STS0 CARB PXDR OUTDPE	STS0 CARB PXOR INDPE	STS0 CARB PXTME	STS0 CARB ABTE	STS0 CARB PXHE	STS0 CARB PXMAE
42	STATUS0(SLAVE 1) byte3							
	STS0 CARB CXOR INDPE	STS0 CARB CXDR INDPE	STS0 CARB CXLRCE	STS0 CARB CXDR OUTDPE	STS0 CARB CXTME	STS0 CARB CXHE	STS0 CARB Reserved	STS0 CARB Reserved
43	STATUS0(SLAVE 1) byte4							
	STS0 CMA BOARD DISABLE	STS0 CMA MEM NOT RDY	STS0 CMA MODULE DISABLE	STS0 CMA MEM BACKUP MODE	STS0 CMA DIAG UMNT	STS0 CMA SP UMNT	STS0 CMA REG CODE ERR	STS0 CMA INVLD COM
44	STATUS0(SLAVE 1) byte5							
	STS0 CMA PKID PEER	STS0 CMA GSLRCER	STS0 CMA DT PKT ER	STS0 CMA CMD PKT ER	STS0 CMA MODULE ER	STS0 CMA HCTL ER	STS0 CMA MCTL ER	STS0 CMA BRD ER
45	STATUS0(SLAVE 2) byte2							
	STS1 CARB PXDR INDPE	STS1 CARB PXLRCE	STS1 CARB PXDR OUTDPE	STS1 CARB PXOR INDPE	STS1 CARB PXTME	STS1 CARB ABTE	STS1 CARB PXHE	STS1 CARB PXMAE
46	STATUS0(SLAVE 2) byte3							
	STS1 CARB CXOR INDPE	STS1 CARB CXDR INDPE	STS1 CARB CXLRCE	STS1 CARB CXDR OUTDPE	STS1 CARB CXTME	STS1 CARB CXHE	STS1 CARB Reserved	STS1 CARB Reserved
47	STATUS0(SLAVE 2) byte4							
	STS1 CMA BOARD DISABLE	STS1 CMA MEM NOT RDY	STS1 CMA MODULE DISABLE	STS1 CMA MEM BACKUP MODE	STS1 CMA DIAG UMNT	STS1 CMA SP UMNT	STS1 CMA REG CODE ERR	STS1 CMA INVLD COM
48	STATUS0(SLAVE 2) byte5							
	STS1 CMA PKID PEER	STS1 CMA GSLRCER	STS1 CMA DT PKT ER	STS1 CMA CMD PKT ER	STS1 CMA MODULE ER	STS1 CMA HCTL ER	STS1 CMA MCTL ER	STS1 CMA BRD ER
49	CMA:: ADDRESSERR1 / DATAERR1							
	SLAVE1 ADR PARITY ERR	SLAVE1 CMD PARITY ERR	SLAVE1 ADR/CMD 0 PARITY ERR	SLAVE1 ADR/CMD 1 PARITY ERR	ADR/CMD PLRC ERR	WRITE DATA PARITY ERR	WRITE LOOP DATA PARITY ERR	WRITE DATA PLRC ERR
4A	CMA::ADDRESSERR1							
	SLAVE1 LEN ZERO	SLAVE1 LEN BNDER	SLAVE1 LEN OVER	SLAVE1 CMD CNSTER	CP CMD ERR	NOT SEL ERR	END-CODE ERR	ENT OFF
4B	CMA::ADDRESSERR2							
	SLAVE2 ADR PARITY ERR	SLAVE2 CMD PARITY ERR	SLAVE2 ADR/CMD 0 PARITY ERR	SLAVE2 ADR/CMD 1 PARITY ERR	END-CODE PARITY ERR	(RSV)	(RSV)	(RSV)
4C	CMA::ADDRESSERR2							
	SLAVE2 LEN ZERO	SLAVE2 LEN BNDER	SLAVE2 LEN OVER	SLAVE2 CMD CNSTER	INVL CMD ERR	ONE SLAVE ERR	PATH ERR	HEAD TIME OUT
4D	CMA::DATAERR1							
	PLRC ERR	PAD ERR	WRITE DATA0 PARITY ERR	WRITE DATA1 PARITY ERR	TX PLRC ERR	TX PAD ERR	TX BYTE0 PARITY ERR	TX BYTE1 PARITY ERR
4E	CMA::DATAERR2							
	WRITE SLRC ERR	READ SLRC ERR	MEM UNCORRECT ERR	MEM CORRECT ERR	MEM DATA ERR	REG PATH ERR	MEM WRITE UNDER RUN ERR	(RSV)
4F	CMA::PORTBRDERR1							
	TIME OUT CNT1(M) PARITY ERR	TIME OUT CNT2(M) PARITY ERR	TIME OUT CNT1(PR) PARITY ERR	TIME OUT CNT2(PR) PARITY ERR	HSEQ PARITY ERR	RXSEQ PARITY ERR	TXSEQ PARITY ERR	FIFO READ DATA LEN ERR

Copyright ©2000, Hitachi, Ltd.

Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(3) Byte29 bit0 - 3 = 7 (2/4)

	0	1	2	3	4	5	6	7
50		CMA::PORTBRDERR1						
	FIFO WRITE DATA LEN ERR	FIFO READ PNT PARITY ERR	FIFO WRITE PNT PARITY ERR	PR PARITY ERR	MCT PARITY ERR	CMCT PARITY ERR	(RSV)	PCNV ERR
51		CMA::PORTBRDERR2 / BOARDEXPTERR						
	DATA TIME OUT	ARB TIME OUT	HCTL-MCTL I/F ERR	HTCL-RCTL I/F ERR	MCTL HARD ERR	PATH CLOCK ERR	MEM CLOCK ERR	RCTL HARD ERR
52		CMA::SETUPERR / BOARDEXPTERR						
	BOARD DISABLE	MEM NOT RDY	MODULE DISABLE	BACK UP BUSY	DIAG UNMATCH	SP UNMATCH	REG CODE ERR	PKID PARITY ERR
53		CMA::BOARDERR0 / BOARDERR2						
	READ ECC UNCORRECT ERR	READ ECC CORRECT ERR	WRITE ECC CORRECT ERR	REGCLT ADR CNT PARITY ERR	REGCLT TF CNT PARITY ERR	REGCLT CNT OVER	(RSV)	(RSV)
54		CMA::BOARDERR1						
	CTL LOOP PARITY CHK 000 ERR	CTL LOOP PARITY CHK 001 ERR	CTL LOOP PARITY CHK 002 ERR	CTL LOOP PARITY CHK 003 ERR	CTL LOOP PARITY CHK 010 ERR	CTL LOOP PARITY CHK 011 ERR	CTL LOOP PARITY CHK 012 ERR	CTL LOOP PARITY CHK 013 ERR
55		CMA::BOARDERR1						
	CTL LOOP PARITY CHK 100 ERR	CTL LOOP PARITY CHK 101 ERR	CTL LOOP PARITY CHK 102 ERR	CTL LOOP PARITY CHK 103 ERR	CTL LOOP PARITY CHK 110 ERR	CTL LOOP PARITY CHK 111 ERR	CTL LOOP PARITY CHK 112 ERR	CTL LOOP PARITY CHK 113 ERR
56		CMA::BOARDERR2						
	PORT ADR ERR	PORT CNT	PORT PLRC ERR	PORT WRITE DATA PARITY ERR	OTHER PORT ADR ERR	OTHER PORT CNT	OTHER PORT PLRC ERR	OTHER PORT WRITE DATA PARITY ERR
57		CMA::BOARDERR3 / PSCTL						
	MCTL MAINSEQ ERR	MCTL INISEQ ERR	MCTL PWDSEQ ERR	MCTL REFSEQ ERR	MCTL REGSEQ ERR	MCTL MEMSEQ ERR	(RSV)	CACHE P/K PS DOWN
58		CMA::BOARDERR4 / PD_SROM						
	PATH CLOCK ERR	MEM CLOCK ERR	(RSV)	PDCTL ERR	(RSV)	(RSV)	SCK ERR	SDA ERR
59		CMA::PD_SROM						
	SEQ1 ERR	SEQ2 ERR	(RSV)	WRITE DATA PARITY ERR	ACNT ERR	TCNT ERR	BCNT ERR	TIME ERR
5A		CMA::BOARDERR3						
	MCTL TIMECNT ERR	MCTL IREFCNT ERR	MCTL SELFCNT ERR	(RSV)	MCTL TFCNT ERR	ARB ERR	(RSV)	GTL INI TIMER PARITY ERR
5B		CMA::BOARDERR4						
	MEM ADR CNT ERR	ADR CTL ERR	ADR CNT OVER	ADR PARITY ERR	TAG ERR	ECC HARD ERR	REF CNT ERR	REF TIME OUT
5C		CMA::MODULEERR						
	MG#0 ECC UNCORRECT ERR	MG#1 ECC UNCORRECT ERR	MG#2 ECC UNCORRECT ERR	MG#3 ECC UNCORRECT ERR	MG#4 ECC UNCORRECT ERR	MG#5 ECC UNCORRECT ERR	MG#6 ECC UNCORRECT ERR	MG#7 ECC UNCORRECT ERR
5D		CMA::MODULEERR						
	MG#8 ECC UNCORRECT ERR	MG#9 ECC UNCORRECT ERR	MG#10 ECC UNCORRECT ERR	MG#11 ECC UNCORRECT ERR	MG#12 ECC UNCORRECT ERR	MG#13 ECC UNCORRECT ERR	MG#14 ECC UNCORRECT ERR	MG#15 ECC UNCORRECT ERR
5E		CMA::MEMADLOGCAS						
		Error Access CAS Address (Low)						
5F		CARB::PnERR0						
	Pn DR IN DATA PARITY ERR	Pn PATH LRC ERR	Pn PATH END-CODE ERR	Pn PATH SLRC ERR	Pn DR OUT DATA ERR	Pn OR IN DATA PARITY ERR	Pn WR1 TIMER TIME OUT	CLK ERR

Copyright ©2000, Hitachi, Ltd.

Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(3) Byte29 bit0 - 3 = 7 (3/4)

	0	1	2	3	4	5	6	7
60		CARB::PnERR0						
	ABT CMP ERR	ABT SEQ PARITY ERR	Pn SEQA PARITY ERR	Pn IP-CX DR PNT PARITY ERR	Pn SEQA TRF CNT PARITY ERR	Pn SEQB PARITY ERR	CXDR-P0OR PNT PARITY ERR	P0DR-CXOR PNT PARITY ERR
61		CARB::PnERR1						
	Pn SEQB TRF CNT PARITY ERR	Pn SEQD PARITY ERR	Pn SYNC0 CNT PARITY ERR	Pn SYNC1 CNT PARITY ERR	Pn WR1 TIMER PARITY ERR	Pn MICRO ERR	Pn I/O ACS ERR	T6 PARITY ERR
62		CARB::CxERR0						
	Cx OR IN DATA PARITY ERR	Cx DR IN DATA PARITY ERR	Cx PLRC ERR	Cx END-CODE ERR	Cx SLRC ERR	Cx DR OUT DATA PARITY ERR	(RSV)	(RSV)
63		CARB::CxERR0						
	Cx DR1 TIMER TIME OUT	Cx DR2 TIMER TIME OUT	Cx WR2 TIMER TIME OUT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
64		CARB::CxERR1						
	Cx SEQC PARITY ERR	Cx TRF CNT PARITY ERR	Cx DR PNT PARITY ERR	Cx SEQD PARITY ERR	Cx IP PNT0 PARITY ERR	Cx IP PNT1 PARITY ERR	(RSV)	(RSV)
65		CARB::CxERR1						
	Cx RD1 TIMER PARITY ERR	Cx RD2 TIMER PARITY ERR	Cx WT2 TIMER PARITY ERR	Cx STM CNT PARITY ERR	Cx SCM CNT PARITY ERR	(RSV)	(RSV)	(RSV)
66		CARB::CyERR0						
	Cy OR IN DATA PARITY ERR	Cy DR IN DATA PARITY ERR	Cy PLRC ERR	Cy END-CODE ERR	Cy SLRC ERR	Cy DR OUT DATA PARITY ERR	(RSV)	(RSV)
67		CARB::CyERR0						
	Cy DR1 TIMER TIME OUT	Cy DR2 TIMER TIME OUT	Cy WR2 TIMER TIME OUT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
68		CARB::CyERR1						
	Cy SEQC PARITY ERR	Cy TRF CNT PARITY ERR	Cy DR PNT PARITY ERR	Cy SEQD PARITY ERR	Cy IP PNT0 PARITY ERR	Cy IP PNT1 PARITY ERR	(RSV)	(RSV)
69		CARB::CxERR1						
	Cy RD1 TIMER PARITY ERR	Cy RD2 TIMER PARITY ERR	Cy WT2 TIMER PARITY ERR	Cy STM CNT PARITY ERR	Cy SCM CNT PARITY ERR	(RSV)	(RSV)	(RSV)
6A		FCA::BMPWT21						
		BPMOC Value When Writing to Cache						
6B		FCA::BMPWT21						
		BPMOC Value When Writing to Cache						
6C		FCA::BMPRD21						
		BPMOC Value When Writing to Cache						
6D		FCA::CHK2F40						
	BBUF OUTPUT DATA PARITY ERR	CC2 SLRC ERR	SLV0 STS PATH ID ERR	SLV1 STS PATH ID ERR	CC3 SLRC ERR	CC3 DATA PLRC0 ERR	CC3 DATA PLRC1 ERR	CC3 DATA INV-PLRC0 ERR
6E		FCA::CHK2F40						
	CC3 INV-PLRC1 ERR	CC3 DATA ENDCODE ERR	CC4 SLRC ERR	SLV0 STS PLRC0 ERR	SLV0 STS PLRC1 ERR	SLV0 STS INV-PLRC0 ERR	SLV0 STS INV-PLRC1 ERR	SLV1 STS PLRC0 ERR
6F		FCA::CHK2F40						
	SLV1 STS PLRC1 ERR	SLV1 STS INV-PLRC0 ERR	SLV1 STS INV-PLRC1 ERR	SLV0 STS ENDCODE ERR	SLV1 STS ENDCODE ERR	SLV0 STS ANY ERR	SLV1 STS ANY ERR	QDTA ANY ERR

Copyright ©2000, Hitachi, Ltd.

Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(3) Byte29 bit0 - 3 = 7 (4/4)

	0	1	2	3	4	5	6	7
70		FCA::CWCSA00						
		Slave 1 Cache Write Address (BYTE0)						
71		FCA::CWCSA0104						
		Slave 1 Cache Write Address (BYTE1)						
72		FCA::CWCSA10						
		Slave 2 Cache Write Address (BYTE0)						
73		FCA::CWCSA1114						
		Slave 2 Cache Write Address (BYTE1)						
74		FCA::CRCSA00						
		Cache Read Address (BYTE0)						
75		FCA::CRCSA0104						
		Cache Read Address (BYTE1)						
76		FCA::QDSTS0						
	ANT ERROR	CHK2A/2B	CHK2C	CHK2D	STATUS0 VALID	STATUS1 VALID	P0 USE FLAG	P1 USE FLAG
77		FCA::QDSTS0						
	P0 ERRINT	P1 ERRINT	STATUS0 C-ERR	STATUS1 C-ERR	DT0 PLRC ERR	DT1 PLRC ERR	STATUS0 PLRC ERR ERR	STATUS0 INV-PLRC ERR
78		FCA::QDSTS0						
	STATUS0 END-CODE ERR	STATUS0 PLRC ERR ERR	STATUS0 INV-PLRC ERR	STATUS0 END-CODE ERR	(RSV)	(RSV)	I/O DT0 ERR	I/O DT1 ERR
79		FCA::QDSTS0						
	I/O DT2 ERR	I/O DT3 ERR	STATUS0 DT0-3 PARITY ERR	STATUS0 DT4-7 PARITY ERR	STATUS1 DT0-3 PARITY ERR	STATUS1 DT4-7 PARITY ERR	TIME OUT	ABT ERR
7A		FCA::QDSTS1						
	DTN SEQ ERR	DTN INPUT CTL ERR	DTN RD CTL ERR	DTN WT CTL ERR	P0 SYNCI PNT ERR	P1 SYNCI PNT ERR	P0 SYNCI CLOCK ERR	P1 SYNCI CLOCK ERR
7B		FCA::QDSTS1						
	P0 SLRC CNT ERR	P0 SEQ ERR	P0 TX RD PNT PARITY ERR	P0 RX WT PNT PARITY ERR	P1 SLRC CNT ERR	P1 SEQ ERR	P1 TX RD PNT PARITY ERR	P1 RX WT PNT PARITY ERR
7C		FCA::QDSTS1						
	I/O DT2 ERR	I/O DT3 ERR	STATUS0 DT0-3 PARITY ERR	STATUS0 DT4-7 PARITY ERR	STATUS1 DT0-3 PARITY ERR	STATUS1 DT4-7 PARITY ERR	TIME OUT	ABT ERR
7D		FCA::QDSTS1						
	TRANS MODE ERR	ADR/CMD PLRC ERR	ADR/CMD END-CODE ERR	ADR/CMD DT PARITY ERR	DTN DT0-3 PARITY ERR	DTN DT4-7 PARITY ERR	P0 PLRC ERR	P1 PLRC ERR
7E		Reserved						
	((RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7F		Reserved						
	((RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

Copyright ©2000, Hitachi, Ltd.

Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(4) Byte29 bit0 - 3 = 8 (1/4)

	0	1	2	3	4	5	6	7
40	STATUS1(SLAVE 2) byte1							
	STATUS1 Reserved	STATUS1 PATH ID			STATUS1 Reserved	STATUS1 CACHE P/K#		
41	STATUS0(SLAVE 1) byte2							
	STS0 CARB PXDR INDPE	STS0 CARB PXLRCE	STS0 CARB PXDR OUTDPE	STS0 CARB PXOR INDPE	STS0 CARB PXTME	STS0 CARB ABTE	STS0 CARB PXHE	STS0 CARB PXMAE
42	STATUS0(SLAVE 1) byte3							
	STS0 CARB CXOR INDPE	STS0 CARB CXDR INDPE	STS0 CARB CXLRCE	STS0 CARB CXDR OUTDPE	STS0 CARB CXTME	STS0 CARB CXHE	STS0 CARB Reserved	STS0 CARB Reserved
43	STATUS0(SLAVE 1) byte4							
	STS0 CMA BOARD DISABLE	STS0 CMA MEM NOT RDY	STS0 CMA MODULE DISABLE	STS0 CMA MEM BACKUP MODE	STS0 CMA DIAG UMNT	STS0 CMA SP UMNT	STS0 CMA REG CODE ERR	STS0 CMA INVLD COM
44	STATUS0(SLAVE 1) byte5							
	STS0 CMA PKID PEER	STS0 CMA GSLRCER	STS0 CMA DT PKT ER	STS0 CMA CMD PKT ER	STS0 CMA MODULE ER	STS0 CMA HCTL ER	STS0 CMA MCTL ER	STS0 CMA BRD ER
45	STATUS0(SLAVE 2) byte2							
	STS1 CARB PXDR INDPE	STS1 CARB PXLRCE	STS1 CARB PXDR OUTDPE	STS1 CARB PXOR INDPE	STS1 CARB PXTME	STS1 CARB ABTE	STS1 CARB PXHE	STS1 CARB PXMAE
46	STATUS0(SLAVE 2) byte3							
	STS1 CARB CXOR INDPE	STS1 CARB CXDR INDPE	STS1 CARB CXLRCE	STS1 CARB CXDR OUTDPE	STS1 CARB CXTME	STS1 CARB CXHE	STS1 CARB Reserved	STS1 CARB Reserved
47	STATUS0(SLAVE 2) byte4							
	STS1 CMA BOARD DISABLE	STS1 CMA MEM NOT RDY	STS1 CMA MODULE DISABLE	STS1 CMA MEM BACKUP MODE	STS1 CMA DIAG UMNT	STS1 CMA SP UMNT	STS1 CMA REG CODE ERR	STS1 CMA INVLD COM
48	STATUS0(SLAVE 2) byte5							
	STS1 CMA PKID PEER	STS1 CMA GSLRCER	STS1 CMA DT PKT ER	STS1 CMA CMD PKT ER	STS1 CMA MODULE ER	STS1 CMA HCTL ER	STS1 CMA MCTL ER	STS1 CMA BRD ER
49	CMA:: ADDRESSERR1 / DATAERR1							
	SLAVE1 ADR PARITY ERR	SLAVE1 CMD PARITY ERR	SLAVE1 ADR/CMD 0 PARITY ERR	SLAVE1 ADR/CMD 1 PARITY ERR	ADR/CMD PLRC ERR	WRITE DATA PARITY ERR	WRITE LOOP DATA PARITY ERR	WRITE DATA PLRC ERR
4A	CMA::ADDRESSERR1							
	SLAVE1 LEN ZERO	SLAVE1 LEN BNDER	SLAVE1 LEN OVER	SLAVE1 CMD CNSTER	CP CMD ERR	NOT SEL ERR	END-CODE ERR	ENT OFF
4B	CMA::ADDRESSERR2							
	SLAVE2 ADR PARITY ERR	SLAVE2 CMD PARITY ERR	SLAVE2 ADR/CMD 0 PARITY ERR	SLAVE2 ADR/CMD 1 PARITY ERR	END-CODE PARITY ERR	(RSV)	(RSV)	(RSV)
4C	CMA::ADDRESSERR2							
	SLAVE2 LEN ZERO	SLAVE2 LEN BNDER	SLAVE2 LEN OVER	SLAVE2 CMD CNSTER	INVL CMD ERR	ONE SLAVE ERR	PATH ERR	HEAD TIME OUT
4D	CMA::DATAERR1							
	PLRC ERR	PAD ERR	WRITE DATA0 PARITY ERR	WRITE DATA1 PARITY ERR	TX PLRC ERR	TX PAD ERR	TX BYTE0 PARITY ERR	TX BYTE1 PARITY ERR
4E	CMA::DATAERR2							
	WRITE SLRC ERR	READ SLRC ERR	MEM UNCORRECT ERR	MEM CORRECT ERR	MEM DATA ERR	REG PATH ERR	MEM WRITE UNDER RUN ERR	(RSV)
4F	CMA::PORTBRDERR1							
	TIME OUT CNT1(M) PARITY ERR	TIME OUT CNT2(M) PARITY ERR	TIME OUT CNT1(PR) PARITY ERR	TIME OUT CNT2(PR) PARITY ERR	HSEQ PARITY ERR	RXSEQ PARITY ERR	TXSEQ PARITY ERR	FIFO READ DATA LEN ERR

Copyright ©2000, Hitachi, Ltd.

Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(4) Byte29 bit0 - 3 = 8 (2/4)

	0	1	2	3	4	5	6	7
50		CMA::PORTBRDERR1						
	FIFO WRITE DATA LEN ERR	FIFO READ PNT PARITY ERR	FIFO WRITE PNT PARITY ERR	PR PARITY ERR	MCT PARITY ERR	CMCT PARITY ERR	(RSV)	PCNV ERR
51		CMA::PORTBRDERR2 / BOARDEXPTERR						
	DATA TIME OUT	ARB TIME OUT	HCTL-MCTL I/F ERR	HTCL-RCTL I/F ERR	MCTL HARD ERR	PATH CLOCK ERR	MEM CLOCK ERR	RCTL HARD ERR
52		CMA::SETUPERR / BOARDEXPTERR						
	BOARD DISABLE	MEM NOT RDY	MODULE DISABLE	BACK UP BUSY	DIAG UNMATCH	SP UNMATCH	REG CODE ERR	PKID PARITY ERR
53		CMA::BOARDERR0 / BOARDERR2						
	READ ECC UNCORRECT ERR	READ ECC CORRECT ERR	WRITE ECC CORRECT ERR	REGCLT ADR CNT PARITY ERR	REGCLT TF CNT PARITY ERR	REGCLT CNT OVER	(RSV)	(RSV)
54		CMA::BOARDERR1						
	CTL LOOP PARITY CHK 000 ERR	CTL LOOP PARITY CHK 001 ERR	CTL LOOP PARITY CHK 002 ERR	CTL LOOP PARITY CHK 003 ERR	CTL LOOP PARITY CHK 010 ERR	CTL LOOP PARITY CHK 011 ERR	CTL LOOP PARITY CHK 012 ERR	CTL LOOP PARITY CHK 013 ERR
55		CMA::BOARDERR1						
	CTL LOOP PARITY CHK 100 ERR	CTL LOOP PARITY CHK 101 ERR	CTL LOOP PARITY CHK 102 ERR	CTL LOOP PARITY CHK 103 ERR	CTL LOOP PARITY CHK 110 ERR	CTL LOOP PARITY CHK 111 ERR	CTL LOOP PARITY CHK 112 ERR	CTL LOOP PARITY CHK 113 ERR
56		CMA::BOARDERR2						
	PORT ADR ERR	PORT CNT	PORT PLRC ERR	PORT WRITE DATA PARITY ERR	OTHER PORT ADR ERR	OTHER PORT CNT	OTHER PORT PLRC ERR	OTHER PORT WRITE DATA PARITY ERR
57		CMA::BOARDERR3 / PSCTL						
	MCTL MAINSEQ ERR	MCTL INISEQ ERR	MCTL PWDSEQ ERR	MCTL REFSEQ ERR	MCTL REGSEQ ERR	MCTL MEMSEQ ERR	(RSV)	CACHE P/K PS DOWN
58		CMA::BOARDERR4 / PD_SROM						
	PATH CLOCK ERR	MEM CLOCK ERR	(RSV)	PDCTL ERR	(RSV)	(RSV)	SCK ERR	SDA ERR
59		CMA::PD_SROM						
	SEQ1 ERR	SEQ2 ERR	(RSV)	WRITE DATA PARITY ERR	ACNT ERR	TCNT ERR	BCNT ERR	TIME ERR
5A		CMA::BOARDERR3						
	MCTL TIMECNT ERR	MCTL IREFCNT ERR	MCTL SELFCNT ERR	(RSV)	MCTL TFCNT ERR	ARB ERR	(RSV)	GTL INI TIMER PARITY ERR
5B		CMA::BOARDERR4						
	MEM ADR CNT ERR	ADR CTL ERR	ADR CNT OVER	ADR PARITY ERR	TAG ERR	ECC HARD ERR	REF CNT ERR	REF TIME OUT
5C		CMA::MODULEERR						
	MG#0 ECC UNCORRECT ERR	MG#1 ECC UNCORRECT ERR	MG#2 ECC UNCORRECT ERR	MG#3 ECC UNCORRECT ERR	MG#4 ECC UNCORRECT ERR	MG#5 ECC UNCORRECT ERR	MG#6 ECC UNCORRECT ERR	MG#7 ECC UNCORRECT ERR
5D		CMA::MODULEERR						
	MG#8 ECC UNCORRECT ERR	MG#9 ECC UNCORRECT ERR	MG#10 ECC UNCORRECT ERR	MG#11 ECC UNCORRECT ERR	MG#12 ECC UNCORRECT ERR	MG#13 ECC UNCORRECT ERR	MG#14 ECC UNCORRECT ERR	MG#15 ECC UNCORRECT ERR
5E		CMA::MEMADLOGCAS						
		Error Access CAS Address (Low)						
5F		CARB::PnERR0						
	Pn DR IN DATA PARITY ERR	Pn PATH LRC ERR	Pn PATH END-CODE ERR	Pn PATH SLRC ERR	Pn DR OUT DATA ERR	Pn OR IN DATA PARITY ERR	Pn WR1 TIMER TIME OUT	CLK ERR

Copyright ©2000, Hitachi, Ltd.

Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(4) Byte29 bit0 - 3 = 8 (3/4)

	0	1	2	3	4	5	6	7
60		CARB::PnERR0						
	ABT CMP ERR	ABT SEQ PARITY ERR	Pn SEQA PARITY ERR	Pn IP-CX DR PNT PARITY ERR	Pn SEQA TRF CNT PARITY ERR	Pn SEQB PARITY ERR	CXDR-P0OR PNT PARITY ERR	P0DR-CXOR PNT PARITY ERR
61		CARB::PnERR1						
	Pn SEQB TRF CNT PARITY ERR	Pn SEQD PARITY ERR	Pn SYNC0 CNT PARITY ERR	Pn SYNC1 CNT PARITY ERR	Pn WR1 TIMER PARITY ERR	Pn MICRO ERR	Pn I/O ACS ERR	T6 PARITY ERR
62		CARB::CxERR0						
	Cx OR IN DATA PARITY ERR	Cx DR IN DATA PARITY ERR	Cx PLRC ERR	Cx END-CODE ERR	Cx SLRC ERR	Cx DR OUT DATA PARITY ERR	(RSV)	(RSV)
63		CARB::CxERR0						
	Cx DR1 TIMER TIME OUT	Cx DR2 TIMER TIME OUT	Cx WR2 TIMER TIME OUT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
64		CARB::CxERR1						
	Cx SEQC PARITY ERR	Cx TRF CNT PARITY ERR	Cx DR PNT PARITY ERR	Cx SEQD PARITY ERR	Cx IP PNT0 PARITY ERR	Cx IP PNT1 PARITY ERR	(RSV)	(RSV)
65		CARB::CxERR1						
	Cx RD1 TIMER PARITY ERR	Cx RD2 TIMER PARITY ERR	Cx WT2 TIMER PARITY ERR	Cx STM CNT PARITY ERR	Cx SCM CNT PARITY ERR	(RSV)	(RSV)	(RSV)
66		CARB::CyERR0						
	Cy OR IN DATA PARITY ERR	Cy DR IN DATA PARITY ERR	Cy PLRC ERR	Cy END-CODE ERR	Cy SLRC ERR	Cy DR OUT DATA PARITY ERR	(RSV)	(RSV)
67		CARB::CyERR0						
	Cy DR1 TIMER TIME OUT	Cy DR2 TIMER TIME OUT	Cy WR2 TIMER TIME OUT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
68		CARB::CyERR1						
	Cy SEQC PARITY ERR	Cy TRF CNT PARITY ERR	Cy DR PNT PARITY ERR	Cy SEQD PARITY ERR	Cy IP PNT0 PARITY ERR	Cy IP PNT1 PARITY ERR	(RSV)	(RSV)
69		CARB::CxERR1						
	Cy RD1 TIMER PARITY ERR	Cy RD2 TIMER PARITY ERR	Cy WT2 TIMER PARITY ERR	Cy STM CNT PARITY ERR	Cy SCM CNT PARITY ERR	(RSV)	(RSV)	(RSV)
6A		DRR::STATS						
	CMD A TRANSFER END	(RSV)	CMD A Transfer Start	CMD A Transfer Excuting	CMD B TRANSFER END	(RSV)	CMD B Transfer Start	CMD B Transfer Excuting
6B		DRR::STATS						
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	ABORT Detected	Force Err Detected
6C		DRR::DRERR						
	DRR CTL ERR	P0 CTL ERR	P1 CTL ERR	DRR DATA ERR	P0 DT ERR	P1 DT ERR	STATUS0 CARB/CMA ERR	STATUS1 CARB/CMA ERR
6D		DRR::DRERR						
	P0 ERR INT	P1 ERR INT	DT ERR	TIME OVER ERR	STATUS0 VALID	STATUS1 VALID	P0 USE FLAG	P1 USE FLAG
6E		DRR::DRESTA1						
	P0 SYNC0 PNT PARITY ERR	P0 SYNC1 PNT PARITY ERR	P0 SYNC0 CLOCK PARITY ERR	P0 SYNC1 CLOCK PARITY ERR	P0 TX SEQ ERR	P0 TX RD PNT PARITY ERR	P0 RX SEQ ERR	P0 RX RD PNT PARITY ERR
6F		DRR::DRESTA2						
	P1 SYNC0 PNT PARITY ERR	P1 SYNC1 PNT PARITY ERR	P1 SYNC0 CLOCK PARITY ERR	P1 SYNC1 CLOCK PARITY ERR	P1 TX SEQ ERR	P1 TX RD PNT PARITY ERR	P1 RX SEQ ERR	P1 RX RD PNT PARITY ERR

Copyright ©2000, Hitachi, Ltd.

Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(4) Byte29 bit0 - 3 = 8 (4/4)

	0	1	2	3	4	5	6	7
70	DRR::DRESTA2							
	P0 SEQ PARITY ERR	P1 SEQ PARITY ERR	SLRC CAL-DT PARITY ERR	SLRC DT PARITY ERR	AC PLRCGEN DT PARITY ERR0	AC PLRCGEN DT PARITY ERR1	DT PLRCGEN DT PARITY ERR0	DT PLRCGEN DT PARITY ERR1
71	DRR::DRESTA3							
	STATUS0 PLRC ERR	STATUS0 INV-PLRC ERR	STATUS1 PLRC ERR	STATUS1 INV-PLRC ERR	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE	LA DT PARITY ERR
72	DRR::DRESTA4							
	ELA/CLA DT PARITY ERR	CMD PARITY ERR AT 64-CMD	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	SLAVE1 CMD-A ADR PARITY ERR	SLAVE1 CMD-B ADR PARITY ERR	SLAVE2 CMD-A ADR PARITY ERR	SLAVE2 CMD-B ADR PARITY ERR
73	DRR::DRESTA4							
	STATUS0 DT0 PARITY ERR	STATUS0 DT1 PARITY ERR	STATUS0 DT2 PARITY ERR	STATUS0 DT3 PARITY ERR	STATUS0 DT4 PARITY ERR	STATUS0 DT5 PARITY ERR	STATUS0 DT6 PARITY ERR	STATUS0 DT7 PARITY ERR
74	DRR::DRESTA5							
	STATUS1 DT0 PARITY ERR	STATUS1 DT1 PARITY ERR	STATUS1 DT2 PARITY ERR	STATUS1 DT3 PARITY ERR	STATUS1 DT4 PARITY ERR	STATUS1 DT5 PARITY ERR	STATUS1 DT6 PARITY ERR	STATUS1 DT7 PARITY ERR
75	FCA::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE
76	DRR::DRESTAD							
	ABT SEQ PARITY ERR (M)	ABT SEQ PARITY ERR (S)	P0 ABT CMP CHK ERR	P1 ABT CMP CHK ERR	PKID CHK ERR	(RSV)	(RSV)	(FSV)
77	DRR::DRESTAD							
	CBUF0/1 DATA0 PARITY ERR	CBUF0/1 DATA1 PARITY ERR	CBUF0/1 DATA2 PARITY ERR	CBUF0/1 DATA3 PARITY ERR	CBUF0/1 DATA4 PARITY ERR	CBUF0/1 DATA5 PARITY ERR	CBUF0/1 DATA6 PARITY ERR	CBUF0/1 DATA7 PARITY ERR
78	DRR::TRMDA							
	CMD A SYND CHK	(RSV)	CMD A MRCF Function	CMD A Double WT	CMD A Transfer Command			
79	DRR::TRMDA							
	LA0(LBA) COMP CHK ENABLE	LA1 COMP CHK ENABLE	LA2 COMP CHK ENABLE	(RSV)	EXLA COUNT UP STOP	(RSV)	(RSV)	(RSV)
7A	DRR::ADR0A							
	CMD A Slave 1 Cache Transfer Address (BYTE0)							
7B	DRR::ADR0A							
	CMD A Slave 2 Cache Transfer Address (BYTE0)							
7C	DRR::TRMDB							
	CMD B SYND CHK	(RSV)	CMD B MRCF Function	CMD B Double WT	CMD B Transfer Command			
7D	DRR::TRMDB							
	LA0(LBA) COMP CHK ENABLE	LA1 COMP CHK ENABLE	LA2 COMP CHK ENABLE	(RSV)	EXLA COUNT UP STOP	(RSV)	(RSV)	(RSV)
7E	DRR::ADR0B							
	CMD B Slave 1 Cache Transfer Address (BYTE0)							
7F	DRR::ADR0B							
	CMD B Slave 2 Cache Transfer Address (BYTE0)							

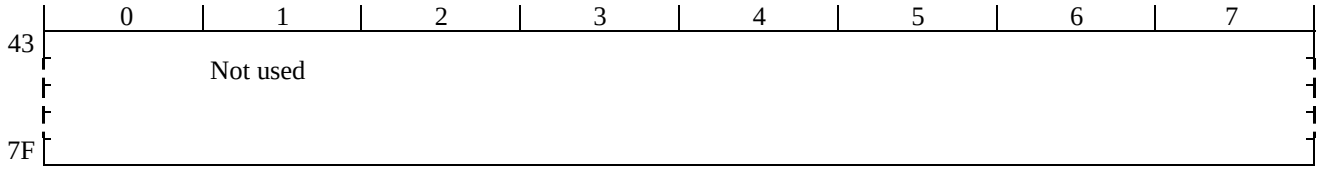
Copyright ©2000, Hitachi, Ltd.

Byte27 = F6 (CFW Access not Authorized) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘F’)				Message (x‘6’)			
28	Reason code (x‘01’ : CFW ID unmatch)							
29	Not used							
2A								
2B								
2C								
2D	SSID of mate subsystem (x‘0000’ for EDCC)							
2E								
2F	Maker code & Manufacture code (x‘00’)							
30	Not used							
31	Module ID							
32	Routine ID							
33	PCB number				Not used			
34	SSID of self subsystem							
35								
36	Symptom code (x‘FFF6’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not usde (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = F6 (CFW Access not Authorized) (2/2)



Copyright ©2000, Hitachi, Ltd.

Byte27 = FA (NVS Terminated) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘F’)				Message (x‘A’)			
28	Reason code (x‘02’ : NVS failure)							
29	Not used							
2A								
2B								
2C								
2D	SSID of mate subsystem (x‘0000’ for EDCC)							
2E								
2F	Mader code & Manufacture code (x‘00’)							
30	Not used							
31	Module ID							
32	Routine ID							
33	PCB number				Error code (x‘F’)			
34	SSID of self subsystem							
35								
36	Symptom code (x‘FFFA’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not usde (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte27 = FA (NVS Terminated) (2/2)

	0	1	2	3	4	5	6	7
40	Key cede (for reconnection)							
41	Format/Message (for reconnection)							
42	Module ID (for reconnection)							
43	Routine ID(for reconnection)							
44	Not used							
7F								

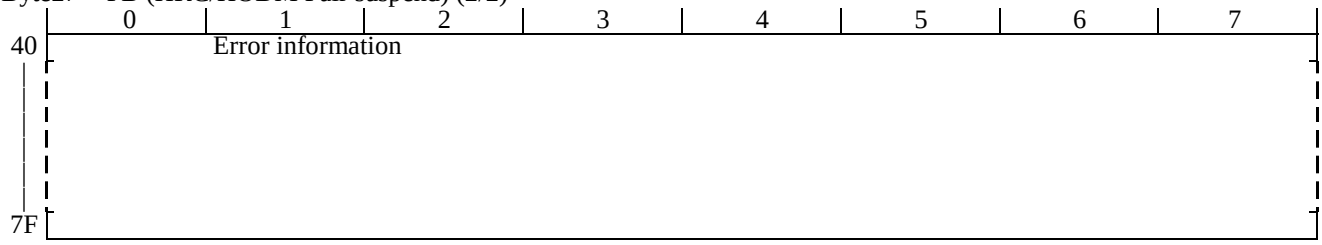
Copyright ©2000, Hitachi, Ltd.

Byte27 = FB (HRC/HODM Pair suspend) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low order)							
26	Cylinder address (high order)				Head address			
27	Format (x‘F’)				Message (x‘B’)			
28	R-Vol Suspended	R-Vol failed	Reason code(Note)					
29	RCU device address							
2A	RCU Manufacture code/Factory code							
2B								
2C								
2D	RCU Sequence No.							
2E								
2F	MCU Manufacture code/Factory code							
30								
31								
32	MCU Sequence No.							
33								
34	SSID of self subsystem							
35								
36	Sympton code (x‘FE’)							
37	Sympton code (same byte #28)							
38	Not used (x‘00’)							
39	Not used (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Not used (x‘00’)							
3E	Reference code(x‘FFFB’)							
3F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = FB (HRC/HODM Pair suspend) (2/2)



(Note) Reason code

x‘14’-x‘2F’	: Reserved
x‘30’	: Pair suspended. MCU device write error.
x‘31’	: Pair suspended. RCU subsystem error/or MCU subsystem error.
x‘32’	: Pair suspended. RCU device communication error.
x‘33’	: Pair suspended (Critical device status). All write command is rejected until pair re-established.
x‘34’	: Pair suspended. RCU device is not ready (intervention required).

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB (x‘35’)							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘F’)				Message (x‘F’)			
28	Subcode (See following pages)							
29	Hardware information (See following pages)							
30								
31	Module ID							
32	Routine ID							
33	PCB number				Message code (x‘0’)			
34	SSID of self subsystem							
35								
36	Symptom code (x‘FFFF’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Sylinder address							
3E								
3F	Head address							
40	Hardware information (See following pages)							
7F								

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(1) Byte28 = 02 : Cache 1 symbol error

	0	1	2	3	4	5	6	7
28	Subcode : x‘02’ : Cache 1 symbol error							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30								

40 | 7F	Common information (See “Type 1”)

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(2) Byte28 = 04 : Shared memory 1 symbol error

	0	1	2	3	4	5	6	7
28	Subcode : x‘04’ : Shared memory 1 symbol error							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Slot number of shared memory (Side A:x‘00’, Side B:x‘01’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							

40 | 7F	Common information (See “Type 2”)

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(3) Byte28 = 08/09 :Three SM DISABLE lines inconsistent

	0	1	2	3	4	5	6	7
28	Subcode : x‘08’ : Three SM (A) DISABLE lines inconsistent x‘09’ : Three SM (B) DISABLE lines inconsistent							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Threshold counter for the warning							
2C	MPA::HOUT							
	SMDA(0-2) signal all	SMDA0 signal	SMDA1 signal	SMDA2 signal	SMDB(0-2) signal all	SMDB0 signal	SMDB1 signal	SMDB2 signal
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	MPA::HIN							
	SMDA(0-2) MV	SMDA0 status	SMDA1 status	SMDA2 status	SMDB(0-2) MV	SMDB0 status	SMDB1 status	SMDB2 status

40 | 7F	Common information (See “Type 3”)

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(4) Byte28 = 10 : SMA slave error

	0	1	2	3	4	5	6	7
28	Subcode : x‘10’ : SMA slave error							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Slot number of shared memory							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Scan slave MPID							

40 | 7F	Common information (See “Type 4”)

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(5) Byte28 = 11 : MPA slave error

	0	1	2	3	4	5	6	7
28	Subcode : x‘11’ : MPA slave error							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Transfer SMA (2:Side A, 1:Side B)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	PKID (Reported SSB)							

40 | 7F	Common information (See “Type 5”)

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(6) Byte28 = 12 : SMA SCINT error

	0	1	2	3	4	5	6	7
28	Subcode : x‘12’ : SMA SCINT error							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Slot number of shared memory							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	MPID (Reported SSB)							

40 | 7F	Common information (See “Type 9”)

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(7) Byte28 = 13 : SMA BCINT error

	0	1	2	3	4	5	6	7
28	Subcode : x‘13’ : SMA BCINT error							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Slot number of shared memory							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	MPID (Reported SSB)							

40 | 7F	Common information (See “Type 10”)

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(8) Byte28 = 20 : FSW LED BUS test error

	0	1	2	3	4	5	6	7
28	Subcode : x‘20’ : FSW LED BUS test error							
29	MPID (Reported SSB)							
2A	FCA::LEDADRDT							
	Address of LED BUS							
2B	FCA::LEDADRDT							
	Data of LED BUS							
2C	FCA::LEDCMD							
	Not used	Not used	Not used	Not used	Not used	Not used	LED BUS RD CMD	LED BUS WR CMD
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	FCA::LEDSTAT							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used

40 | 7F	Common information (See “Type 6”)

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(9) Byte28 = 40 : Abnormal DC CTL warning

	0	1	2	3	4	5	6	7
28	Subcode : x‘40’ : Abnormal DC CTL warning							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							

40 | 7F	Common information (See “Type 7”)

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(10) Byte28 = 41 : Abnormal CEMODE warning

	0	1	2	3	4	5	6	7
28	Subcode : x‘41’ : Abnormal CEMODE warning							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							

40 | 7F	Common information (See “Type 7”)

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(11) Byte28 = B0 : CARB error : Warning

	0	1	2	3	4	5	6	7
28	Subcode : x‘B0’ : CARB error : Warning							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Used P-PATH No. (00 : P-PATH0, 01 : P-PATH1)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							

40 | 7F	Common information (See “Type 8”)

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type1 (1/4)

	0	1	2	3	4	5	6	7
40	Threshold counter for cache memory 1 symbol error							
	Module group #0 - H							
41	Threshold counter for cache memory 1 symbol error							
	Module group #0 - L							
42	Threshold counter for cache memory 1 symbol error							
	Module group #1 - H							
43	Threshold counter for cache memory 1 symbol error							
	Module group #1 - L							
44	Threshold counter for cache memory 1 symbol error							
	Module group #2 - H							
45	Threshold counter for cache memory 1 symbol error							
	Module group #2 - L							
46	Threshold counter for cache memory 1 symbol error							
	Module group #3 - H							
47	Threshold counter for cache memory 1 symbol error							
	Module group #3 - L							
48	Threshold counter for cache memory 1 symbol error							
	Module group #4 - H							
49	Threshold counter for cache memory 1 symbol error							
	Module group #4 - L							
4A	Threshold counter for cache memory 1 symbol error							
	Module group #5 - H							
4B	Threshold counter for cache memory 1 symbol error							
	Module group #5 - L							
4C	Threshold counter for cache memory 1 symbol error							
	Module group #6 - H							
4D	Threshold counter for cache memory 1 symbol error							
	Module group #6 - L							
4E	Threshold counter for cache memory 1 symbol error							
	Module group #7 - H							
4F	Threshold counter for cache memory 1 symbol error							
	Module group#7 - L							

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type1 (2/4)

	0	1	2	3	4	5	6	7
50	Threshold counter for cache memory 1 symbol error							
	Module group #8 - H							
51	Threshold counter for cache memory 1 symbol error							
	Module group #8 - L							
52	Threshold counter for cache memory 1 symbol error							
	Module group #9 - H							
53	Threshold counter for cache memory 1 symbol error							
	Module group #9 - L							
54	Threshold counter for cache memory 1 symbol error							
	Module group #10 - H							
55	Threshold counter for cache memory 1 symbol error							
	Module group #10 - L							
56	Threshold counter for cache memory 1 symbol error							
	Module group #11 - H							
57	Threshold counter for cache memory 1 symbol error							
	Module group #11 - L							
58	Threshold counter for cache memory 1 symbol error							
	Module group #12 - H							
59	Threshold counter for cache memory 1 symbol error							
	Module group #12 - L							
5A	Threshold counter for cache memory 1 symbol error							
	Module group #13 - H							
5B	Threshold counter for cache memory 1 symbol error							
	Module group #13 - L							
5C	Threshold counter for cache memory 1 symbol error							
	Module group #14 - H							
5D	Threshold counter for cache memory 1 symbol error							
	Module group #14 - L							
5E	Threshold counter for cache memory 1 symbol error							
	Module group #15 - H							
5F	Threshold counter for cache memory 1 symbol error							
	Module group#15 - L							

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type1 (3/4)

	0	1	2	3	4	5	6	7
60	CMA::WARNING							
	MG#00 1 symbol error	MG#01 1 symbol error	MG#02 1 symbol error	MG#03 1 symbol error	MG#04 1 symbol error	MG#05 1 symbol error	MG#06 1 symbol error	MG#07 1 symbol error
61	CMA::WARNING							
	MG#08 1 symbol error	MG#09 1 symbol error	MG#10 1 symbol error	MG#11 1 symbol error	MG#12 1 symbol error	MG#13 1 symbol error	MG#14 1 symbol error	MG#15 1 symbol error
62	CMA::MGxxHERRSTAT0							
	byte11 High order 4 bits warning	byte11 Low order 4 bits warning	Not used	Not used	Not used	Not used	Not used	Not used
63	CMA::MGxxHERRSTAT0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
64	CMA::MGxxHERRSTAT0							
	byte0F High order 4 bits warning	byte0F Low order 4 bits warning	byte0E High order 4 bits warning	byte0E Low order 4 bits warning	byte0D High order 4 bits warning	byte0D Low order 4 bits warning	byte0C High order 4 bits warning	byte0C Low order 4 bits warning
65	CMA::MGxxHERRSTAT0							
	byte0B High order 4 bits warning	byte0B Low order 4 bits warning	byte0A High order 4 bits warning	byte0A Low order 4 bits warning	byte09 High order 4 bits warning	byte09 Low order 4 bits warning	byte08 High order 4 bits warning	byte08 Low order 4 bits warning
66	CMA::MGxxLERRSTAT0							
	byte10 High order 4 bits warning	byte10 Low order 4 bits warning	Not used	Not used	Not used	Not used	Not used	Not used
67	CMA::MGxxLERRSTAT0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
68	CMA::MGxxLERRSTAT0							
	byte07 High order 4 bits warning	byte07 Low order 4 bits warning	byte06 High order 4 bits warning	byte06 Low order 4 bits warning	byte05 High order 4 bits warning	byte05 Low order 4 bits warning	byte04 High order 4 bits warning	byte04 Low order 4 bits warning
69	CMA::MGxxLERRSTAT0							
	byte03 High order 4 bits warning	byte03 Low order 4 bits warning	byte02 High order 4 bits warning	byte02 Low order 4 bits warning	byte01 High order 4 bits warning	byte01 Low order 4 bits warning	byte00 High order 4 bits warning	byte00 Low order 4 bits warning
6A	Not used							
6B	Not used							
6C	Not used							
6D	Not used							
6E	Not used							
6F	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type1 (4/4)

	0	1	2	3	4	5	6	7
70	Cache module number							
71	Cache PCB number							
72	Not used							
73	Not used							
74	Not used							
75	Not used							
76	Not used							
77	Not used							
78	Not used							
79	Not used							
7A	Not used							
7B	Not used							
7C	Not used							
7D	Not used							
7E	Not used							
7F	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type2 (1/4)

	0	1	2	3	4	5	6	7
40	Threshold counter for shared memory 1 symbol error							
	SMA-DIMM00							
41	Threshold counter for shared memory 1 symbol error							
	SMA-DIMM01							
42	Threshold counter for shared memory 1 symbol error							
	SMA-DIMM02							
43	Threshold counter for shared memory 1 symbol error							
	SMA-DIMM03							
44	Threshold counter for shared memory 1 symbol error							
	SMA-DIMM04							
45	Threshold counter for shared memory 1 symbol error							
	SMA-DIMM05							
46	Not used							
47	Not used							
48	Not used							
49	SMA::DIMM SIGNAL ERROR DIMM							
	DIMM00 control error	DIMM01 control error	DIMM02 control error	DIMM03 control error	DIMM04 control error	DIMM05 control error	Not used control error	Not used control error
4A	SMA::UNCOR ERROR DIMM							
	DIMM00 uncorrectable error	DIMM01 uncorrectable error	DIMM02 uncorrectable error	DIMM03 uncorrectable error	DIMM04 uncorrectable error	DIMM05 uncorrectable error	Not used	Not used
4B	SMA::COR ERROR DIMM							
	DIMM00 correctable error	DIMM01 correctable error	DIMM02 correctable error	DIMM03 correctable error	DIMM04 correctable error	DIMM05 correctable error	Not used	Not used
4C	SMA::COR ERROR DIMM00 LOCATION							
	Correctable error in memory element 0 (for data)	Correctable error in memory element 1 (for data)	Correctable error in memory element 2 (for data)	Correctable error in memory element 3 (for data)	Correctable error in memory element 4 (for data)	Correctable error in memory element 5 (for data)	Correctable error in memory element 6 (for data)	Correctable error in memory element 7 (for data)
4D	SMA::COR ERROR DIMM00 LOCATION							
	Correctable error in memory element 8 (for data)	Correctable error in memory element 9 (for data)	Correctable error in memory element 10 (for data)	Not used	Not used	Not used	Not used	Not used
4E	SMA::COR ERROR DIMM01 LOCATION							
	Correctable error in memory element 0 (for data)	Correctable error in memory element 1 (for data)	Correctable error in memory element 2 (for data)	Correctable error in memory element 3 (for data)	Correctable error in memory element 4 (for data)	Correctable error in memory element 5 (for data)	Correctable error in memory element 6 (for data)	Correctable error in memory element 7 (for data)
4F	SMA::COR ERROR DIMM01 LOCATION							
	Correctable error in memory element 8 (for data)	Correctable error in memory element 9 (for data)	Correctable error in memory element 10 (for data)	Not used	Not used	Not used	Not used	Not used

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type2 (2/4)

	0	1	2	3	4	5	6	7
50	SMA::COR ERROR DIMM02 LOCATION							
	Correctable error in memory element 0 (for data)	Correctable error in memory element 1 (for data)	Correctable error in memory element 2 (for data)	Correctable error in memory element 3 (for data)	Correctable error in memory element 4 (for data)	Correctable error in memory element 5 (for data)	Correctable error in memory element 6 (for data)	Correctable error in memory element 7 (for data)
51	SMA::COR ERROR DIMM02 LOCATION							
	Correctable error in memory element 8 (for data)	Correctable error in memory element 9 (for data)	Correctable error in memory element 10 (for data)	Not used	Not used	Not used	Not used	Not used
52	SMA::COR ERROR DIMM03 LOCATION							
	Correctable error in memory element 0 (for data)	Correctable error in memory element 1 (for data)	Correctable error in memory element 2 (for data)	Correctable error in memory element 3 (for data)	Correctable error in memory element 4 (for data)	Correctable error in memory element 5 (for data)	Correctable error in memory element 6 (for data)	Correctable error in memory element 7 (for data)
53	SMA::COR ERROR DIMM03 LOCATION							
	Correctable error in memory element 8 (for data)	Correctable error in memory element 9 (for data)	Correctable error in memory element 10 (for data)	Not used	Not used	Not used	Not used	Not used
54	SMA::COR ERROR DIMM04 LOCATION							
	Correctable error in memory element 0 (for data)	Correctable error in memory element 1 (for data)	Correctable error in memory element 2 (for data)	Correctable error in memory element 3 (for data)	Correctable error in memory element 4 (for data)	Correctable error in memory element 5 (for data)	Correctable error in memory element 6 (for data)	Correctable error in memory element 7 (for data)
55	SMA::COR ERROR DIMM04 LOCATION							
	Correctable error in memory element 8 (for data)	Correctable error in memory element 9 (for data)	Correctable error in memory element 10 (for data)	Not used	Not used	Not used	Not used	Not used
56	SMA::COR ERROR DIMM05 LOCATION							
	Correctable error in memory element 0 (for data)	Correctable error in memory element 1 (for data)	Correctable error in memory element 2 (for data)	Correctable error in memory element 3 (for data)	Correctable error in memory element 4 (for data)	Correctable error in memory element 5 (for data)	Correctable error in memory element 6 (for data)	Correctable error in memory element 7 (for data)
57	SMA::COR ERROR DIMM05 LOCATION							
	Correctable error in memory element 8 (for data)	Correctable error in memory element 9 (for data)	Correctable error in memory element 10 (for data)	Not used	Not used	Not used	Not used	Not used
58	Not used							
59	SMA::PATH0 ERROR STATUS							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLECAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
5A	SMA::PATH0 ERROR STATUS							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
5B	SMA::PATH0 ERROR STATUS							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	Not used	Not used	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
5C	SMA::PATH0 ERROR DETAIL							
	RX CMD PARITY ERROR	RX ADR PARITY ERROR	RX WDT PARITY ERROR	Not used	SYNC0 UNDER ERROR	SYNC1 UNDER ERROR	SYNC0 OVER ERROR	SYNC1 OVER ERROR
5D	SMA::PATH0 ERROR DETAIL							
	LRC ERROR	LRC COMPERE ERROR	LOCK COMMAND ERROR	R/W COMMAND ERROR	ILLEGAL LOCK DBL ERROR	DOUBLE LOCK ERROR	LOCK ACCESS OVER(ENT)	Not used
5E	SMA::PATH0 ERROR DETAIL							
	CMD PGEN ERROR	ADR PGEN ERROR	WDT PGEN ERROR	PCB PARITY ERROR	PAB PARITY ERROR	PWB PARITY ERROR	PCB LOCK COMMAND ERROR	PCB R/W COMMAND ERROR
5F	SMA::PATH0 ERROR DETAIL							
	Not used	Not used	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	Not used	PATH SEQUENCE R ERROR	REQ COUNTER PARITY ERROR	LOCK COUNTER PATH ERROR

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type2 (3/4)

	0	1	2	3	4	5	6	7
60	Not used							
61	SMA::PATH1 ERROR STATUS							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
62	SMA::PATH1 ERROR STATUS							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
63	SMA::PATH1 ERROR STATUS							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	Not used	Not used	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
64	SMA::PATH1 ERROR DETAIL							
	RX CMD PARITY ERROR	RX ADR PARITY ERROR	RX WDT PARITY ERROR	Not used	SYNC0 UNDER ERROR	SYNC1 UNDER ERROR	SYNC0 OVER ERROR	SYNC1 OVER ERROR
65	SMA::PATH1 ERROR DETAIL							
	LRC ERROR	LRC COMPERE ERROR	LOCK COMMAND ERROR	R/W COMMAND ERROR	ILLEGAL LOCK DBL ERROR	DOUBLE LOCK ERROR	LOCK ACCESS OVER(ENT)	Not used
66	SMA::PATH1 ERROR DETAIL							
	CMD PGEN ERROR	ADR PGEN ERROR	WDT PGEN ERROR	PCB PARITY ERROR	PAB PARITY ERROR	PWB PARITY ERROR	PCB LOCK COMMAND ERROR	PCB R/W COMMAND ERROR
67	SMA::PATH1 ERROR DETAIL							
	Not used	Not used	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	Not used	PATH SEQUENCE R ERROR	REQ COUNTER PARITY ERROR	LOCK COUNTER PATH ERROR
68	SMA::BOARD ERROR STATUS							
	MCB PARITY ERROR	MAB PARITY ERROR	MWB PARITY ERROR	SIMMSEL PARITY ERROR	MEMPATHA DR PARITY ERROR	RDTLT NOTHING ERROR	ICB PARITY ERROR	IAB PARITY ERROR
69	SMA::BOARD ERROR STATUS							
	IWB PARYTY ERROR	I/O PATHADR PARITY ERROR	PDADR OUTPUT ERROR	LOCK ADR PARITY ERROR	LOCK WAIT TIMEOUT	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	SLOT PARITY ERROR
6A	SMA::BOARD ERROR STATUS							
	CLOCK ERROR	REFRESH ERROR	TIMER PARITY ERROR	ARBITER ERROR	WT WEQ PARITY ERROR	RD SEQ PARITY ERROR	MEM SEQ PARITY ERROR	I/O SEQ PARITY ERROR
6B	SMA::BOARD ERROR STATUS							
	ECC GENERATE ERROR	SMDT OUTPUT ERROR	BSSWEN OUTPUT ERROR	VALID CNT PARITY ERROR	SCAN CNT PARITY ERROR	SCAn SEQ ERROR	BCINT OUTPUT ERROR	SCINT OUTPUT ERROR
6C	Not used							
6D	Not used							
6E	SMA::BOARD ERROR DETAIL							
	Not used	Not used	Not used	Not used	Not used	MEMORY ARBITER ERROR	LOCK ARBITER ERROR	I/O ARBITER ERROR
6F	SMA::BOARD ERROR DETAIL							
	Not used	CLOCK GENERATE ERROR	CLOCK CNT PARITY ERROR	CLOCK FREQUEN-CY ERROR	Not used	INITIAL CNT PARITY ERROR	REFRESH CNT PARITY ERROR	REFRESH PROTCOL ERROR

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type2 (4/4)

	0	1	2	3	4	5	6	7
70	Not used							
71	Not used							
72	SMA::SMA CONTROL							
	DBG SIG	Not used	Not used	Not used	Not used	BSSW CHK EN	ENT WAIT EN	ENTOFF RST EN
73	SMA::SMA CONTROL							
	SMPSDWN EN	CLK CHK EN	ECC ADR MSK	DIAG EN	DUMP MODE	PWR DWN EN	DT RVS INH	REF MODE
74	Not used							
75	SMA::SMA STATUS							
	Not used	Not used	Not used	Not used	SLOT (Side B)	SLOT (Side A)	DISC MODE	PWR DWN MODE
76	SMA::SMA STATUS							
	DISC REQ	SELF REF	SMPS DWN	PS DTCT	TIM EN	ALL LOCK	MEM PDY	SM EN
77	SMA::SMA STATUS							
	PK VER				LSI VER			
78	SMA::DIMM ENABLE							
	DIMM00 EN	DIMM01 EN	DIMM02 EN	DIMM03 EN	DIMM04 EN	DIMM05 EN	Not used	Not used
79	SMA::DIMM KIND							
	DIMM00 KIND 0:64MB 1:128mb	DIMM01 KIND 0:64MB 1:128MB	DIMM02 KIND 0:64MB 1:128MB	DIMM03 KIND 0:64MB 1:128MB	DIMM04 KIND 0:64MB 1:128MB	DIMM05 KIND 0:64MB 1:128MB	Not used	Not used
7A	SMA::DIMM CHECK ENABLE							
	DIMM00 CHKEN	DIMM01 CHKEN	DIMM02 CHKEN	DIMM03 CHKEN	DIMM04 CHKEN	DIMM05 CHKEN	Not used	Not used
7B	SMA::REWRITE INHIBIT							
	DIMM00 REW INH	DIMM01 REW INH	DIMM02 REW INH	DIMM03 REW INH	DIMM04 REW INH	DIMM05 REW INH	Not used	Not used
7C	Not used							
7D	Not used							
7E	Not used							
7F	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type3 (1/4)

	0	1	2	3	4	5	6	7
40	Threshold counter for the warning							
	MPID 0							
41	Threshold counter for the warning							
	MPID 1							
42	Threshold counter for the warning							
	MPID 2							
43	Threshold counter for the warning							
	MPID 3							
44	Threshold counter for the warning							
	MPID 4							
45	Threshold counter for the warning							
	MPID 5							
46	Threshold counter for the warning							
	MPID 6							
47	Threshold counter for the warning							
	MPID 7							
48	Threshold counter for the warning							
	MPID 8							
49	Threshold counter for the warning							
	MPID 9							
4A	Threshold counter for the warning							
	MPID 10							
4B	Threshold counter for the warning							
	MPID 11							
4C	Threshold counter for the warning							
	MPID 12							
4D	Threshold counter for the warning							
	MPID 13							
4E	Threshold counter for the warning							
	MPID 14							
4F	Threshold counter for the warning							
	MPID15							

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type3 (2/4)

	0	1	2	3	4	5	6	7
50	Threshold counter for the warning							
	MPID 16							
51	Threshold counter for the warning							
	MPID 17							
52	Threshold counter for the warning							
	MPID 18							
53	Threshold counter for the warning							
	MPID 19							
54	Threshold counter for the warning							
	MPID 20							
55	Threshold counter for the warning							
	MPID 21							
56	Threshold counter for the warning							
	MPID 22							
57	Threshold counter for the warning							
	MPID 23							
58	Threshold counter for the warning							
	MPID 24							
59	Threshold counter for the warning							
	MPID 25							
5A	Threshold counter for the warning							
	MPID 26							
5B	Threshold counter for the warning							
	MPID 27							
5C	Threshold counter for the warning							
	MPID 28							
5D	Threshold counter for the warning							
	MPID 29							
5E	Threshold counter for the warning							
	MPID 30							
5F	Threshold counter for the warning							
	MPID 31							

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type3 (3/4)

	0	1	2	3	4	5	6	7
60	Threshold counter for the warning							
	MPID 32							
61	Threshold counter for the warning							
	MPID 33							
62	Threshold counter for the warning							
	MPID 34							
63	Threshold counter for the warning							
	MPID 35							
64	Threshold counter for the warning							
	MPID 36							
65	Threshold counter for the warning							
	MPID 37							
66	Threshold counter for the warning							
	MPID 38							
67	Threshold counter for the warning							
	MPID 39							
68	Threshold counter for the warning							
	MPID 40							
69	Threshold counter for the warning							
	MPID 41							
6A	Threshold counter for the warning							
	MPID 42							
6B	Threshold counter for the warning							
	MPID 43							
6C	Threshold counter for the warning							
	MPID 44							
6D	Threshold counter for the warning							
	MPID 45							
6E	Threshold counter for the warning							
	MPID 46							
6F	Threshold counter for the warning							
	MPID 47							

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type3 (4/4)

	0	1	2	3	4	5	6	7
70	Threshold counter for the warning							
	MPID 48							
71	Threshold counter for the warning							
	MPID 49							
72	Threshold counter for the warning							
	MPID 50							
73	Threshold counter for the warning							
	MPID 51							
74	Threshold counter for the warning							
	MPID 52							
75	Threshold counter for the warning							
	MPID 53							
76	Threshold counter for the warning							
	MPID 54							
77	Threshold counter for the warning							
	MPID 55							
78	Threshold counter for the warning							
	MPID 56							
79	Threshold counter for the warning							
	MPID 57							
7A	Threshold counter for the warning							
	MPID 58							
7B	Threshold counter for the warning							
	MPID 59							
7C	Threshold counter for the warning							
	MPID 60							
7D	Threshold counter for the warning							
	MPID 61							
7E	Threshold counter for the warning							
	MPID 62							
7F	Threshold counter for the warning							
	MPID 63							

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type4 (1/4)

	0	1	2	3	4	5	6	7
40	Scan type							
	04 : MP status read 02 : Scan read 01 : Scan write							
41	Not used							
42	Threshold counter for the scan group							
	Scan path group A							
43	Threshold counter for the scan group							
	Scan path group B							
44	SMA::SCINT OUTPUT MASK							
	SC_MASK MPA#0	SC_MASK MPA#1	SC_MASK MPA#2	SC_MASK MPA#3	SC_MASK MPA#4	SC_MASK MPA#5	SC_MASK MPA#6	SC_MASK MPA#7
45	SMA::SCINT OUTPUT MASK							
	SC_MASK MPA#8	SC_MASK MPA#9	SC_MASK MPA#A	SC_MASK MPA#B	SC_MASK MPA#C	SC_MASK MPA#D	SC_MASK MPA#E	SC_MASK MPA#F
46	SMA::MP STATUS TIMEOUT DATA							
	MPST_TODT							
47	SMA::MP STATUS TIMEOUT DATA							
	MPST_TODT							
48	SMA::VALID TIMER TIMEOUT DATA							
	VAL_TODT							
49	SMA::VALID TIMER TIMEOUT DATA							
	VAL_TODT							
4A	SMA::SCINT TIMEOUT DATA							
	SC_TODT							
4B	SMA::SCINT TIMEOUT DATA							
	SC_TODT							
4C	SMA::SCAN COUNTER PARITY ERROR							
	SCCNT_PERR MPA#0	SCCNT_PERR MPA#1	SCCNT_PERR MPA#2	SCCNT_PERR MPA#3	SCCNT_PERR MPA#4	SCCNT_PERR MPA#5	SCCNT_PERR MPA#6	SCCNT_PERR MPA#7
4D	SMA::SCAN COUNTER PARITY ERROR							
	SCCNT_PERR MPA#8	SCCNT_PERR MPA#9	SCCNT_PERR MPA#A	SCCNT_PERR MPA#B	SCCNT_PERR MPA#C	SCCNT_PERR MPA#D	SCCNT_PERR MPA#E	SCCNT_PERR MPA#F
4E	SMA::VALID COUNTER PARITY ERROR							
	VALCNT_PERR MPA#0	VALCNT_PERR MPA#1	VALCNT_PERR MPA#2	VALCNT_PERR MPA#3	VALCNT_PERR MPA#4	VALCNT_PERR MPA#5	VALCNT_PERR MPA#6	VALCNT_PERR MPA#7
4F	SMA::VALID COUNTER PARITY ERROR							
	VALCNT_PERR MPA#8	VALCNT_PERR MPA#9	VALCNT_PERR MPA#A	VALCNT_PERR MPA#B	VALCNT_PERR MPA#C	VALCNT_PERR MPA#D	VALCNT_PERR MPA#E	VALCNT_PERR MPA#F

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type4 (2/4)

	0	1	2	3	4	5	6	7
50	SMA::SCAN SEQUENCER ERROR							
	SCSEQ_ERR MPA#0	SCSEQ_ERR MPA#1	SCSEQ_ERR MPA#2	SCSEQ_ERR MPA#3	SCSEQ_ERR MPA#4	SCSEQ_ERR MPA#5	SCSEQ_ERR MPA#6	SCSEQ_ERR MPA#7
51	SMA::SCAN SEQUENCER ERROR							
	SCSEQ_ERR MPA#8	SCSEQ_ERR MPA#9	SCSEQ_ERR MPA#A	SCSEQ_ERR MPA#B	SCSEQ_ERR MPA#C	SCSEQ_ERR MPA#D	SCSEQ_ERR MPA#E	SCSEQ_ERR MPA#F
52	SMA::SCINT OUT ERROR							
	SINT_OUT_ ERR MPA#0	SINT_OUT_ ERR MPA#1	SINT_OUT_ ERR MPA#2	SINT_OUT_ ERR MPA#3	SINT_OUT_ ERR MPA#4	SINT_OUT_ ERR MPA#5	SINT_OUT_ ERR MPA#6	SINT_OUT_ ERR MPA#7
53	SMA::SCINT OUT ERROR							
	SINT_OUT_ ERR MPA#8	SINT_OUT_ ERR MPA#9	SINT_OUT_ ERR MPA#A	SINT_OUT_ ERR MPA#B	SINT_OUT_ ERR MPA#C	SINT_OUT_ ERR MPA#D	SINT_OUT_ ERR MPA#E	SINT_OUT_ ERR MPA#F
54	SMA::SCINT SIGNAL							
	SINT_SIG MPA#0	SINT_SIG MPA#1	SINT_SIG MPA#2	SINT_SIG MPA#3	SINT_SIG MPA#4	SINT_SIG MPA#5	SINT_SIG MPA#6	SINT_SIG MPA#7
55	SMA::SCINT SIGNAL							
	SINT_SIG MPA#8	SINT_SIG MPA#9	SINT_SIG MPA#A	SINT_SIG MPA#B	SINT_SIG MPA#C	SINT_SIG MPA#D	SINT_SIG MPA#E	SINT_SIG MPA#F
56	Not used							
57	Not used							
58	Not used							
59	SMA::PATH0 ERROR STATUS							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
5A	SMA::PATH0 ERROR STATUS							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
5B	SMA::PATH0 ERROR STATUS							
	CORRECTA-BLE ERROR	UNCORREC -TABLE ERROR	I/O REG PARITY ERROR	Not used	Not used	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
5C	SMA::PATH0 ERROR DETAIL							
	RX CMD PARITY ERROR	RX ADR PARITY ERROR	RX WDT PARITY ERROR	Not used	SYNC0 UNDER ERROR	SYNC1 UNDER ERROR	SYNC0 OVER ERROR	SYNC1 OVER ERROR
5D	SMA::PATH0 ERROR DETAIL							
	LRC ERROR	LRC COMPERE ERROR	LOCK COMMAND ERROR	R/W COMMAND ERROR	ILLEGAL LOCK DBL ERROR	DOUBLE LOCK ERROR	LOCK ACCESS OVER(ENT)	Not used
5E	SMA::PATH0 ERROR DETAIL							
	CMD PGEN ERROR	ADR PGEN ERROR	WDT PGEN ERROR	PCB PARITY ERROR	PAB PARITY ERROR	PWB PARITY ERROR	PCB LOCK COMMAND ERROR	PCB R/W COMMAND ERROR
5F	SMA::PATH0 ERROR DETAIL							
	Not used	Not used	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	Not used	PATH SEQUENCE R ERROR	REQ COUNTER PARITY ERROR	LOCK COUNTER PATH ERROR

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type4 (3/4)

	0	1	2	3	4	5	6	7
60	Not used							
61	SMA::PATH1 ERROR STATUS							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
62	SMA::PATH1 ERROR STATUS							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
63	SMA::PATH1 ERROR STATUS							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	Not used	Not used	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
64	SMA::PATH1 ERROR DETAIL							
	RX CMD PARITY ERROR	RX ADR PARITY ERROR	RX WDT PARITY ERROR	Not used	SYNC0 UNDER ERROR	SYNC1 UNDER ERROR	SYNC0 OVER ERROR	SYNC1 OVER ERROR
65	SMA::PATH1 ERROR DETAIL							
	LRC ERROR	LRC COMPERE ERROR	LOCK COMMAND ERROR	R/W COMMAND ERROR	ILLEGAL LOCK DBL ERROR	DOUBLE LOCK ERROR	LOCK ACCESS OVER(ENT)	Not used
66	SMA::PATH1 ERROR DETAIL							
	CMD PGEN ERROR	ADR PGEN ERROR	WDT PGEN ERROR	PCB PARITY ERROR	PAB PARITY ERROR	PWB PARITY ERROR	PCB LOCK COMMAND ERROR	PCB R/W COMMAND ERROR
67	SMA::PATH1 ERROR DETAIL							
	Not used	Not used	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	Not used	PATH SEQUENCE R ERROR	REQ COUNTER PARITY ERROR	LOCK COUNTER PATH ERROR
68	SMA::BOARD ERROR STATUS							
	MCB PARITY ERROR	MAB PARITY ERROR	MWB PARITY ERROR	SIMMSEL PARITY ERROR	MEMPATHA DR PARITY ERROR	RDTLT NOTHING ERROR	ICB PARITY ERROR	IAB PARITY ERROR
69	SMA::BOARD ERROR STATUS							
	IWB PARYTY ERROR	I/O PATHADR PARITY ERROR	PDADR OUTPUT ERROR	LOCK ADR PARITY ERROR	LOCK WAIT TIMEOUT	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	SLOT PARITY ERROR
6A	SMA::BOARD ERROR STATUS							
	CLOCK ERROR	REFRESH ERROR	TIMER PARITY ERROR	ARBITER ERROR	WT WEQ PARITY ERROR	RD SEQ PARITY ERROR	MEM SEQ PARITY ERROR	I/O SEQ PARITY ERROR
6B	SMA::BOARD ERROR STATUS							
	ECC GENERATE ERROR	SMDT OUTPUT ERROR	BSSWEN OUTPUT ERROR	VALID CNT PARITY ERROR	SCAN CNT PARITY ERROR	SCAn SEQ ERROR	BCINT OUTPUT ERROR	SCINT OUTPUT ERROR
6C	Not used							
6D	Not used							
6E	SMA::BOARD ERROR DETAIL							
	Not used	Not used	Not used	Not used	Not used	MEMORY ARBITER ERROR	LOCK ARBITER ERROR	I/O ARBITER ERROR
6F	SMA::BOARD ERROR DETAIL							
	Not used	CLOCK GENERATE ERROR	CLOCK CNT PARITY ERROR	CLOCK FREQUEN-CY ERROR	Not used	INITIAL CNT PARITY ERROR	REFRESH CNT PARITY ERROR	REFRESH PROTCOL ERROR

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type4 (4/4)

	0	1	2	3	4	5	6	7
70	Not used							
71	Not used							
72	SMA::SMA CONTROL							
	DBG SIG	Not used	Not used	Not used	Not used	BSSW CHK EN	ENT WAIT EN	ENTOFF RST EN
73	SMA::SMA CONTROL							
	SMPSDWN EN	CLK CHK EN	ECC ADR MSK	DIAG EN	DUMP MODE	PWR DWN EN	DT RVS INH	REF MODE
74	Not used							
75	SMA::SMA STATUS							
	Not used	Not used	Not used	Not used	SLOT (Side B)	SLOT (Side A)	DISC MODE	PWR DWN MODE
76	SMA::SMA STATUS							
	DISC REQ	SELF REF	SMPS DWN	PS DTCT	TIM EN	ALL LOCK	MEM PDY	SM EN
77	SMA::SMA STATUS							
	PK VER				LSI VER			
78	MPA::RXAEDT							
	MPST INT	MPST STATUS FLAG	MPST VALID	MPST TIMEOUT	SCAN INT	SCAN READDATA FLAG	SCAN STATUS FLAG	SCAN TIMEOUT
79	MPA::RXAEDT							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
7A	MPA::RXAEDT							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
7B	MPA::RXAEDT							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	Not used	Not used	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
7C	MPA::RXBEDT							
	MPST INT	MPST STATUS FLAG	MPST VALID	MPST TIMEOUT	SCAN INT	SCAN READDATA FLAG	SCAN STATUS FLAG	SCAN TIMEOUT
7D	MPA::RXBEDT							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
7E	MPA::RXBEDT							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
7F	MPA::RXBEDT							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	0	0	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type5 (1/4)

	0	1	2	3	4	5	6	7
40	MPA::MPASTS							
	MPA INT	CHK3 MST	CHK3 SLV	0	0	CHK1B COM	CHK1B XR	MPINT
41	Not used							
42	Not used							
43	Not used							
44	MPA::SLVCHK3STS							
	SCANIF#0 ERR	SCANIF#1 ERR	SCANIF#2 ERR	SCANIF#3 ERR	0	0	CHK3 SLV A	CHK3 SLV B
45	Not used							
46	Not used							
47	Not used							
48	Not used							
49	Not used							
4A	Not used							
4B	Not used							
4C	Not used							
4D	Not used							
4E	Not used							
4F	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type5 (2/4)

	0	1	2	3	4	5	6	7
50	MPA::SCANIF0 ADRER							
	0	0	0	SCAN_ ACSERR	0	0	PERR2	PERR3
51	MPA::SCANIF0 CNTER							
	0	0	0	0	0	0	0	PERR
52	MPA::SCANIF0 INER							
	0	0	0	0	PERR0	PERR1	PERR2	PERR3
53	MPA::SCANIF0 OUTER							
	0	0	0	0	PERR0	PERR1	PERR2	PERR3
54	MPA::SCANIF1 ADRER							
	0	0	0	SCAN_ ACSERR	0	0	PERR2	PERR3
55	MPA::SCANIF1 CNTER							
	0	0	0	0	0	0	0	PERR
56	MPA::SCANIF1 INER							
	0	0	0	0	PERR0	PERR1	PERR2	PERR3
57	MPA::SCANIF1 OUTER							
	0	0	0	0	PERR0	PERR1	PERR2	PERR3
58	MPA::SCANIF2 ADRER							
	0	0	0	SCAN_ ACSERR	0	0	PERR2	PERR3
59	MPA::SCANIF2 CNTER							
	0	0	0	0	0	0	0	PERR
5A	MPA::SCANIF2 INER							
	0	0	0	0	PERR0	PERR1	PERR2	PERR3
5B	MPA::SCANIF2 OUTER							
	0	0	0	0	PERR0	PERR1	PERR2	PERR3
5C	MPA::SCANIF3 ADRER							
	0	0	0	SCAN_ ACSERR	0	0	PERR2	PERR3
5D	MPA::SCANIF3 CNTER							
	0	0	0	0	0	0	0	PERR
5E	MPA::SCANIF3 INER							
	0	0	0	0	PERR0	PERR1	PERR2	PERR3
5F	MPA::SCANIF3 OUTER							
	0	0	0	0	PERR0	PERR1	PERR2	PERR3

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type5 (3/4)

	0	1	2	3	4	5	6	7
60	MPA::SLVA SCSQER							
	ILGLMD	TMOUT	TMPER	TMPER	TMPER	TMPER	SQPER1	SQPER0
61	Not used							
62	Not used							
63	Not used							
64	MPA::SLVB SCSQER							
	ILGLMD	TMOUT	TMPER	TMPER	TMPER	TMPER	SQPER1	SQPER0
65	Not used							
66	Not used							
67	Not used							
68	Not used							
69	Not used							
6A	Not used							
6B	Not used							
6C	Not used							
6D	Not used							
6E	Not used							
6F	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type5 (4/4)

	0	1	2	3	4	5	6	7
70	Not used							
71	Not used							
72	Not used							
73	Not used							
74	Not used							
75	Not used							
76	Not used							
77	Not used							
78	Not used							
79	Not used							
7A	Not used							
7B	Not used							
7C	Not used							
7D	Not used							
7E	Not used							
7F	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type6 (1/4)

	0	1	2	3	4	5	6	7
40	FCA::LEDSTAT							
	0	DKUSTAT	ACKERR	STSPERR	RDTPERR	DKUERR-OUT	RDBSY	WTBSY
41	FCA::LEDADRDT (After PK_STAT read)							
	Address of LED BUS							
42	FCA::LEDADRDT (After PK_STAT read)							
	Data of LED BUS							
43	FCA::LEDCMD (After PK_STAT read)							
	Not used	Not used	Not used	Not used	Not used	Not used	LED BUS RD CMD	LED BUS WR DMD
44	FCA::LEDSTAT (After PK_STAT read)							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
45	FCA::LEDSTAT (After PK_STAT read)							
	0	DKUSTAT	ACKERR	STSPERR	RDTPERR	DKUERR-OUT	RDBSY	WTBSY
46	FCA::LEDADRDT (After LBUS_ERR read)							
	Address of LED BUS							
47	FCA::LEDADRDT (After LBUS_ERR read)							
	Data of LED BUS							
48	FCA::LEDCMD (After LBUS_ERR read)							
	Not used	Not used	Not used	Not used	Not used	Not used	LED BUS RD CMD	LED BUS WR DMD
49	FCA::LEDSTAT (After LBUS_ERR read)							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4A	FCA::LEDSTAT (After LBUS_ERR read)							
	0	DKUSTAT	ACKERR	STSPERR	RDTPERR	DKUERR-OUT	RDBSY	WTBSY
4B	Not used							
4C	Not used							
4D	Not used							
4E	Not used							
4F	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type6 (2/4)

	0	1	2	3	4	5	6	7
50	Not used							
51	Not used							
52	Not used							
53	Not used							
54	Not used							
55	Not used							
56	Not used							
57	Not used							
58	Not used							
59	Not used							
5A	Not used							
5B	Not used							
5C	Not used							
5D	Not used							
5E	Not used							
5F	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type6 (3/4)

	0	1	2	3	4	5	6	7
60	Not used							
61	Not used							
62	Not used							
63	Not used							
64	Not used							
65	Not used							
66	Not used							
67	Not used							
68	Not used							
69	Not used							
6A	Not used							
6B	Not used							
6C	Not used							
6D	Not used							
6E	Not used							
6F	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type6 (4/4)

	0	1	2	3	4	5	6	7
70	Not used							
71	Not used							
72	Not used							
73	Not used							
74	Not used							
75	Not used							
76	Not used							
77	Not used							
78	Not used							
79	Not used							
7A	Not used							
7B	Not used							
7C	Not used							
7D	Not used							
7E	Not used							
7F	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type7 (1/4)

	0	1	2	3	4	5	6	7
40	Threshold counter for the warning							
	CHA-1P							
41	Threshold counter for the warning							
	CHA-1Q							
42	Threshold counter for the warning							
	CHA-1R							
43	Threshold counter for the warning							
	CHA-1S							
44	Threshold counter for the warning							
	DKA-1B							
45	Threshold counter for the warning							
	DKA-1C							
46	Threshold counter for the warning							
	DKA-1D							
47	Threshold counter for the warning							
	DKA-1E							
48	Threshold counter for the warning							
	CSW-1A							
49	Threshold counter for the warning							
	CSW-1N							
4A	Threshold counter for the warning							
	CACHE-1T							
4B	Threshold counter for the warning							
	CACHE-1U							
4C	Not used							
4D	Not used							
4E	Not used							
4F	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type7 (2/4)

	0	1	2	3	4	5	6	7
50	Threshold counter for the warning							
	CHA-2V							
51	Threshold counter for the warning							
	CHA-2W							
52	Threshold counter for the warning							
	CHA-2X							
53	Threshold counter for the warning							
	CHA-2Y							
54	Threshold counter for the warning							
	DKA-2H							
55	Threshold counter for the warning							
	DKA-2J							
56	Threshold counter for the warning							
	DKA-2K							
57	Threshold counter for the warning							
	DKA-2L							
58	Threshold counter for the warning							
	CSW-2M							
59	Threshold counter for the warning							
	CSW-2Z							
5A	Threshold counter for the warning							
	CACHE-2F							
5B	Threshold counter for the warning							
	CACHE-2G							
5C	Not used							
5D	Not used							
5E	Not used							
5F	Not used							

Copyright ©2000,2002, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type7 (3/4)

	0	1	2	3	4	5	6	7
60		CHA-1P						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
61		CHA-1Q						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
62		CHA-1R						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
63		CHA-1S						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
64		DKA-1B						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
65		DKA-1C						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
66		DKA-1D						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
67		DKA-1E						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
68		CSW-1A						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
69		CSW-1N						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
6A		CACHE-1T						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
6B		CACHE-1U						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
6C		Not used						
6D		Not used						
6E		Not used						
6F		Not used						

Copyright ©2000,2002, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type7 (4/4)

	0	1	2	3	4	5	6	7
70		CHA-2V						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
71		CHA-2W						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
72		CHA-2X						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
73		CHA-2Y						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
74		DKA-2H						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
75		DKA-2J						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
76		DKA-2K						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
77		DKA-2L						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
78		CSW-2M						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
79		CSW-2Z						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
7A		CACHE-2F						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
7B		CACHE-2G						
	CEMODE	0	DC CTL (1.5V + 10%)	DC CTL (1.5V -10%)	DC CTL (1.8V + 10%)	DC CTL (1.8V -10%)	DC CTL (2.5V + 10%)	DC CTL (2.5V -10%)
7C		Not used						
7D		Not used						
7E		Not used						
7F		Not used						

Copyright ©2000,2002, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type8 (1/4)

	0	1	2	3	4	5	6	7
40		CARB::P0ERR0						
	P0DRINP-ERR	P0LRCERR	P0ENDC-ERR	P0SLRCERR	P0DROUT PERR	P0ORINP-ERR	P0WR1TO-ERR	CLKERR
41		CARB::P0ERR0						
	ABTCMP-ERR	ABTSEQP-ERR	P0SEQAP-ERR	P0SEQAC PERR	P0SEQAT PERR	P0SEQBT-ERR	P0J1CNT PERR	P0J4CNT PERR
42		CARB::P0ERR0						
	P0SEQBT PERR	P0SEQDP-ERR	P0S0CNT PERR	P0S1CNT PERR	P0WR1P-ERR	P0MICERR	P0MACS-ERR	T6PERR
43		Not used						
44		CARB::P1ERR0						
	P1DRINP-ERR	P1LRCERR	P1ENDC-ERR	P1SLRCERR	P1DROUT PERR	P1ORINP-ERR	P1WR1TO-ERR	CLKERR
45		CARB::P1ERR0						
	ABTCMP-ERR	ABTSEQP-ERR	P1SEQAP-ERR	P1SEQAC PERR	P1SEQAT PERR	P1SEQBT-ERR	P1J1CNT PERR	P1J4CNT PERR
46		CARB::P1ERR0						
	P1SEQBT PERR	P1SEQDP-ERR	P1S0CNT PERR	P1S1CNT PERR	P1WR1P-ERR	P1MICERR	P1MACS-ERR	T6PERR
47		Not used						
48		CARB::P2ERR0						
	P2DRINP-ERR	P2LRCERR	P2ENDC-ERR	P2SLRCERR	P2DROUT PERR	P2ORINP-ERR	P2WR1TO-ERR	CLKERR
49		CARB::P2ERR0						
	ABTCMP-ERR	ABTSEQP-ERR	P2SEQAP-ERR	P2SEQAC PERR	P2SEQAT PERR	P2SEQBT-ERR	P2J1CNT PERR	P2J4CNT PERR
4A		CARB::P2ERR0						
	P2SEQBT PERR	P2SEQDP-ERR	P2S0CNT PERR	P2S1CNT PERR	P2WR1P-ERR	P2MICERR	P2MACS-ERR	T6PERR
4B		Not used						
4C		CARB::P3ERR0						
	P3DRINP-ERR	P3LRCERR	P3ENDC-ERR	P3SLRCERR	P3DROUT PERR	P3ORINP-ERR	P3WR1TO-ERR	CLKERR
4D		CARB::P3ERR0						
	ABTCMP-ERR	ABTSEQP-ERR	P3SEQAP-ERR	P3SEQAC PERR	P3SEQAT PERR	P3SEQBT-ERR	P3J1CNT PERR	P3J4CNT PERR
4E		CARB::P3ERR0						
	P3SEQBT PERR	P3SEQDP-ERR	P3S0CNT PERR	P3S1CNT PERR	P3WR1P-ERR	P3MICERR	P3MACS-ERR	T6PERR
4F		Not used						

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type8 (2/4)

	0	1	2	3	4	5	6	7
50		CARB::P4ERR0						
	P4DRINP-ERR	P4LRCERR	P4ENDC-ERR	P4SLRCERR	P4DROUT PERR	P4ORINP-ERR	P4WR1TO-ERR	CLKERR
51		CARB::P4ERR0						
	ABTCMP-ERR	ABTSEQP-ERR	P4SEQAP-ERR	P4SEQAC PERR	P4SEQAT PERR	P4SEQBT-ERR	P4J1CNT PERR	P4J4CNT PERR
52		CARB::P4ERR0						
	P4SEQBT PERR	P4SEQDP-ERR	P4S0CNT PERR	P4S1CNT PERR	P4WR1P-ERR	P4MICERR	P4MACS-ERR	T6PERR
53		Not used						
54		CARB::P5ERR0						
	P5DRINP-ERR	P5LRCERR	P5ENDC-ERR	P5SLRCERR	P5DROUT PERR	P5ORINP-ERR	P5WR1TO-ERR	CLKERR
55		CARB::P5ERR0						
	ABTCMP-ERR	ABTSEQP-ERR	P5SEQAP-ERR	P5SEQAC PERR	P5SEQAT PERR	P5SEQBT-ERR	P5J1CNT PERR	P5J4CNT PERR
56		CARB::P5ERR0						
	P5SEQBT PERR	P5SEQDP-ERR	P5S0CNT PERR	P5S1CNT PERR	P5WR1P-ERR	P5MICERR	P5MACS-ERR	T6PERR
57		Not used						
58		CARB::P6ERR0						
	P6DRINP-ERR	P6LRCERR	P6ENDC-ERR	P6SLRCERR	P6DROUT PERR	P6ORINP-ERR	P6WR1TO-ERR	CLKERR
59		CARB::P6ERR0						
	ABTCMP-ERR	ABTSEQP-ERR	P6SEQAP-ERR	P6SEQAC PERR	P6SEQAT PERR	P6SEQBT-ERR	P6J1CNT PERR	P6J4CNT PERR
5A		CARB::P6ERR0						
	P6SEQBT PERR	P6SEQDP-ERR	P6S0CNT PERR	P6S1CNT PERR	P6WR1P-ERR	P6MICERR	P6MACS-ERR	T6PERR
5B		Not used						
5C		CARB::P7ERR0						
	P7DRINP-ERR	P7LRCERR	P7ENDC-ERR	P7SLRCERR	P7DROUT PERR	P7ORINP-ERR	P7WR1TO-ERR	CLKERR
5D		CARB::P7ERR0						
	ABTCMP-ERR	ABTSEQP-ERR	P7SEQAP-ERR	P7SEQAC PERR	P7SEQAT PERR	P7SEQBT-ERR	P7J1CNT PERR	P7J4CNT PERR
5E		CARB::P7ERR0						
	P7SEQBT PERR	P7SEQDP-ERR	P7S0CNT PERR	P7S1CNT PERR	P7WR1P-ERR	P7MICERR	P7MACS-ERR	T6PERR
5F		Not used						

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type8 (3/4)

	0	1	2	3	4	5	6	7
60		CARB::C0ERR0						
	C0 ORINPER	C0 DRINPER	C0 PLRC ERR	C0 ENDC ERR	C0SLRC ERR	C0 DROPERR	0	0
61		CARB::C0ERR0						
	C0 RD1TMO	C0 RD2TMO	C0 WR2TMO	0	0	0	0	0
62		CARB::C0ERR1						
	C0 SEQCPERR	C0 TCNTPERR	C0 DRPINPERR	C0 SEQDPERR	C0 IPPINPERR0	C0 IPPINPERR1	0	0
63		CARB::C0ERR1						
	C0 RD1TMR-PER	C0 RD2TMR-PER	C0 WR2TMR-PER	C0 STMPERR	C0 SCNPERR	0	0	0
64		CARB::C1ERR0						
	C1 ORINPER	C1 DRINPER	C2 PLRC ERR	C1 ENDC ERR	C1SLRC ERR	C1 DROPERR	0	0
65		CARB::C1ERR0						
	C1 RD1TMO	C1 RD2TMO	C1 WR2TMO	0	0	0	0	0
66		CARB::C1ERR1						
	C1 SEQCPERR	C1 TCNTPERR	C1 DRPINPERR	C1 SEQDPERR	C1 IPPINPERR0	C1 IPPINPERR1	0	0
67		CARB::C1ERR1						
	C1 RD1TMR-PER	C1 RD2TMR-PER	C1 WR2TMR-PER	C1 STMPERR	C1 SCNPERR	0	0	0
68		CARB::C2ERR0						
	C2 ORINPER	C2 DRINPER	C2 PLRC ERR	C2 ENDC ERR	C2SLRC ERR	C2 DROPERR	0	0
69		CARB::C2ERR0						
	C2 RD1TMO	C2 RD2TMO	C2 WR2TMO	0	0	0	0	0
6A		CARB::C2ERR1						
	C2 SEQCPERR	C2 TCNTPERR	C2 DRPINPERR	C2 SEQDPERR	C2 IPPINPERR0	C2 IPPINPERR1	0	0
6B		CARB::C2ERR0						
	C2 RD1TMR-PER	C2 RD2TMR-PER	C2 WR2TMR-PER	C2 STMPERR	C2 SCNPERR	0	0	0
6C		CARB::C3ERR0						
	C3 ORINPER	C3 DRINPER	C3 PLRC ERR	C3 ENDC ERR	C3SLRC ERR	C3 DROPERR	0	0
6D		CARB::C3ERR1						
	C3 RD1TMO	C3 RD2TMO	C3 WR2TMO	0	0	0	0	0
6E		CARB::C3ERR1						
	C3 SEQCPERR	C3 TCNTPERR	C3 DRPINPERR	C3 SEQDPERR	C3 IPPINPERR0	C3 IPPINPERR1	0	0
6F		CARB::C3ERR1						
	C3 RD1TMR-PER	C3 RD2TMR-PER	C3 WR2TMR-PER	C3 STMPERR	C3 SCNPERR	0	0	0

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type8 (4/4)

	0	1	2	3	4	5	6	7
70	Not used							
71	Not used							
72	Not used							
73	Not used							
74	Not used							
75	Not used							
76	Not used							
77	Not used							
78	Not used							
79	Not used							
7A	Not used							
7B	Not used							
7C	Not used							
7D	Not used							
7E	Not used							
7F	Not used							

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type9 (1/4)

	0	1	2	3	4	5	6	7
40	Not used							
41	Not used							
42	SMA:: BCAST REG5 MASK							
	BC REG5 MASK bit 20	BC REG5 MASK bit 21	BC REG5 MASK bit 22	BC REG5 MASK bit 23	BC REG5 MASK bit 24	BC REG5 MASK bit 25	BC REG5 MASK bit 26	BC REG5 MASK bit 27
43	SMA:: BCAST REG5 MASK							
	BC REG5 MASK bit 30	BC REG5 MASK bit 31	BC REG5 MASK bit 32	BC REG5 MASK bit 33	BC REG5 MASK bit 34	BC REG5 MASK bit 35	BC REG5 MASK bit 36	BC REG5 MASK bit 37
44	SMA::SCINT OUTPUT MASK							
	SC_MASK MPA#0	SC_MASK MPA#1	SC_MASK MPA#2	SC_MASK MPA#3	SC_MASK MPA#4	SC_MASK MPA#5	SC_MASK MPA#6	SC_MASK MPA#7
45	SMA::SCINT OUTPUT MASK							
	SC_MASK MPA#8	SC_MASK MPA#9	SC_MASK MPA#A	SC_MASK MPA#B	SC_MASK MPA#C	SC_MASK MPA#D	SC_MASK MPA#E	SC_MASK MPA#F
46	SMA::MP STATUS TIMEOUT DATA							
	MPST_TODT							
47	SMA::MP STATUS TIMEOUT DATA							
	MPST_TODT							
48	SMA::VALID TIMER TIMEOUT DATA							
	VAL_TODT							
49	SMA::VALID TIMER TIMEOUT DATA							
	VAL_TODT							
4A	SMA::SCINT TIMEOUT DATA							
	SC_TODT							
4B	SMA::SCINT TIMEOUT DATA							
	SC_TODT							
4C	SMA::SCAN COUNTER PARITY ERROR							
	SCCNT_PERR MPA#0	SCCNT_PERR MPA#1	SCCNT_PERR MPA#2	SCCNT_PERR MPA#3	SCCNT_PERR MPA#4	SCCNT_PERR MPA#5	SCCNT_PERR MPA#6	SCCNT_PERR MPA#7
4D	SMA::SCAN COUNTER PARITY ERROR							
	SCCNT_PERR MPA#8	SCCNT_PERR MPA#9	SCCNT_PERR MPA#A	SCCNT_PERR MPA#B	SCCNT_PERR MPA#C	SCCNT_PERR MPA#D	SCCNT_PERR MPA#E	SCCNT_PERR MPA#F
4E	SMA::VALID COUNTER PARITY ERROR							
	VALCNT_PERR MPA#0	VALCNT_PERR MPA#1	VALCNT_PERR MPA#2	VALCNT_PERR MPA#3	VALCNT_PERR MPA#4	VALCNT_PERR MPA#5	VALCNT_PERR MPA#6	VALCNT_PERR MPA#7
4F	SMA::VALID COUNTER PARITY ERROR							
	VALCNT_PERR MPA#8	VALCNT_PERR MPA#9	VALCNT_PERR MPA#A	VALCNT_PERR MPA#B	VALCNT_PERR MPA#C	VALCNT_PERR MPA#D	VALCNT_PERR MPA#E	VALCNT_PERR MPA#F

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type9 (2/4)

	0	1	2	3	4	5	6	7
50	SMA::SCAN SEQUENCER ERROR							
	SCSEQ_ERR MPA#0	SCSEQ_ERR MPA#1	SCSEQ_ERR MPA#2	SCSEQ_ERR MPA#3	SCSEQ_ERR MPA#4	SCSEQ_ERR MPA#5	SCSEQ_ERR MPA#6	SCSEQ_ERR MPA#7
51	SMA::SCAN SEQUENCER ERROR							
	SCSEQ_ERR MPA#8	SCSEQ_ERR MPA#9	SCSEQ_ERR MPA#A	SCSEQ_ERR MPA#B	SCSEQ_ERR MPA#C	SCSEQ_ERR MPA#D	SCSEQ_ERR MPA#E	SCSEQ_ERR MPA#F
52	SMA::SCINT OUT ERROR							
	SINT_OUT_ ERR MPA#0	SINT_OUT_ ERR MPA#1	SINT_OUT_ ERR MPA#2	SINT_OUT_ ERR MPA#3	SINT_OUT_ ERR MPA#4	SINT_OUT_ ERR MPA#5	SINT_OUT_ ERR MPA#6	SINT_OUT_ ERR MPA#7
53	SMA::SCINT OUT ERROR							
	SINT_OUT_ ERR MPA#8	SINT_OUT_ ERR MPA#9	SINT_OUT_ ERR MPA#A	SINT_OUT_ ERR MPA#B	SINT_OUT_ ERR MPA#C	SINT_OUT_ ERR MPA#D	SINT_OUT_ ERR MPA#E	SINT_OUT_ ERR MPA#F
54	SMA::SCINT SIGNAL							
	SINT_SIG MPA#0	SINT_SIG MPA#1	SINT_SIG MPA#2	SINT_SIG MPA#3	SINT_SIG MPA#4	SINT_SIG MPA#5	SINT_SIG MPA#6	SINT_SIG MPA#7
55	SMA::SCINT SIGNAL							
	SINT_SIG MPA#8	SINT_SIG MPA#9	SINT_SIG MPA#A	SINT_SIG MPA#B	SINT_SIG MPA#C	SINT_SIG MPA#D	SINT_SIG MPA#E	SINT_SIG MPA#F
56	Not used							
57	Not used							
58	Not used							
59	SMA::PATH0 ERROR STATUS							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
5A	SMA::PATH0 ERROR STATUS							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
5B	SMA::PATH0 ERROR STATUS							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	Not used	Not used	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
5C	SMA::PATH0 ERROR DETAIL							
	RX CMD PARITY ERROR	RX ADR PARITY ERROR	RX WDT PARITY ERROR	Not used	SYNC0 UNDER ERROR	SYNC1 UNDER ERROR	SYNC0 OVER ERROR	SYNC1 OVER ERROR
5D	SMA::PATH0 ERROR DETAIL							
	LRC ERROR	LRC COMPERE ERROR	LOCK COMMAND ERROR	R/W COMMAND ERROR	ILLEGAL LOCK DBL ERROR	DOUBLE LOCK ERROR	LOCK ACCESS OVER(ENT)	Not used
5E	SMA::PATH0 ERROR DETAIL							
	CMD PGEN ERROR	ADR PGEN ERROR	WDT PGEN ERROR	PCB PARITY ERROR	PAB PARITY ERROR	PWB PARITY ERROR	PCB LOCK COMMAND ERROR	PCB R/W COMMAND ERROR
5F	SMA::PATH0 ERROR DETAIL							
	Not used	Not used	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	Not used	PATH SEQUENCE R ERROR	REQ COUNTER PARITY ERROR	LOCK COUNTER PATH ERROR

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type9 (3/4)

	0	1	2	3	4	5	6	7
60	Not used							
61	SMA::PATH1 ERROR STATUS							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
62	SMA::PATH1 ERROR STATUS							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
63	SMA::PATH1 ERROR STATUS							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	Not used	Not used	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
64	SMA::PATH1 ERROR DETAIL							
	RX CMD PARITY ERROR	RX ADR PARITY ERROR	RX WDT PARITY ERROR	Not used	SYNC0 UNDER ERROR	SYNC1 UNDER ERROR	SYNC0 OVER ERROR	SYNC1 OVER ERROR
65	SMA::PATH1 ERROR DETAIL							
	LRC ERROR	LRC COMPERE ERROR	LOCK COMMAND ERROR	R/W COMMAND ERROR	ILLEGAL LOCK DBL ERROR	DOUBLE LOCK ERROR	LOCK ACCESS OVER(ENT)	Not used
66	SMA::PATH1 ERROR DETAIL							
	CMD PGEN ERROR	ADR PGEN ERROR	WDT PGEN ERROR	PCB PARITY ERROR	PAB PARITY ERROR	PWB PARITY ERROR	PCB LOCK COMMAND ERROR	PCB R/W COMMAND ERROR
67	SMA::PATH1 ERROR DETAIL							
	Not used	Not used	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	Not used	PATH SEQUENCE R ERROR	REQ COUNTER PARITY ERROR	LOCK COUNTER PATH ERROR
68	SMA::BOARD ERROR STATUS							
	MCB PARITY ERROR	MAB PARITY ERROR	MWB PARITY ERROR	SIMMSEL PARITY ERROR	MEMPATHA DR PARITY ERROR	RDTLT NOTHING ERROR	ICB PARITY ERROR	IAB PARITY ERROR
69	SMA::BOARD ERROR STATUS							
	IWB PARYTY ERROR	I/O PATHADR PARITY ERROR	PDADR OUTPUT ERROR	LOCK ADR PARITY ERROR	LOCK WAIT TIMEOUT	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	SLOT PARITY ERROR
6A	SMA::BOARD ERROR STATUS							
	CLOCK ERROR	REFRESH ERROR	TIMER PARITY ERROR	ARBITER ERROR	WT WEQ PARITY ERROR	RD SEQ PARITY ERROR	MEM SEQ PARITY ERROR	I/O SEQ PARITY ERROR
6B	SMA::BOARD ERROR STATUS							
	ECC GENERATE ERROR	SMDT OUTPUT ERROR	BSSWEN OUTPUT ERROR	VALID CNT PARITY ERROR	SCAN CNT PARITY ERROR	SCAn SEQ ERROR	BCINT OUTPUT ERROR	SCINT OUTPUT ERROR
6C	Not used							
6D	Not used							
6E	SMA::BOARD ERROR DETAIL							
	Not used	Not used	Not used	Not used	Not used	MEMORY ARBITER ERROR	LOCK ARBITER ERROR	I/O ARBITER ERROR
6F	SMA::BOARD ERROR DETAIL							
	Not used	CLOCK GENERATE ERROR	CLOCK CNT PARITY ERROR	CLOCK FREQUEN-CY ERROR	Not used	INITIAL CNT PARITY ERROR	REFRESH CNT PARITY ERROR	REFRESH PROTCOL ERROR

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type9 (4/4)

	0	1	2	3	4	5	6	7
70	MPA:: MPAINTSTS							
	0	0	0	0	0	0	SCINT0	SCINT1
71	MPA:: MPAINTSTS							
	XR BC0	XR BC1	XR BC2	XR BC3	XR BC4	BCREQ	BCINT0	BCINT1
72	SMA:: SMACNTRL							
	DBG SIG	Not used	Not used	Not used	Not used	BSSW CHK EN	ENT WAIT EN	ENTOFF RST EN
73	SMA:: SMACNTRL							
	SMPSDWN EN	CLK CHK EN	ECC ADR MSK	DIAG EN	DUMP MODE	PWR DWN EN	DT RVS INH	REF MODE
74	Not used							
75	SMA:: SMASTATS							
	Not used	Not used	Not used	Not used	SLOT (Side B)	SLOT (Side A)	DISC MODE	PWR DWN MODE
76	SMA:: SMASTATS							
	DISC REQ	SELF REF	SMPS DWN	PS DTCT	TIM EN	ALL LOCK	MEM PDY	SM EN
77	SMA:: SMASTATS							
	PK VER				LSI VER			
78	MPA:: RXAEDT							
	MPST INT	MPST STATUS FLAG	MPST VALID	MPST TIMEOUT	SCAN INT	SCAN READDATA FLAG	SCAN STATUS FLAG	SCAN TIMEOUT
79	MPA:: RXAEDT							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
7A	MPA:: RXAEDT							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
7B	MPA:: RXAEDT							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	0	0	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
7C	MPA:: RXBEDT							
	MPST INT	MPST STATUS FLAG	MPST VALID	MPST TIMEOUT	SCAN INT	SCAN READDATA FLAG	SCAN STATUS FLAG	SCAN TIMEOUT
7D	MPA:: RXBEDT							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
7E	MPA:: RXBEDT							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
7F	MPA:: RXBEDT							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	0	0	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type10 (1/4)

	0	1	2	3	4	5	6	7
40	SMA:: BCAST REG0 MASK							
	BC REG0 MASK bit 00	BC REG0 MASK bit 01	BC REG0 MASK bit 02	BC REG0 MASK bit 03	BC REG0 MASK bit 04	BC REG0 MASK bit 05	BC REG0 MASK bit 06	BC REG0 MASK bit 07
41	SMA:: BCAST REG0 MASK							
	BC REG0 MASK bit 10	BC REG0 MASK bit 11	BC REG0 MASK bit 12	BC REG0 MASK bit 13	BC REG0 MASK bit 14	BC REG0 MASK bit 15	BC REG0 MASK bit 16	BC REG0 MASK bit 17
42	SMA:: BCAST REG0 MASK							
	BC REG0 MASK bit 20	BC REG0 MASK bit 21	BC REG0 MASK bit 22	BC REG0 MASK bit 23	BC REG0 MASK bit 24	BC REG0 MASK bit 25	BC REG0 MASK bit 26	BC REG0 MASK bit 27
43	SMA:: BCAST REG0 MASK							
	BC REG0 MASK bit 30	BC REG0 MASK bit 31	BC REG0 MASK bit 32	BC REG0 MASK bit 33	BC REG0 MASK bit 34	BC REG0 MASK bit 35	BC REG0 MASK bit 36	BC REG0 MASK bit 37
44	SMA:: BCAST REG1 MASK							
	BC REG1 MASK bit 00	BC REG1 MASK bit 01	BC REG1 MASK bit 02	BC REG1 MASK bit 03	BC REG1 MASK bit 04	BC REG1 MASK bit 05	BC REG1 MASK bit 06	BC REG1 MASK bit 07
45	SMA:: BCAST REG1 MASK							
	BC REG1 MASK bit 10	BC REG1 MASK bit 11	BC REG1 MASK bit 12	BC REG1 MASK bit 13	BC REG1 MASK bit 14	BC REG1 MASK bit 15	BC REG1 MASK bit 16	BC REG1 MASK bit 17
46	SMA:: BCAST REG1 MASK							
	BC REG1 MASK bit 20	BC REG1 MASK bit 21	BC REG1 MASK bit 22	BC REG1 MASK bit 23	BC REG1 MASK bit 24	BC REG1 MASK bit 25	BC REG1 MASK bit 26	BC REG1 MASK bit 27
47	SMA:: BCAST REG1 MASK							
	BC REG1 MASK bit 30	BC REG1 MASK bit 31	BC REG1 MASK bit 32	BC REG1 MASK bit 33	BC REG1 MASK bit 34	BC REG1 MASK bit 35	BC REG1 MASK bit 36	BC REG1 MASK bit 37
48	SMA:: BCAST REG2 MASK							
	BC REG2 MASK bit 00	BC REG2 MASK bit 01	BC REG2 MASK bit 02	BC REG2 MASK bit 03	BC REG2 MASK bit 04	BC REG2 MASK bit 05	BC REG2 MASK bit 06	BC REG2 MASK bit 07
49	SMA:: BCAST REG2 MASK							
	BC REG2 MASK bit 10	BC REG2 MASK bit 11	BC REG2 MASK bit 12	BC REG2 MASK bit 13	BC REG2 MASK bit 14	BC REG2 MASK bit 15	BC REG2 MASK bit 16	BC REG2 MASK bit 17
4A	SMA:: BCAST REG2 MASK							
	BC REG2 MASK bit 20	BC REG2 MASK bit 21	BC REG2 MASK bit 22	BC REG2 MASK bit 23	BC REG2 MASK bit 24	BC REG2 MASK bit 25	BC REG2 MASK bit 26	BC REG2 MASK bit 27
4B	SMA:: BCAST REG2 MASK							
	BC REG2 MASK bit 30	BC REG2 MASK bit 31	BC REG2 MASK bit 32	BC REG2 MASK bit 33	BC REG2 MASK bit 34	BC REG2 MASK bit 35	BC REG2 MASK bit 36	BC REG2 MASK bit 37
4C	SMA:: BCAST REG3 MASK							
	BC REG3 MASK bit 00	BC REG3 MASK bit 01	BC REG3 MASK bit 02	BC REG3 MASK bit 03	BC REG3 MASK bit 04	BC REG3 MASK bit 05	BC REG3 MASK bit 06	BC REG3 MASK bit 07
4D	SMA:: BCAST REG3 MASK							
	BC REG3 MASK bit 10	BC REG3 MASK bit 11	BC REG3 MASK bit 12	BC REG3 MASK bit 13	BC REG3 MASK bit 14	BC REG3 MASK bit 15	BC REG3 MASK bit 16	BC REG3 MASK bit 17
4E	SMA:: BCAST REG3 MASK							
	BC REG3 MASK bit 20	BC REG3 MASK bit 21	BC REG3 MASK bit22	BC REG3 MASK bit 23	BC REG3 MASK bit 24	BC REG3 MASK bit 25	BC REG3 MASK bit 26	BC REG3 MASK bit 27
4F	SMA:: BCAST REG3 MASK							
	BC REG3 MASK bit 30	BC REG3 MASK bit 31	BC REG3 MASK bit 32	BC REG3 MASK bit 33	BC REG3 MASK bit 34	BC REG3 MASK bit 35	BC REG3 MASK bit 36	BC REG3 MASK bit 37

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type10 (2/4)

	0	1	2	3	4	5	6	7
50	SMA:: BCAST REG4 MASK							
	BC REG4 MASK bit 00	BC REG4 MASK bit 01	BC REG4 MASK bit 02	BC REG4 MASK bit 03	BC REG4 MASK bit 04	BC REG4 MASK bit 05	BC REG4 MASK bit 06	BC REG4 MASK bit 07
51	SMA:: BCAST REG4 MASK							
	BC REG4 MASK bit 10	BC REG4 MASK bit 11	BC REG4 MASK bit 12	BC REG4 MASK bit 13	BC REG4 MASK bit 14	BC REG4 MASK bit 15	BC REG4 MASK bit 16	BC REG4 MASK bit 17
52	SMA:: BCAST REG4 MASK							
	BC REG4 MASK bit 20	BC REG4 MASK bit 21	BC REG4 MASK bit 22	BC REG4 MASK bit 23	BC REG4 MASK bit 24	BC REG4 MASK bit 25	BC REG4 MASK bit 26	BC REG4 MASK bit 27
53	SMA:: BCAST REG4 MASK							
	BC REG4 MASK bit 30	BC REG4 MASK bit 31	BC REG4 MASK bit 32	BC REG4 MASK bit 33	BC REG4 MASK bit 34	BC REG4 MASK bit 35	BC REG4 MASK bit 36	BC REG4 MASK bit 37
54	SMA::BCINT OUT ERROR							
	BINT_OUT_ ERR MPA#0	BINT_OUT_ ERR MPA#1	BINT_OUT_ ERR MPA#2	BINT_OUT_ ERR MPA#3	BINT_OUT_ ERR MPA#4	BINT_OUT_ ERR MPA#5	BINT_OUT_ ERR MPA#6	BINT_OUT _ERR MPA#7
55	SMA::BCINT OUT ERROR							
	BINT_OUT_ ERR MPA#8	BINT_OUT_ ERR MPA#9	BINT_OUT_ ERR MPA#A	BINT_OUT_ ERR MPA#B	BINT_OUT_ ERR MPA#C	BINT_OUT_ ERR MPA#D	BINT_OUT_ ERR MPA#E	BINT_OUT _ERR MPA#F
56	SMA::BCINT SIGNAL							
	BINT_SIG MPA#0	BINT_SIG MPA#1	BINT_SIG MPA#2	BINT_SIG MPA#3	BINT_SIG MPA#4	BINT_SIG MPA#5	BINT_SIG MPA#6	BINT_SIG MPA#7
57	SMA::BCINT SIGNAL							
	BINT_SIG MPA#8	BINT_SIG MPA#9	BINT_SIG MPA#A	BINT_SIG MPA#B	BINT_SIG MPA#C	BINT_SIG MPA#D	BINT_SIG MPA#E	BINT_SIG MPA#F
58	Not used							
59	SMA::PATH0 ERROR STATUS							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
5A	SMA::PATH0 ERROR STATUS							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
5B	SMA::PATH0 ERROR STATUS							
	CORRECTA-BLE ERROR	UNCORREC -TABLE ERROR	I/O REG PARITY ERROR	Not used	Not used	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
5C	SMA::PATH0 ERROR DETAIL							
	RX CMD PARITY ERROR	RX ADR PARITY ERROR	RX WDT PARITY ERROR	Not used	SYNC0 UNDER ERROR	SYNC1 UNDER ERROR	SYNC0 OVER ERROR	SYNC1 OVER ERROR
5D	SMA::PATH0 ERROR DETAIL							
	LRC ERROR	LRC COMPERE ERROR	LOCK COMMAND ERROR	R/W COMMAND ERROR	ILLEGAL LOCK DBL ERROR	DOUBLE LOCK ERROR	LOCK ACCESS OVER(ENT)	Not used
5E	SMA::PATH0 ERROR DETAIL							
	CMD PGEN ERROR	ADR PGEN ERROR	WDT PGEN ERROR	PCB PARITY ERROR	PAB PARITY ERROR	PWB PARITY ERROR	PCB LOCK COMMAND ERROR	PCB R/W COMMAND ERROR
5F	SMA::PATH0 ERROR DETAIL							
	Not used	Not used	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	Not used	PATH SEQUENCE R ERROR	REQ COUNTER PARITY ERROR	LOCK COUNTER PATH ERROR

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type10 (3/4)

	0	1	2	3	4	5	6	7
60	Not used							
61	SMA::PATH1 ERROR STATUS							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
62	SMA::PATH1 ERROR STATUS							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
63	SMA::PATH1 ERROR STATUS							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	Not used	Not used	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
64	SMA::PATH1 ERROR DETAIL							
	RX CMD PARITY ERROR	RX ADR PARITY ERROR	RX WDT PARITY ERROR	Not used	SYNC0 UNDER ERROR	SYNC1 UNDER ERROR	SYNC0 OVER ERROR	SYNC1 OVER ERROR
65	SMA::PATH1 ERROR DETAIL							
	LRC ERROR	LRC COMPERE ERROR	LOCK COMMAND ERROR	R/W COMMAND ERROR	ILLEGAL LOCK DBL ERROR	DOUBLE LOCK ERROR	LOCK ACCESS OVER(ENT)	Not used
66	SMA::PATH1 ERROR DETAIL							
	CMD PGEN ERROR	ADR PGEN ERROR	WDT PGEN ERROR	PCB PARITY ERROR	PAB PARITY ERROR	PWB PARITY ERROR	PCB LOCK COMMAND ERROR	PCB R/W COMMAND ERROR
67	SMA::PATH1 ERROR DETAIL							
	Not used	Not used	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	Not used	PATH SEQUENCE R ERROR	REQ COUNTER PARITY ERROR	LOCK COUNTER PATH ERROR
68	SMA::BOARD ERROR STATUS							
	MCB PARITY ERROR	MAB PARITY ERROR	MWB PARITY ERROR	SIMMSEL PARITY ERROR	MEMPATHA DR PARITY ERROR	RDTLT NOTHING ERROR	ICB PARITY ERROR	IAB PARITY ERROR
69	SMA::BOARD ERROR STATUS							
	IWB PARYTY ERROR	I/O PATHADR PARITY ERROR	PDADR OUTPUT ERROR	LOCK ADR PARITY ERROR	LOCK WAIT TIMEOUT	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	SLOT PARITY ERROR
6A	SMA::BOARD ERROR STATUS							
	CLOCK ERROR	REFRESH ERROR	TIMER PARITY ERROR	ARBITER ERROR	WT WEQ PARITY ERROR	RD SEQ PARITY ERROR	MEM SEQ PARITY ERROR	I/O SEQ PARITY ERROR
6B	SMA::BOARD ERROR STATUS							
	ECC GENERATE ERROR	SMDT OUTPUT ERROR	BSSWEN OUTPUT ERROR	VALID CNT PARITY ERROR	SCAN CNT PARITY ERROR	SCAn SEQ ERROR	BCINT OUTPUT ERROR	SCINT OUTPUT ERROR
6C	Not used							
6D	Not used							
6E	SMA::BOARD ERROR DETAIL							
	Not used	Not used	Not used	Not used	Not used	MEMORY ARBITER ERROR	LOCK ARBITER ERROR	I/O ARBITER ERROR
6F	SMA::BOARD ERROR DETAIL							
	Not used	CLOCK GENERATE ERROR	CLOCK CNT PARITY ERROR	CLOCK FREQUEN-CY ERROR	Not used	INITIAL CNT PARITY ERROR	REFRESH CNT PARITY ERROR	REFRESH PROTCOL ERROR

Copyright ©2000, Hitachi, Ltd.

Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type10 (4/4)

	0	1	2	3	4	5	6	7
70	MPA:: MPAINTSTS							
	0	0	0	0	0	0	SCINT0	SCINT1
71	MPA::MPA INTSTS							
	XR BC0	XR BC1	XR BC2	XR BC3	XR BC4	BCREQ	BCINT0	BCINT1
72	SMA::SMA CONTROL							
	DBG SIG	Not used	Not used	Not used	Not used	BSSW CHK EN	ENT WAIT EN	ENTOFF RST EN
73	SMA::SMA CONTROL							
	SMPSDWN EN	CLK CHK EN	ECC ADR MSK	DIAG EN	DUMP MODE	PWR DWN EN	DT RVS INH	REF MODE
74	Not used							
75	SMA::SMA STATUS							
	Not used	Not used	Not used	Not used	SLOT (Side B)	SLOT (Side A)	DISC MODE	PWR DWN MODE
76	SMA::SMA STATUS							
	DISC REQ	SELF REF	SMPS DWN	PS DTCT	TIM EN	ALL LOCK	MEM PDY	SM EN
77	SMA::SMA STATUS							
	PK VER				LSI VER			
78	MPA:: RXAEDT							
	MPST INT	MPST STATUS FLAG	MPST VALID	MPST TIMEOUT	SCAN INT	SCAN READDATA FLAG	SCAN STATUS FLAG	SCAN TIMEOUT
79	MPA:: RXAEDT							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
7A	MPA:: RXAEDT							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
7B	MPA:: RXAEDT							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	0	0	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
7C	MPA:: RXBEDT							
	MPST INT	MPST STATUS FLAG	MPST VALID	MPST TIMEOUT	SCAN INT	SCAN READDATA FLAG	SCAN STATUS FLAG	SCAN TIMEOUT
7D	MPA:: RXBEDT							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
7E	MPA:: RXBEDT							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
7F	MPA:: RXBEDT							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	0	0	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR

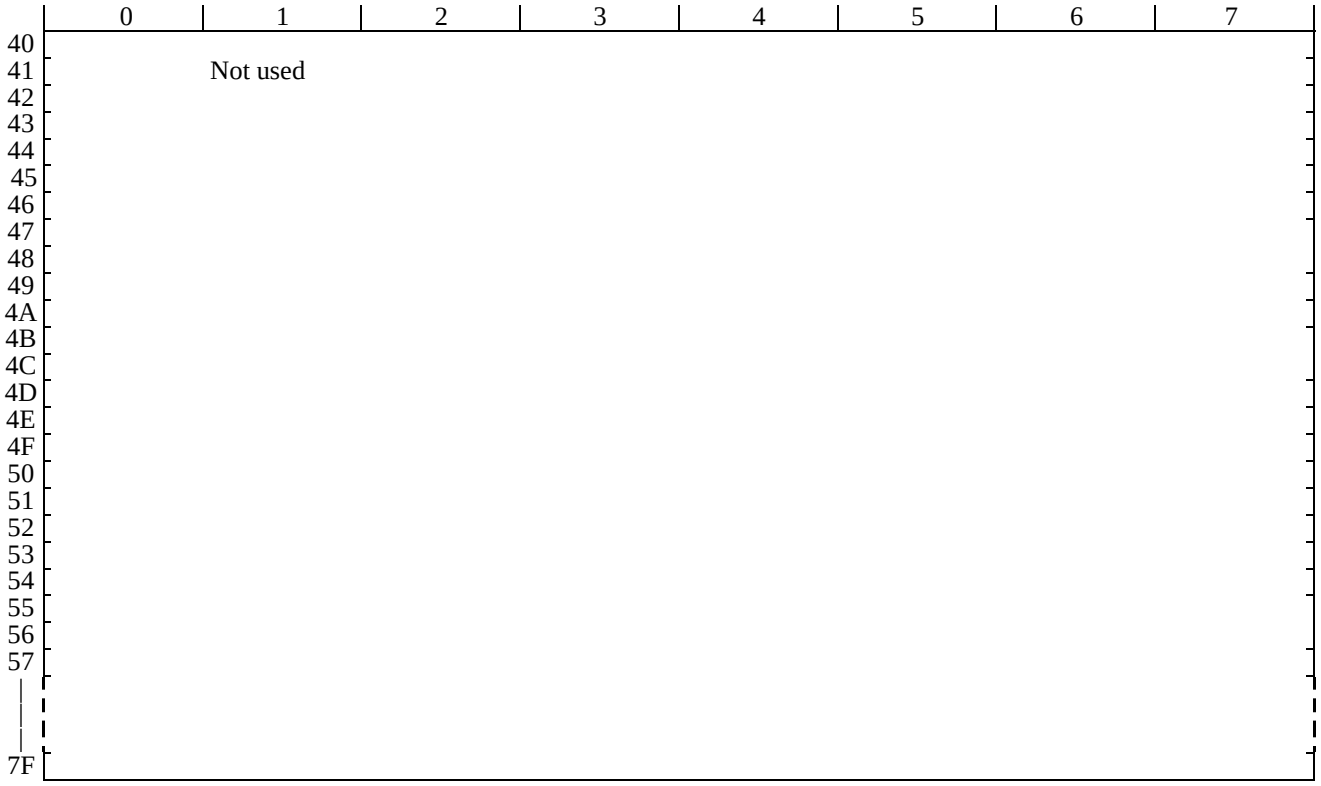
Copyright ©2000, Hitachi, Ltd.

Byte0D : Bit1 = 1 & Byte36-37 = 08C1 (Machine Condition Exception) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x‘06’ : Cache DKC)							
23	Count							
24	Device address							
25	Device type							
26	Content (x‘6’)				Format (x‘3’)			
27	Operation byte of LR/LRE command parameter							
28	Auxiliary byte of LR/LRE command parameter							
29	Byte 2 for LR/LRE command							
2A	Reserved							
2B								
2C	Search parameter of LR command(CCHHR)							
2D	or							
2E	Record ID of re-execution command(R)							
2F								
30	Sector number to re-execute the LR command							
31	TLF for LR/LRE command							
32								
33	Operation byte = 0x3F :LRE External operation byte others :Reserved							
34	SSID (Low) of self subsystem							
35								
36	Exception code (x‘08C1’)							
37								
38	Log and message control (x‘05’)							
39	Program action code (x‘10’)							
3A	Configuration information							
3B								
3C	Not usde (x‘01’)							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte0D : Bit1 = 1 & Byte36-37 = 08C1 (Machine Condition Exception) (2/2)



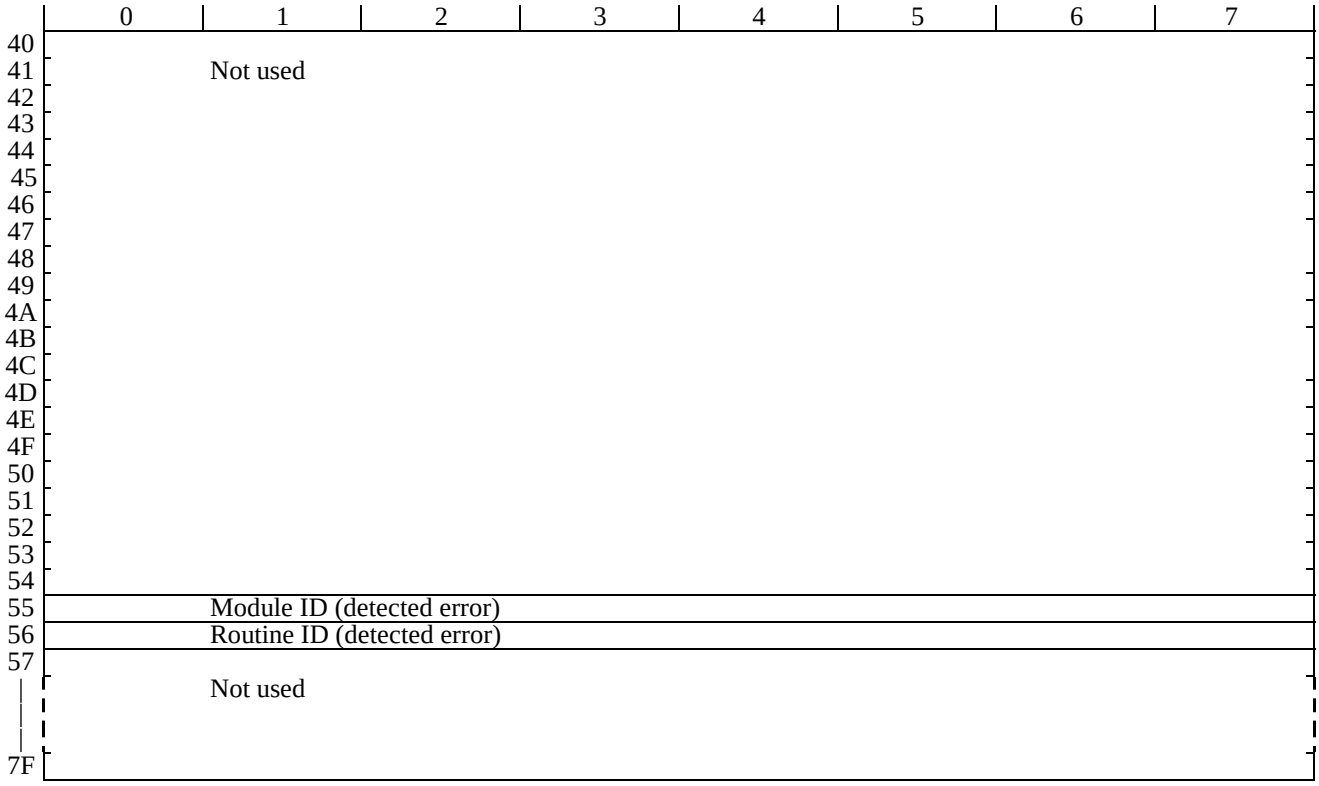
Copyright ©2000, Hitachi, Ltd.

Byte0D : Bit1 = 1 & Byte36-37 = 0212 (Command Sequence Exception: Incomplete Domain) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x‘06’ : Cace DKC)							
23	Count							
24	Device address							
25	Device type							
26	Content (x‘6’)				Format (x‘4’)			
27	Operation byte of LR/LRE command parameter							
28	Extension operation byte of LR/LRE command parameter							
29	Head address of extent (DX command parameter)							
2A								
2B								
2C								
2D								
2E	Path group ID (byte 1 to 7 of the ID by the last Set Path Group ID command)							
2F								
30								
31								
32								
33								
34	SSID (Low) of self subsystem							
35								
36	Exception code (x‘0212’)							
37								
38	Log and message control (x‘05’)							
39	Program action code (x‘10’)							
3A	Configuration information							
3B								
3C	Not usde (x‘01’)							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte0D : Bit1 = 1 & Byte36-37 = 0212 (Command Sequence Exception : Incomplete Domain) (2/2)



Copyright ©2000, Hitachi, Ltd.

Byte0D : Bit1 = 1 & Byte36-37 = 4XXX (Data exception) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x‘06’ : Cache DKC)							
23	Count							
24	Device address							
25	Device type (x‘24’ :DKU87I-3)							
26	Content				Format (x‘1’)			
27	Sector number (Note 1)							
28	Cylinder address (Note 1)							
29								
2A	Head address (Note 1)							
2B								
2C	Record number (Note 1)							
2D	Error displacement (Note 1)							
2E								
2F	Drive serial number (x‘0C’) +							
30	(x‘69’) +							
31	(DKU sequence number)							
32								
33								
34	SSID of self subsystem							
35								
36	Exception class (x‘4’)				Message (Note 2)			
37	Correction flag (Note 3)							
38	Log and message control (x‘08’)							
39	Program action code (x‘91’)							
3A	Configuration information							
3B								
3C	Not usde (x‘01’)							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte0D : Bit1 = 1 & Byte36-37 = 4XXX (Data exception) (2/3)

	0	1	2	3	4	5	6	7
40	Causal Key code							
41	Causal Format/Message							
42	Causal Module ID							
43	Causal Routine ID							
44	VDEV number, slot number							
45								
46								
47								
48	Slot status							
49								
4A								
4B								
4C	staging bit map/Dirty bit map							
4D								
4E								
4F								
50	Current subblock number							
51	EXIT falg (Note 4)							
52	Slot failure information (Note 5)							
53	Obtained information flat (Note 6)							
54	Head subblock number for HIT/MISS decision + Remain subblock count							
55	(when byte36 is x‘40/41/42/43’) / PACC in CBUF (when byte36 is x‘45’)							
56	Not used (when byte36 is x‘40/41/42/43’) /							
57	PAHF in CBUF (when byte36 is x‘45’)							
58	Not used (when byte36 is x‘40/41/42/43’) /							
59	Current CC in JCB (when byte36 is x‘45’)							
5A	Not used (when byte36 is x‘40/41/42/43’) /							
5B	Current HH in JCB (when byte36 is x‘45’)							
5C								
	Reserved							
7F								

(Note 1) Not determined for occurrence in HA or RO

(Note 2) Contents of message

- x' 0' : Data check in HA field
- x' 1' : Data check in C field
- x' 2' : Data check in K field
- x' 3' : Data check in D field
- x' 4' : Missing SYNC byte in HA field
- x' 5' : Missing SYNC byte in C field (PA error)
- x' 6' : Missing SYNC byte in K field
- x' 7' : Missing SYNC byte in D field
- x' 8' : Not used
- x' 9' : Missing AM during retry
- x' A' to x' F' : Not used

(Note 3) Contents of correctionflag

- Bits 0 and 1 : ECC correction bit
  - 10 : Correctable (Recoverd)
  - 11 : Uncorrectable
- Bit 2 : offset activ
- Bits 3 to 7 : Not used

Copyright ©2000, Hitachi, Ltd.

Byte0D : Bit1 = 1 & Byte36-37 = 4XXX (Data exception) (3/3)

(Note 4) EXIT flag

x' 08' : CHL I/F CHK2 timeover
x' 0D' : EOF
x' 0E' : DSB=0E requested
x' 0F' : Logical error
x' 1E' : Make sense only
x' 1F' : Logical error (make sense only)
x' 30' : Selective reset requested
x' 40' : ' Staging' requested
x' 41' : ' Waiting free segment' requested
x' 42' : ' Timeover of waiting for staging' requested
x' 43' : ' Staging for PA unmatch' requested
x' 45' : ' Destaging' requested
x' 46' : ' High priority destaging' requested
x' 47' : ' Pseud-through process' requested
x' 4B' : ' DSB=4E retry' requested (data transfer)
x' 4E' : ' DSB=4E retry' requested (DSB=4E retry)
x' 4F' :STG requested (Read or STG in progress)

(Note 5) Slot failure

x' 80' : Sector write error
x' 40' : Sector read error
x' 20' : ECC/LRC error
x' 10' : Incomplete data
x' 08' : No decision

(Note 6) Obtained information flag

bit0-1 : Block type
- 00 : Data block
- 01 : HA/RO block
- 10 : Bit map block

bit2-3 : Side
- 00 : Cache write side
- 01 : NVS write side
- 10 : Cache read side

bit4 : Segment
- 0 :No segment
- 1 :Segment exist

bit5-7 : Reserved

Copyright ©2000, Hitachi, Ltd.

Byte36 = 6F (Subsystem Information) (1/1)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x‘06’ : Cace DKC)							
23	Command overrun threshold exceeded							
24	Device address							
25	Device type							
26	Unit flag	DEV ADR V	TRK ADR V	Unused(0)	Format (x‘1’)			
27	Data overrun hreshold exceeded							
28	Seek count							
29								
2A	Drive serial number (x‘0C’) +							
2B	(x‘69’) +							
2C	(DKU sequence number)							
2D								
2E								
2F	DKC serial number (x‘0C’) +							
30	(x‘69’) +							
31	(x‘00’) +							
32	(DKC sequence number : high) +							
33	(DKC sequence number : low)							
34	SSID of self subsystem							
35								
36	Exception code Y : 0 : Statistics/RRBL command, 2 : Channel data overrun							
37	(x‘6FXY’) X : For serial CHL : LCP#, For parallel CHL : CHL#							
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Read/search byte count							
3F								
40	Not used							
7F								

Copyright ©2000, Hitachi, Ltd.

Byte36 : Bit0-3 = D & Byte26 : Bit4-7 = 1 & Byte27 : Bit0-2 = 7 & Byte40 : Bit7 = 0 (FPC Detected Failure : DSP) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format ID							
07	PCB type		MP number					
08	System error code							
09	(Return Code : Low 2 Byte)							
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPT	ECKD32	SRAID	RCOPY	SEPARAT	HSTREP	HST REP	EXPLS
0E	LDEV#VL	PDEV#VL	SSB#VL	LOG#VL	SIM#VL	RSSB#VL	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x‘06’ : Cache DKC)							
23	Count							
24	Device address							
25	Device type							
26	Unit flag	DEV ADR V	TRK ADR V	0	Format (x‘1’)			
27	Type code (‘111’ : FPC Detected Failure)			0				
28	Not used							
29	Not used							
2A	SCSI command code (See SSBLOG05-4070)							
2B	Threshold type (See SSBLOG05-4070)							
2C	Module ID							
2D	Routine ID							
2E	Not used							
2F	Drive serial number (x‘0C22’) + (DKU sequence number)							
30	This information is not fixed until DKC reports SSB to HOST.							
31								
32								
33								
34	SSID of self subsystem							
35								
36	Exception code (x‘DYZZ’) Y : CDEV number ZZ : RDEV number							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte36 : Bit0-3 = D & Byte26 : Bit4-7 = 1 & Byte27 : Bit0-2 = 7 & Byte40 : Bit7 = 0 (FPC Detected Failure : DSP) (2/2)

	0	1	2	3	4	5	6	7
40	SSB edit format form (x'00')							
41	Not used							
42	CDB							
43								
44								
45								
46								
47								
48								
49								
4A								
4B								
4C	(x'AB')							
4D	(x'CD')							
4E	CMD BLK number							
4F	Data transfer end flag							
50	I/O status							
51								
52	PDEV status							
53								
54	LOOP status							
55								
56								
57								
58	Frame Manager status							
59								
5A								
5B								
5C	TL status							
5D								
5E								
5F								
60	IO issued status 1							
61								
62	IO issued status 2							
63								
64	Not used							
65								
66								
67								
68	JOB require info							
69								
6A								
6B								
6C	Data transfer status							
6D								
6E								
6F								
70	Not used							
71								
72								
73								
74								
75								
76								
77								
78								
79								
7A								
7B								
7C								
7D								
7E								
7F								

Copyright ©2000, Hitachi, Ltd.

Byte36 : Bit0-3 = D & Byte26 : Bit4-7 = 1 & Byte27 : Bit0-2 = 7 & Byte40 : Bit7 = 1 (FPC Detected Failure : FBP) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format ID							
07	PCB type		MP number					
08	System error code							
09	(Return Code : Low 2 Byte)							
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPT	ECKD32	SRAID	RCOPY	SEPARAT	HSTREP	HST REP	EXPLS
0E	LDEV#VL	PDEV#VL	SSB#VL	LOG#VL	SIM#VL	RSSB#VL	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x‘06’)							
23	Count							
24	Device address							
25	Device type							
26	Unit flag	DEV ADR V	TRK ADR V	0	Format (x‘1’)			
27	Type code (‘111’ : FPC Detected Failure)			0				
28	Internal Failure Part							
29								
2A	Not used							
2B	Threshold type							
2C	Module ID							
2D	Routine ID							
2E	Not used							
2F	Drive serial number (x‘0C22’) + (DKU sequence number)							
30	This information is not fixed until DKC reports SSB to HOST.							
31								
32								
33								
34	SSID of self subsystem							
35								
36	Exception code (x‘DYZZ’) Y : CDEV number ZZ : RDEV number							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000,2001, Hitachi, Ltd.

Byte36 : Bit0-3 = D & Byte26 : Bit4-7 = 1 & Byte27 : Bit0-2 = 7 & Byte40 : Bit7 = 1 (FPC Detected Failure : FBP) (2/2)

	0	1	2	3	4	5	6	7
40	SSB edit format form (x'01')							
41	Not used							
42								
43								
44	ERQ index							
45								
46								
47								
48	IMQ index							
49								
4A								
4B								
4C	IO request information							
4D								
4E								
4F								
50	FPC Config/Control register							
51								
52								
53								
54	FPC Status register							
55								
56								
57								
58	FM Configuration register							
59								
5A								
5B								
5C	FM Status register							
5D								
5E								
5F								
60	FM Link Status 1 register							
61								
62								
63								
64	FM Link Status 2 register							
65								
66								
67								
68	FCA register 1							
69								
6A								
6B								
6C	FCA register 2							
6D								
6E								
6F								
70	FPC PCI register							
71								
72	AL_PA							
73								
74	FPC Config Command							
75								
76								
77								
78	Fibre status							
79								
7A								
7B								
7C	Fibre error count							
7D								
7E								
7F								

Copyright ©2000,2001, Hitachi, Ltd.

SCSI command code

Code	Command name
00	TEST UNIT READY
03	REQUEST SENSE
04	FORMAT UNIT
07	REASSIGN BLOCKS
12	INQUIRY
15	MODE SELECT
1A	MODE SENSE
1B	START/STOP UNIT
1C	RECEIVE DIAGNOSTIC RESULT
1D	SEND DIAGNOSTIC
28	READ (EXTEND)
2A	WRITE (EXTEND)
2E	WRITE AND VERIFY
3B	WRITE BUFFER

Threshold type

Code	Threshold (failure) type
40	Fibre port failure
41	Drive mechanism recovered error
42	Drive mechanism unrecovered error
43	Drive media recovered error
44	Drive media unrecovered error
45	Drive R/W recovered error
46	Drive R/W unrecovered error
47	Drive interface recovered error
48	Drive interface unrecovered error
49	Controller recovered error
4A	Controller unrecovered error
4B	Fibre interface recovered error
4C	Fibre interface unrecovered error
4D	Drive I/O read error
4E	Drive I/O write error
FF	Invalid threshold type

Copyright ©2000, Hitachi, Ltd.

Byte36 : Bit0-3 = E & Byte26 : Bit4-7 = 1 & Byte27 : Bit0-2 = 0 (Drive Detected Failure : DSP) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format ID							
07	PCB type		MP number					
08	System error code							
09	(Return COde : Low 2 Byte)							
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPT	ECKD32	SRAID	RCOPY	SEPARAT	HSTREP	HST REP	EXPLS
0E	LDEV#VL	PDEV#VL	SSB#VL	LOG#VL	SIM#VL	RSSB#VL	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x‘06’)							
23	Count							
24	Device address							
25	Device type							
26	Unit flag	DEV ADR V	TRK ADR V	0	Format (x‘1’)			
27	Type code (‘000’ : Driver Detected Failure)			0	Sense key			
28	Additional Sense Code							
29	Additional Sense Code Qualifire							
2A	SCSI command code							
2B	Threshold type							
2C	Module ID							
2D	Routine ID							
2E	Not used							
2F	Drive serial number (x‘0C22’) + (DKU sequence number)							
30	This information is not fixed until DKC reports SSB to HOST.							
31								
32								
33								
34	SSID of self subsystem							
35								
36	Exception code (x‘EYZZ’) Y : CDEV number ZZ : RDEV number							
37								
38	Log and message control (x‘08’)							
39	Program action code (x‘92’)							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte36 : Bit0-3 = E & Byte26 : Bit4-7 = 1 & Byte27 : Bit0-2 = 0 (Drive Detected Failure : DSP) (2/2)

	0	1	2	3	4	5	6	7
40	Not used							
41								
42	CDB							
43								
44								
45								
46								
47								
48								
49								
4A								
4B								
4C	Not used							
4D								
4E								
4F								
50								
51								
52								
53								
54	SCSI extend sense data							
55								
56								
57								
58								
59								
5A								
5B								
5C								
5D								
5E								
5F								
60								
61								
62								
63								
64								
65								
66								
67								
68								
69								
6A								
6B								
6C								
6D								
6E								
6F								
70								
71								
72								
73								
74	Error LBA number							
75								
76								
77								
78	Logical LBA number							
79								
7A								
7B								
7C	Physical LBA number							
7D								
7E								
7F								

Copyright ©2000, Hitachi, Ltd.

Byte36 : Bit0-3 = E & Byte2C : Bit0-7 ≠ 5X/6X (Drive Detected Failure : DSP) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format ID							
07	PCB type		MP number					
08	System error code							
09	(Return Code : Low 2 Byte)							
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPT	ECKD32	SRAID	RCOPY	SEPARAT	HSTREP	HST REP	EXPLS
0E	LDEV#VL	PDEV#VL	SSB#VL	LOG#VL	SIM#VL	RSSB#VL	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x‘06’)							
23	Count							
24	Device address							
25	Device type							
26	Unit flag	DEV ADR V	TRK ADR V	0	Format (x‘1’)			
27	Type code (‘000’ : Driver Detected Failure)			0	Sense key			
28	Additional Sense Code							
29	Additional Sense Code Qualifire							
2A	SCSI command code							
2B	Threshold type							
2C	Module ID (≠ 5X/6X)							
2D	Routine ID							
2E	Not used							
2F	Drive serial number (x‘0C22’) + (DKU sequence number)							
30	This information is not fixed until DKC reports SSB to HOST.							
31								
32								
33								
34	SSID of self subsystem							
35								
36	Exception code (x‘EYZZ’) Y : CDEV number ZZ : RDEV number							
37								
38	Log and message control (x‘08’)							
39	Program action code (x‘92’)							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte36 : Bit0-3 = E & Byte2C : Bit0-7 ≠ 5X/6X (Drive Detected Failure : DSP) (2/2)

	0	1	2	3	4	5	6	7
40	Not used							
41								
42	CDB							
43								
44								
45								
46								
47								
48								
49								
4A								
4B								
4C	Not used							
4D								
4E								
4F								
50								
51								
52								
53								
54	SCSI extend sense data							
55								
56								
57								
58								
59								
5A								
5B								
5C								
5D								
5E								
5F								
60								
61								
62								
63								
64								
65								
66								
67								
68								
69								
6A								
6B								
6C								
6D								
6E								
6F								
70								
71								
72								
73								
74	Error LBA number							
75								
76								
77								
78	Logical LBA number							
79								
7A								
7B								
7C	Physical LBA number							
7D								
7E								
7F								

Copyright ©2000, Hitachi, Ltd.

Blank Sheet

Copyright ©2000, Hitachi, Ltd.

Blank Sheet

Copyright ©2000, Hitachi, Ltd.

Blank Sheet

Copyright ©2000, Hitachi, Ltd.

Blank Sheet

Copyright ©2000, Hitachi, Ltd.

Blank Sheet

Copyright ©2000, Hitachi, Ltd.

Blank Sheet

Copyright ©2000, Hitachi, Ltd.

Blank Sheet

Copyright ©2000, Hitachi, Ltd.

Blank Sheet

Copyright ©2000, Hitachi, Ltd.

Blank Sheet

Copyright ©2000, Hitachi, Ltd.

Byte36 : Bit0-3 = E & Byte2C : Bit0-7 ≠ 5X/6X (Drive Detected Failure : DSP)

(Note 2) Threshold type

Code	Meanning
00	CHA CHK1A failure
01	CHA CHK1B failure
02	CHA CHK3 failure
03	CHA CHK2 failure
04	CHA ADP temporary failure
05	LCM hardware error
06	BSA F bus open
07	BSA LIVEINS
08	BSA check error
09	SMP M bus open
0A	SMP M bus check error
0B	SMP H/L check error
10	DKA CHK1A failure
11	DKA CHK1B failure
12	DKA CHK3 failure
13	DKA SCA temporary failure
14	DKA DRR temporary failure
16	BSA F bus open
17	BSA LIVEINS
18	BSA check error
19	SMP M bus open
1A	SMP M bus check error
1B	SMP H/L check error
20	Shared memory correctable error
21	Shared memory uncorrectable error
22	SMC M bus open
23	SMC H/L bus open
30	Cache one bit correctable error
31	Cache uncorrectable error
32	Cache two bits correctable error
33	CPC check error
40	SCSI port failure
41	Drive recovered error (mechanism)
42	Drive unrecovered error (mechanism)
43	Drive recovered error (media)
44	Drive unrecovered error (media)
45	Drive recovered error (read/write)
46	Drive unrecovered error (read/write)
47	Drive interface recovered error
48	Drive interface unrecovered error
49	Controller recovered error
4A	Controller unrecovered error
4B	SCSI interface recovered error
4C	SCSI interface unrecovered error
4D	Drive I/O read error
4E	Drive I/O write error
60	SVP interface error
FF	Invalid threshold type

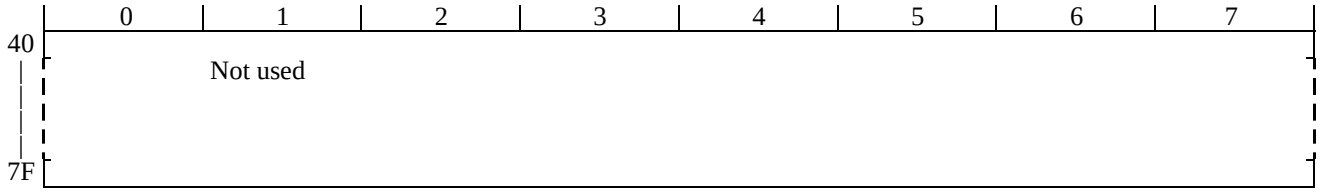
Copyright ©2000, Hitachi, Ltd.

Byte36 = E0 & Byte2C = 5X/6X & Byte20 : Bit3 = 1 (LDEV blokckade/Pin VOL detected/Write inhibited) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x‘06’ : Cace DKC)							
23	Count							
24	Device address							
25	Device type							
26	Unit flag	DEV ADR V	TRK ADR V	Not used		Format (x‘1’)		
27	Type code (b‘000’)			Not used		Not used		
28	Ready	Enable	SSB pending		Not used			
29		Not used						
2A	M.M. RSV	PIN VOL	Write INH		Not used			
2B		Not used						
2C		Module ID (Note 1)						
2D		Routine ID (Note 1)						
2E		Not used						
2F		Drive serial number (x‘0C’) +						
30		(x‘69’) +						
31		(DKU sequence number)						
32								
33								
34		SSID of self subsystem						
35								
36		Exception code (x‘E000’)						
37								
38		Log and message control (x‘08’)						
39		Program action code (x‘92’)						
3A		Configuration information						
3B								
3C		Message code						
3D		Cylinder address						
3E								
3F		Head address						

Copyright ©2000, Hitachi, Ltd.

Byte36 = E0 & Byte 2C = 5X/6X & Byte20 : Bit3 = 1 (LDEV blokckade/Pin VOL detected/Write inhibited) (2/2)



(Note 1) Module ID·Routine ID

x‘5011/501C/5202’	;	LDEV blockade
x‘501A/501B’	;	Pin VOL detected
x‘6605/6697/6705/6784/6805/6853/6909/6953’	;	Write inhibited

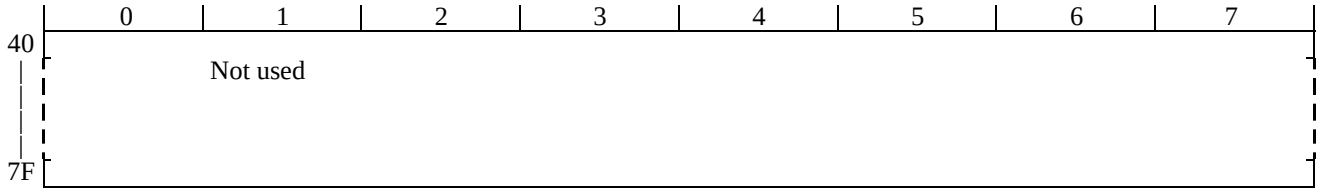
Copyright ©2000, Hitachi, Ltd.

Byte36-37 = E210 & Byte 2C = 5X/6X & Byte20 : Bit1 = 1 (Intervention requested : LDEV not ready) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x‘06’ : Cace DKC)							
23	Count							
24	Device address							
25	Device type							
26	Unit flag	DEV ADR V	TRK ADR V	Not used		Format (x‘2’)		
27	Type code (b‘000’)			Not used		Not used		
28	Ready	Enable	SSB PEND	0	0	0	0	0
29		x‘00’						
2A	M.M RSV	PIN VOL	0	0	0	0	0	0
2B	Host type	DKC type	0	0		DKU type		
2C	Module ID¥ Routine ID							
2D	(x‘501C/5202’ : LDEV not ready)							
2E	Command code							
2F	Drive serial number (x‘0C’) +							
30	(x‘69’) +							
31	(DKU sequence number)							
32								
33								
34	SSID of self subsystem							
35								
36	Exception code (x‘E210’)							
37								
38	Log and message control (x‘01’)							
39	Program action code (x‘02’)							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

Copyright ©2000, Hitachi, Ltd.

Byte36-37 = E210 & Byte 2C = 5X/6X & Byte20 : Bit1 = 1 (Intervention requested : LDEV not ready) (2/2)



Copyright ©2000, Hitachi, Ltd.

Byte26 : Bit4-7 = F & Byte3C = F1 (DKC SIM) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB*							
21								
22	Storage control type (x‘06’ : Cache DKC)*							
23	Count (x‘00’)*							
24	Device address*							
25	Device type*							
26	Content (Note 1)				Format (x‘F’)			
27	SIM sense record ID (x‘E0’)							
28	Range subject to the error (Note 2)				Range affected by repair (Note 3)			
29	Failure level (Note 4)		Failure SPs (Note 5)	SPs in SSID (Note 6)	Failure SSIDs (Note 7)	Affected SSIDs (Note 8)	Status (Note 9)	0
2A	Resent SIM (Note 10)	‘0000000’						
2B	Hardware level (Note 11)							
2C								
2D	Isoration code (Note 12)							
2E	SSB ID (Note 13)	SIM sequence number						SVP ID (Note 14)
2F	DKC serial number(x‘0C’) +							
30	(x‘69’) +							
31	(x‘00’) +							
32	(DKC sequence number : high) +							
33	(DKC sequence number : low)*							

* : This information is not fixed until DKC reports SIM to HOST.

Copyright ©2000, Hitachi, Ltd.

Byte26 : Bit4-7 = F & Byte3C = F1 (DKC SIM) (2/3)

	0	1	2	3	4	5	6	7	
34	SSID of self subsystem								
35									
36	Exception code (See " Reference code " table)								
37									
38	Log and message control (Note 15')*								
39	Program action code (x'10')*								
3A	Dual frame	EDCC mode	0	0	NONSYNC operation	Seial channel	Report output	Permanent path ERR	*
3B	32Byte SSB (0)	0	0	0	0	Extended path	Storage path number		*
3C	SIM message code (x'F1')								
3D	Affected SSID*								
3E									
3F	Not used								
40	Not used								
7F									

* : This information is not fixed until DKC reports SIM to HOST.

(Note 1) Content
- bit0 : Serial number valid (0:Invalid,1:Valid)
- bit1 : Device address valid (0:Invalid,1:Valid)
- bit2 : Track address valid (0:Invalid,1:Valid)
- bit3 : Not used (0)

(Note 2) Range subject to the error
- x'0' : Not used
- x'1' : Error range not known
- x'2' : SP error
- x'3' : CHL-I error
- x'4' : Not affect performance
- x'5~F' : Not used

(Note 3) Range affecte by repair
- x'0' : Not used
- x'1' : Repair range not known
- x'2' : Repair dose not affect performance
- x'3' : SP disabled during repair
- x'4' : SSID disabled during repair
- x'5~F' : Not used

(Note 4) Failure level
- 00 : Service Alert
- 01 : Moderate Alert
- 10 : serious Alert
- 11 : Acute Alert

(Note 5) Failure SPs
- 0 : 1SP
- 1 : 2SP

(Note 6) SPs in SSID
- 0 : 2SP
- 1 : 4SP

(Note 7) Failure SSIDs
- 0 : 1SSID
- 1 : 2SSID

(Note 8) Affected SSIDs
- 0 : 1SSID
- 1 : 2SSID

(Note 9) Status
- 0 : Reduction
- 1 : Stop

(Note 10) Resent SIM
- 0 :Unresent SIM
- 1 : Resent SIM

Copyright ©2000, Hitachi, Ltd.

Byte26 : Bit4-7 = F & Byte3C = F1 (DKC SIM) (3/3)

(Note 11) Hardware level

① When bit 0 is 0.

Bit 1 : Not used
Bit 2-3 : SP number
Bit 4-5 : CHLs PER CLUSTER
- 00 : 4
- 01 : 8
- 10 : Not used
- 10 : Not used
- 11 : Not used

Bit 6 :NVS
- 0 : Without NVS
- 1 : With NVS

Bit 8-10 : Cache size
- 000 : Non cache
- 001 : 256MB
- 010 : 512MB
- 011 : 768MP
- 100 : 1024MB
- 101 : 1280MB
- 110 : 1536MB
- 111 : Over 1536MB

Bit 11-13 : Cluster hardware level (‘000’)
Bit 14-15 : Cache/NVS hardware level (‘000’)

② When bit 0 is 1,

Bit 1 : Not used
Bit 2-3 : SP number
Bit 4-5 : CHLs per cluster
- 0000 : Parallel=4, serial=0
- 0001 : Parallel=8, serial=0
- 0010 : Parallel=4, serial=2
- 0100 : Parallel=4, serial=4
- 0110 : Parallel=0, serial=2
- 1000 : Parallel=0, serial=4
- 1010 : Parallel=0, serial=8
- 1100 : Parallel=0, serial=6

Bit 8 : Dual frame
- 0 : Dual frame
- 1 : Single frame

Bir 9-11 : Cache size
- 000 : Non cache
- 001 : 256MB
- 010 : 512MB
- 011 : 768MB
- 100 : 1024MB
- 101 : 1280MB
- 110 : 1536MB
- 111 : Over 1536MB

Bit 12-13 : Cluster hardware level (‘00’)
Bit 14-15 : Cache/NVS hardware level (‘00’)

(Note 12) Isolation code

Byte 2D ≠ x’ 00’ : Byte 36 and 37 are a sympton code.
Byte 2D = x’ 00’ : Byte 36 and 37 are a sympton code.
This byte is byte 2 of the isorarion code.

(Note 13) SSB ID

0 : SVP
1 : SP

(Note 14) SVP ID

0 : SVP1
1 : SVP2

(Note 15) Log and message control

bit 0-2 : Not used
bit 3 : Log mode (0)
bit 4-5 : Logging action
- 00 :Don’t log
- 01 : Unconditional log
- 10 : Log only once
- 11 : Log only if persistent

bit 6-7 : Operator message
- 00 : No message
- 01 : Unconditional message
- 10 : Send only once
- 11 : Send only if persistent

Copyright ©2000, Hitachi, Ltd.

Byte26 : Bit4-7 = F & Byte3C = F2 (CACHE SIM) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB*							
21								
22	Storage control type (x‘06’ : Cache DKC)*							
23	Count (x‘00’)*							
24	Device address*							
25	Device type*							
26	Content (Note 1)				Format (x‘F’)			
27	SIM sense record ID (x‘E0’)							
28	Range subject to the error (Note 2)				Range affected by repair (Note 3)			
29	Failure level (Note 4)		Failure Sps (Note 5)	Sps in SSID (Note 6)	Failure SSIDs (Note 7)	Affected SSIDs (Note 8)	Status (Note 9)	0
2A	Resent SIM (Note 10)	‘0000000’						
2B	Hardware level (Note 11)							
2C								
2D	Isoration code (Note 12)							
2E	SSB ID (Note 13)	SIM sequence number						SVP ID (Note 14)
2F	DKC serial number(x‘0C’) + (x‘69’) + (x‘00’) + (DKC sequence number : high) + (DKC sequence number : low)*							
30								
31								
32								
33								

* : This information is not fixed until DKC reports SIM to HOST.

Copyright ©2000, Hitachi, Ltd.

Byte26 : Bit4-7 = F & Byte3C = F2 (CACHE SIM) (2/3)

	0	1	2	3	4	5	6	7	
34	SSID of self subsystem								
35									
36	Exception code (See " Reference code" table)								
37									
38	Log and message control (Note 15')*								
39	Program action code (x'10')*								
3A	Dual frame	EDCC mode	0	0	NONSYNC operation	Seial channel	Report output	Permanent path ERR	*
3B	32Byte SSB (0)	0	0	0	0	Extended path	Storage path number		*
3C	SIM message code (x'F1')								
3D	Affected SSID*								
3E									
3F	Not used*								
40	Not used								
7F									

* : This information is not fixed until DKC reports SIM to HOST.

(Note 1) Content
- bit0 : Serial number valid (0:Invalid,1:Valid)
- bit1 : Device address valid (0:Invalid,1:Valid)
- bit2 : Track address valid (0:Invalid,1:Valid)
- bit3 : Not used (0)

(Note 2) Range subject to the error
- x'0' : Not used
- x'1' : Error range not known
- x'2' : SP error
- x'3' : CHL-I error
- x'4' : Not affect performance
- x'5~F' : Not used

(Note 3) Range affecte by repair
- x'0' : Not used
- x'1' : Repair range not known
- x'2' : Repair dose not affect performance
- x'3' : SP disabled during repair
- x'4' : SSID disabled during repair
- x'5~F' : Not used

(Note 4) Failure level
- 00 : Service Alert
- 01 : Moderate Alert
- 10 : serious Alert
- 11 : Acute Alert

(Note 5) Failure SPs
- 0 : 1SP
- 1 : 2SP

(Note 6) SPs in SSID
- 0 : 2SP
- 1 : 4SP

(Note 7) Failure SSIDs
- 0 : 1SSID
- 1 : 2SSID

(Note 8) Affected SSIDs
- 0 : 1SSID
- 1 : 2SSID

(Note 9) Status
- 0 : Reduction
- 1 : Stop

(Note 10) Resent SIM
- 0 :Unresent SIM
- 1 : Resent SIM

Copyright ©2000, Hitachi, Ltd.

Byte26 : bit4-7 = F & Byte3C = F2 (CACHE SIM) (3/3)

(Note 11) Hardware level

① When bit 0 is 0.

Bit 1 : Not used
Bit 2-3 : SP number
Bit 4-5 : CHLs PER CLUSTER
- 00 : 4
- 01 : 8
- 10 : Not used
- 10 : Not used
- 11 : Not used

Bit 6 :NVS
- 0 : Without NVS
- 1 : With NVS

Bit 8-10 : Cache size
- 000 : Non cache
- 001 : 256MB
- 010 : 512MB
- 011 : 768MP
- 100 : 1024MB
- 101 : 1280MB
- 110 : 1536MB
- 111 : Over 1536MB

Bit 11-13 : Cluster hardware level (‘000’)
Bit 14-15 : Cache/NVS hardware level (‘000’)

② When bit 0 is 1,

Bit 1 : Not used
Bit 2-3 : SP number
Bit 4-5 : CHLs per cluster
- 0000 : Parallel = 4, serial = 0
- 0001 : Parallel = 8, serial = 0
- 0010 : Parallel = 4, serial = 2
- 0100 : Parallel = 4, serial = 4
- 0110 : Parallel = 0, serial = 2
- 1000 : Parallel = 0, serial = 4
- 1010 : Parallel = 0, serial = 8
- 1100 : Parallel = 0, serial = 6

Bit 8 : Dual frame
- 0 : Dual frame
- 1 : Single frame

Bir 9-11 : Cache size
- 000 : Non cache
- 001 : 256MB
- 010 : 512MB
- 011 : 768MB
- 100 : 1024MB
- 101 : 1280MB
- 110 : 1536MB
- 111 : Over 1536MB

Bit 12-13 : Cluster hardware level (‘00’)
Bit 14-15 : Cache/NVS hardware level (‘00’)

(Note 12) Isolation code

Byte 2D ≠ x‘00’ : Byte 36 and 37 are a sympton code.
Byte 2D = x‘00’ : Byte 36 and 37 are a sympton code.
This byte is byte 2 of the isorarion code.

(Note 13) SSB ID

0 : SVP
1 : SP

(Note 14) SVP ID

0 : SVP1
1 : SVP2

(Note 15) Log and message control

bit 0-2 : Not used
bit 3 : Log mode (0)
bit 4-5 : Logging action
- 00 :Don’t log
- 01 : Unconditional log
- 10 : Log only once
- 11 : Log only if persistent

bit 6-7 : Operator message
- 00 : No message
- 01 : Unconditional message
- 10 : Send only once
- 11 : Send only if persistent

Copyright ©2000, Hitachi, Ltd.

Byte26 : Bit4-7 = F & Byte3C = FE (Device SIM) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB*							
21								
22	Storage control type (x‘06’ : Cache DKC)*							
23	Count (x‘00’)*							
24	Device address*							
25	Device type*							
26	Content (Note 1)				Format (x‘F’)			
27	SSB ID (Note 2)	SIM sequence number						SVP ID (Note 3)
28	Device exception (x‘1’)				Service message (x‘1’ : Action, x‘C’ : No action)			
29	Failure level (Note 4)		‘000000’					
2A	Resent SIM (Note 5)	‘0000000’						
2B	Exception class FRU list code (x‘80’)							
2C	Harware and microcode corequisite indicator (x‘01’)							
2D	Device address (See reference code)							
2E	Action flag (x‘05’)							
2F	Drive serial number* (x‘0C’) + (x‘69’) + (DKU sequence number)							
30								
31								
32								
33								

* : This information is not fixed until DKC reports SIM to HOST.

Copyright ©2000, Hitachi, Ltd.

Byte26 : Bit4-7 = F & Byte3C = FE (Device SIM) (2/2)

	0	1	2	3	4	5	6	7	
34	SSID of self subsystem								
35									
36	Exception code (See " Reference code" table)								
37									
38	Log and message control (Note 6')*								
39	Program action code (x'10')*								
3A	Dual frame	EDCC mode	0	0	NONSYNC operation	Seial channel	Report output	Permanent path ERR	*
3B	32Byte SSB (0)	0	0	0	0	Extended path	Storage path number		*
3C	SIM message code (x'FE')								
3D	Affected SSID*								
3E									
3F	Not used*								
40	Not used								
7F									

* : This information is not fixed until DKC reported SIM to HOST.

(Note 1) Content

bit0 : Serial number valid (0:Invalid,1:Valid)
bit1 : Device address valid (0:Invalid,1:Valid)
bit2 : Track address valid (0:Invalid,1:Valid)
bit3 : Not used (0)

(Note 2)SSB ID

0 : SVP
1 : SP

(Note 3) SVP ID

0 : SVP1
1 : SVP2

(Note 4) Failure level

00 : Service Alert
01 : Moderate Alert
10 : serious Alert
11 : Acute Alert

(Note 5) Resent SIM

0 : Unresent SIM
1 : Resent SIM

(Note 6) Log and message control

bit 0-2 : Not used
bit 3 : Log mode (0)
bit 4-5 : Logging action
00 :Don't log
01 : Unconditional log
10 : Log only once
11 : Log only if persistent
bit 6-7 : Operator message
00 : No message
01 : Unconditional message
10 : Send only once
11 : Send only if persistent

Copyright ©2000, Hitachi, Ltd.

Byte26 : Bit4-7 = F & Byte3C = FF (Media SIM) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB*							
21								
22	Storage control type (x‘06’ : Cache DKC)*							
23	Count (x‘00’)*							
24	Device address*							
25	Device type*							
26	Content (Note 1)				Format (x‘F’)			
27	SSB ID (Note 2)	SIM sequence number						SVP ID (Note 3)
28	Device exception (x‘1’)				Service message (x‘1’)			
29	Failure level (Note 4)	Media maintenance procedure number (Correctable : x‘07’, Uncorrectable : x‘05’)						
2A	Resend SIM (Note 5)	‘0000000’						
2B	Exception class FRU list code (x‘80’)							
2C	Harware and microcode corequisite indicator (x‘01’)							
2D	Device address (See reference code)							
2E	Action flag (Correctable : x‘87’ , Uncorrectable : x‘85’)							
2F	Drive serial number* (x‘0C’) + (x‘69’) + (DKU sequence number)							
30								
31								
32								
33								

* : This information is not fixed until DKC reports SIM to HOST.

Copyright ©2000, Hitachi, Ltd.

Byte26 : Bit4-7 = F & Byte3C = FF (Media SIM) (2/2)

	0	1	2	3	4	5	6	7	
34	SSID of self subsystem								
35									
36	Exception code (See “Reference code” table)								
37									
38	Log and message control (Note 6’)*								
39	Program action code (x‘10’)*								
3A	Dual frame	EDCC mode	0	0	NONSYNC operation	Seial channel	Report output	Permanent path ERR	*
3B	32Byte SSB (0)	0	0	0	0	Extended path	Storage path number		*
3C	SIM message code (x‘FF’)								
3D	Cylinder addres*								
3E									
3F	Head address*								
40	Not used								
7F									

* : This information is not fixed until DKC reports SIM to HOST.

(Note 1) Content

bit0 : Serial number valid (0:Invalid,1:Valid)
bit1 : Device address valid (0:Invalid,1:Valid)
bit2 : Track address valid (0:Invalid,1:Valid)
bit3 : Not used (0)

(Note 2) SSB ID

0 : SVP
1 : SP

(Note 3) SVP ID

0 : SVP1
1 : SVP2

(Note 4) Failure level

00 : Service Alert
01 : Moderate Alert
10 : serious Alert
11 : Acute Alert

(Note 5) Resent SIM

0 : Unresent SIM
1 : Resent SIM

(Note 6) Log and message control

bit 0-2 : Not used
bit 3 : Log mode (0)
bit 4-5 : Logging action
00 :Don’t log
01 : Unconditional log
10 : Log only once
11 : Log only if persistent
bit 6-7 : Operator message
00 : No message
01 : Unconditional message
10 : Send only once
11 : Send only if persistent

Copyright ©2000, Hitachi, Ltd.

SIM Reference Codes Detected by the Processor (1/7)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		36	37	2D	3C			
LCP/FCP error	LCM Hardware error	21	3Z	XY	F1	Moderate	Yes	X: CHA PCB# (*1) Y: LCP#1 (*3) Z: LCP#2 (*3)
	ADP permanent error	21	70	X0	F1	Moderate	Yes	X: CHA PCB# (*1)
	ADP temporary error	21	71	XY	F1	Service	No	X: CHA PCB# (*1) Y: LCP#0 (*3)
	ADP blocking	21	72	XY	F1	Moderate	Yes	X: CHA PCB# (*1) Y: LCP#0 (*3)
	AL_PA value conflict	21	90	XY	F1	Service	No	X: CHA PCB# (*1) Y: PORT# in PCB
CHA Processor error	CHK1A threshold over	30	70	XY	F1	Service	No	X: CHA PCB# (*1) Y: MP# in PCB
	CHK1B threshold over	30	71	XY	F1	Service	No	X: CHA PCB# (*1) Y: MP# in PCB
	CHK3 threshold over	30	72	XY	F1	Service	No	X: CHA PCB# (*1) Y: MP# in PCB
	Processor blocking	30	73	XY	F1	Moderate	Yes	X: CHA PCB# (*1) Y: MP# in PCB
	FM threshold over	30	74	XY	F1	Service	No	X: CHA PCB# (*1) Y: MP# in PCB
	FM error	30	75	XY	F1	Moderate	Yes	X: CHA PCB# (*1) Y: MP# in PCB
	Incorrect SUM value of FM	30	76	XY	F1	(*27)	No	X: CHA PCB# (*1) Y: MP# in PCB
	LDEV blockade (Effect of processor blockade)	30	90	XY	F1	Serious	Yes	X: CHA PCB# (*1) Y: MP# in PCB
	P/S OFF impossible	38	8F	00	F1	Moderate	No	
	P/S OFF impossible (Device reserved)	38	9F	00	F1	Moderate	No	
	Undefined Package is mounted	39	90	XY	F1	Moderate	No	X: CHA PCB# (*1,5) Y: MP# in PCB
	V-R or serial number is inconsistent	39	91	XY	F1	Moderate	No	X: CHA PCB# (*1) Y: MP# in PCB
	Replace failed	39	93	XY	F1	Moderate	No	X: CHA PCB# (*1) Y: MP# in PCB
	Micro-program version up	39	94	X0	F1	Service	No	X: MP version after replacing (*23)
	Micro-program version up impossible	39	95	XY	F1	Service	No	X: Present MP version (*23) Y: reason code (*13)

Copyright ©2000, Hitachi, Ltd.

SIM Reference Codes Detected by the Processor (2/7)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		36	37	2D	3C			
CHA Processor error	Warning of SM DISABLE (MPA detected)	39	9A	XY	F1	Moderate	No	X: CHA PCB# (*1) Y: 0 = Side A, 1 = Side B (*2)
	SMA slave error	39	9B	XY	F1	Moderate	No	X: CHA PCB# (*1) Y: MP# in PCB
	MPA slave error	39	9C	XY	F1	Moderate	No	X: CHA PCB# (*1) Y: MP# in PCB
	Injustice DC voltage control	39	9D	X0	F1	Moderate	No	X: CHA PCB# (*1)
	Injustice CE MODE	39	9E	X0	F1	Moderate	No	X: CHA PCB# (*1)
	CHT PCB exchange impossible (4GL ↔ 4GS)	39	9F	X0	F1	Moderate	No	X: CHA PCB# (*1)

Copyright ©2000, Hitachi, Ltd.

SIM Reference Codes Detected by the Processor (3/7)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		36	37	2D	3C			
DKA Processor error	CHK1A threshold over	31	70	XY	F1	Service	No	X: DKA PCB# (*1) Y: MP# in PCB
	CHK1B threshold over	31	71	XY	F1	Service	No	X: DKA PCB# (*1) Y: MP# in PCB
	CHK3 threshold over	31	72	XY	F1	Service	No	X: DKA PCB# (*1) Y: MP# in PCB
	Processor blocking	31	73	XY	F1	Moderate	Yes	X: DKA PCB# (*1) Y: MP# in PCB
	FM threshold over	31	74	XY	F1	Service	No	X: DKA PCB# (*1) Y: MP# in PCB
	FM error	31	75	XY	F1	Moderate	Yes	X: DKA PCB# (*1) Y: MP# in PCB
	Incorrect SUM value of FM	31	76	XY	F1	(*27)	No	X: DKA PCB# (*1) Y: MP# in PCB
	LDEV blockade (Effect of processor blockade)	31	90	XY	F1	Serious	Yes	X: DKA PCB# (*1) Y: MP# in PCB
	P/S OFF impossible	3C	8F	00	F1	Moderate	No	
	P/S OFF impossible (Device reserved)	3C	9F	00	F1	Moderate	No	
	Undefined Package is mounted	3D	90	XY	F1	Moderate	No	X: DKA PCB# (*1,5) Y: MP# in PCB
	V-R or serial number is inconsistent	3D	91	XY	F1	Moderate	No	X: DKA PCB# (*1) Y: MP# in PCB
	Replace failed	3D	93	XY	F1	Moderate	No	X: DKA PCB# (*1) Y: MP# in PCB
	Micro-program version up	3D	94	X0	F1	Service	No	X: MP version after replacing (*23)
	Micro-program version up impossible	3D	95	XY	F1	Service	No	X: Present MP version (*23) Y: reason code (*13)
	Warning of SM DISABLE (MPA detected)	3D	9A	XY	F1	Moderate	No	X: DKA PCB# (*1) Y: 0 = Side A, 1 = Side B (*2)
	SMA slave error	3D	9B	XY	F1	Moderate	No	X: DKA PCB# (*1) Y: MP# in PCB
	MPA slave error	3D	9C	XY	F1	Moderate	No	X: DKA PCB# (*1) Y: MP# in PCB
	Injustice DC voltage control	3D	9D	X0	F1	Moderate	No	X: DKA PCB# (*1)
	Injustice CE MODE	3D	9E	X0	F1	Moderate	No	X: DKA PCB# (*1)
	FSW LED BUS test	3D	AZ	XY	FE	Moderate	No	X: DKA PCB# (*1) Y: MP# in PCB Z: FSW PCB#
	Tachyon error	3D	B0	XY	FE	Service	No	X: DKA PCB# (*1) Y: MP# in PCB
SHSN error	Logical path blockade (CHA Processor)	32	8Z	XY	F1	Moderate	No	X: CHA PCB# (*1,31) Y: MP# in PCB Z: PATH# 0: A0 PATH 1: A1 PATH 2: B0 PATH 3: B1 PATH

Copyright ©2000, Hitachi, Ltd.

SIM Reference Codes Detected by the Processor (4/7)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		36	37	2D	3C			
SHSN error	Logical path blockade (DKA Processor)	33	8Z	XY	F1	Moderate	No	X: DKA PCB# (*1,31) Y: MP# in PCB Z: PATH# 0: A0 PATH 1: A1 PATH 2: B0 PATH 3: B1 PATH
CHSN error	Logical path blockade (CHA Processor/CARB0)	32	0Z	XY	F1	Moderate	No	X: CHA PCB# (*1,29) Y: MP# in PCB Z: C path bitmap
	Logical path blockade (CHA Processor/CARB1)	32	1Z	XY	F1	Moderate	No	X: CHA PCB# (*1,29) Y: MP# in PCB Z: C path bitmap
	Logical path blockade (CHA/PMA/CARB0)	32	4Z	XY	F1	Moderate	No	X: CHA PCB# (*1,29) Y: MP# in PCB Z: C path bitmap
	Logical path blockade (CHA/PMA/CARB1)	32	5Z	XY	F1	Moderate	No	X: CHA PCB# (*1,29) Y: MP# in PCB Z: C path bitmap
	Logical path blockade (DKA/DRR/CARB0)	33	0Z	XY	F1	Moderate	No	X: DKA PCB# (*1,29) Y: MP# in PCB Z: C path bitmap
	Logical path blockade (DKA/DRR/CARB1)	33	1Z	XY	F1	Moderate	No	X: DKA PCB# (*1,29) Y: MP# in PCB Z: C path bitmap
	Logical path blockade (DKA/FCA/CARB0)	33	2Z	XY	F1	Moderate	No	X: DKA PCB# (*1,29) Y: MP# in PCB Z: C path bitmap
	Logical path blockade (DKA/FCA/CARB1)	33	3Z	XY	F1	Moderate	No	X: DKA PCB# (*1,29) Y: MP# in PCB Z: C path bitmap
CHA, CHK2 (processor)	RCHA temporary error	3F	84	X0	F1	Service	No	X: CHA PCB# (*1)
	RCHA blocking	3F	85	X0	F1	Serious	Yes	X: CHA PCB# (*1)
DKA CHK2 (processor)	Pinned slot	CF	4X	YY	F1	Moderate	No	X: CU# YY: LDEV#
	DRR temporary error	CF	80	XY	F1	Service	No	X: DKA PCB# (*1) Y: MP# in PCB
	FCA temporary error	CF	81	XY	F1	Service	No	X: DKA PCB# (*1) Y: Port# (*4)
	DRR blocking	CF	82	XY	F1	Moderate	Yes	X: DKA PCB# (*1) Y: MP# in PCB
	FCA blocking (0-3)	CF	83	XY	F1	Moderate	Yes	X: DKA PCB# (*1) Y: Port# (*4)
	Fibre port blocking (Effect of PATH INLINE failed)	CF	84	XY	F1	Moderate	No	X: DKA PCB# (*1) Y: Port# (*4)
	LDEV blockade (Effect of FCA blockade)	CF	90	XY	F1	Serious	Yes	X: DKA PCB# (*1) Y: Port# (*4)

Copyright ©2000,2001, Hitachi, Ltd.

SIM Reference Codes Detected by the Processor (5/7)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		36	37	2D	3C			
Cache data error	Pinned slot	FF	4X	YY	F2	Moderate	No	X: CU# YY: LDEV#
Cache error	Area is volatiled	FF	CD	0X	F2	Service	No	X: 0 = Side A, 1 = Side B (*2)
	Package is volatiled	FF	CE	0X	F2	Service	No	X: PCB# (*1) Side A:Even, Side B:Odd
	Module group is volatiled	FF	CF	YX	F2	Service	No	X: PCB# (*1) Side A:Even, Side B:Odd Y: Module group# (*10)
	Correctable error	FF	F0	YX	F2	Service	No	X: PCB# (*1) Side A:Even, Side B:Odd Y: Module group# (*10)
	Cache temporary error	FF	F1	YX	F2	Service	Yes	X: PCB# (*1) Side A:Even, Side B:Odd Y: Module group# (*10)
	Module group blocking	FF	F2	YX	F2	Moderate	Yes	X: PCB# (*1) Side A:Even, Side B:Odd Y: Module group# (*10)
	Package blocking	FF	F3	0X	F2	Moderate	Yes	X: PCB# (*1) Side A:Even, Side B:Odd
	Area blocking	FF	F4	0X	F2	Serious	Yes	X: 0 = Side A, 1 = Side B (*2)
	Both area failed	FF	F5	0X	F2	Moderate	No	X: PCB# (*1) Side A:Even, Side B:Odd
	Injustice DC voltage control	FF	F6	0X	F2	Moderate	No	X: PCB# (*1) Side A:Even, Side B:Odd
	Injustice CE MODE	FF	F7	0X	F21	Moderate	No	X: PCB# (*1) Side A:Even, Side B:Odd
	Module group error in On-demand area	FF	FD	YX	F2	Moderate	No	X: PCB# (*1) Y: Module group#
Shared memory error	Loss of duplicated information	FF	DE	XX	F1	Service	No	XX: Lost information type (*25)
	One side Area is volatiled	FF	DF	0X	F1	Service	No	X: 0 = Side A, 1 = Side B (*2)
	Correctable error	FF	E0	YX	F1	Service	No	X: 0 = Side A, 1 = Side B Y: Module# (*2,10)
	Uncorrectable error	FF	E1	0X	F1	Service	Yes	X: 0 = Side A, 1 = Side B (*2,10)
	Area blocking	FF	E2	0X	F1	Serious	Yes	X: 0 = Side A, 1 = Side B (*2,10)
	Real memory size inconsistent	FF	E3	XY	F1	Serious	No	X:Number of module (side A) Y:Number of module (side B) (*8)
	Replace failed (*20)	FF	E4	0X	F1	Serious	No	X: 0 = Side A, 1 = Side B (*2)
	Both side invalid	FF	E5	00	F1	Acute	No	
	Configuration information compare error (*22)	FF	E6	00	F1	Acute	No	
	Shared memory is volatiled.	FF	E7	00	F1	Serious	No	
	Configration unmatch	FF	E8	00	F1	Acute	No	
	“DKCMAIN” micro lost	FF	E9	00	F1	Serious	No	(*30)
	CHK3 threshold over	FF	EC	0X	F1	Service	No	X: 0 = Side A, 1 = Side B (*2)
	Area temporary blocking (*19)	FF	EE	0X	F1	Service	Yes	X: 0 = Side A, 1 = Side B (*2)
	Rebooted without volatilization after an instantaneous down	FF	EF	00	F1	Service	No	
	Module error in On-demand area	FF	ED	YX	F1	Service	No	X: 0 = Side A, 1 = Side B (*2) Y: Module#

Copyright ©2000, Hitachi, Ltd.

SIM Reference Codes Detected by the Processor (6/7)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		36	37	2D	3C			
Drive error (normal R/W)	Drive port temporary error (Drive path: Boundary 0)	DF	6X	XX	FE	Service (*32)	No	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive port temporary error (Drive path: Boundary 1)	DF	7X	XX	FE	Service (*32)	No	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive temporary error	EF	AX	XX	FE	Service (*32)	No	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive media error	43	4X	XX	FF	Service (*32)	No	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive port blockade (Drive path: Boundary 0)	DF	8X	XX	FE	Moderate (*32)	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive port blockade (Drive path: Boundary 1)	DF	9X	XX	FE	Moderate (*32)	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	LDEV blockade (Drive path: Boundary 0/ Effect of SCSI blockade) *15	DF	AX	XX	FE	Serious	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	LDEV blockade (Drive path: Boundary 1/ Effect of SCSI blockade) *15	DF	BX	XX	FE	Serious	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive blockade (drive)	EF	1X	XX	FE	Serious	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive blockade (Effect of Dynamic sparing normal end)	EF	2X	XX	FE	Service	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	LDEV blockade (Effect of drive blockade) *15	EF	9X	XX	FE	Serious	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive blockade (media)	43	CX	XX	FF	Serious	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Correction copy start *7	45	1X	XX	FE	Service	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b) (Source side drive)
	Correction copy normal end *7	45	2X	XX	FE	Service	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b) (Source side drive)
	Correction copy abnormal end *7	45	3X	XX	FE	Serious	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b) (Source side drive)
	Correction copy discontinued *7	45	4X	XX	FE	Service	No	XXX: Drive number (CDEV#:4b+RDEV#:8b) (Source side drive)
	Correction copy warning end* *7 (With blockade LDEV or some error)	45	5X	XX	FE	Service	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b) (Source side drive)
	Dynamic sparing start *7 (Drive copy)	46	1X	XX	FE	Service	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b) (Source side drive)
	Dynamic sparing normal end *7 (Drive copy)	46	2X	XX	FE	Service	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b) (Source side drive)

Copyright ©2000, Hitachi, Ltd.

SIM Reference Codes Detected by the Processor (7/7)

Error			REF CODE 36	37	2D	SIM 3C	Level of error	Host report	Remarks
Drive error (normal R/W)	Dynamic sparing abnormal end (Drive copy) *7		46	3X	XX	FE	Moderate	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b) (Source side drive)
	Dynamic sparing discontinued *7		46	4X	XX	FE	Service	No	XXX: Drive number (CDEV#:4b+RDEV#:8b) (Source side drive)
	Dynamic sparing warning end* (With blockade LDEV or some error) (Drive copy) *7		46	5X	XX	FE	Service	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b) (Source side drive)
	Pinned slot		EF	4X	YY	FE	Moderate	No	X: CU# YY: LDEV#
Drive error (ORM)	Drive port temporary error (Drive path: Boundary 0)		50	0X	XX	FE	Service	No	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive port temporary error (Drive path: Boundary 1)		50	1X	XX	FE	Service	No	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive temporary error		50	2X	XX	FE	Service	No	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive media error		50	3X	XX	FF	Service	No	XXX: Drive number (CDEV#:4b+RDEV#:8b)
CSW error	Injustice DC voltage control		FF	20	0X	F1	Moderate	No	X: CSW PCB# (*1)
	Injustice CE MODE		FF	21	0X	F1	Moderate	No	X: CSW PCB# (*1)
SVP interface error (CHA side)	Ethernet error for SVP		14	00	X0	F1	Moderate	Yes	X: CHA PCB# (*1)
	SIM transfer failure to SVP		14	01	X0	F1	Serious	Yes	X: CHA PCB# (*1)
SVP interface error (DKA side)	Ethernet error for SVP		15	00	X0	F1	Moderate	Yes	X: DKA PCB# (*1)
	SIM transfer failure to SVP		15	01	X0	F1	Serious	Yes	X: DKA PCB# (*1)
Power error	Separate Model	HDU power off	AC	50	XY	F1	Moderate	Yes	X: DKU number (*12) Y: HDU number (*12)
		HDU power recovered	AC	51	XY	F1	Service	No	X: DKU number (*12) Y: HDU number (*12)
	Single Cabinet Model	HDU power off	AC	50	0X	F1	Moderate	Yes	X: HDU number
		HDU power recovered	AC	51	0X	F1	Service	No	X: HDU number
	When DKC was set to power error mode, Urgent Destaging start succeeded.		AC	62	00	F1	Service	No	
	When DKC was set to power error mode, Urgent Destaging start failed.		AC	63	00	F1	Moderate	No	
Server error	NAS error (SGI) notice		AC	80	XX	F1	Service	Yes	XX: Error code

* : Warning end : (1) LDEV blockade status is detected, and copy process for the LDEV is skipped.

(2) Some failure is detected, and copy process is complete.

** : When the drive is 3880 emulation mode, the SIM is not reported to host.

*** : The SIM is not reported to SVP.

Copyright ©2000,2001, Hitachi, Ltd.

A three-byte reference code (RC) is provided for a SIM (Service Information Message) to identify an error and error section.

The following shows 32 SIM bytes and reference code.

Byte	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
SIM SSB	00	90	10	00	00	00	8F	E0	44	10	00	04	00	80	04	0C	69	00	00	00	00	02	30	00	05	10	42	0C	F1	00	02	00

Indecates SIM

RC=3000-XXXX-80XX

SIM type
F1 : DKC SIM
F2 : CACHE SIM
FE : DEVICE SIM
FF : MEDIA SIM

Copyright ©2000, Hitachi, Ltd.

SIM Reference Codes Detected by the Processor for HRC/HODM (1/2)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		36	37	2D	3C			
LCP/FCP error (Remote Control Port)	Logical path(s) on the remote copy connections was logically blocked (Due to an error conditions)	21	80	XY	F1	Moderate	Yes	X: CHA PCB# (*1) Y: LCP#1 (*3)
	The logical path has been recovered from blocked condition on the remote copy conditions.	21	81	XY	F1	Service	Yes (*17)	X: CHA PCB# (*1) Y: LCP#1 (*3)
Pair volume status error	HRC started the initial copy or out of sync for this volume.	D0	0X	YY	FE	Service	Yes (*17)	X: CU# YY: LDEV#
	HRC completed the initial copy for this volume.	D0	1X	YY	FE	Service	Yes (*17)	X: CU# YY: LDEV#
	HRC for this volume was deleted. (Operation from an SVP/remote console or a host processor)	D0	2X	YY	FE	Service	Yes (*17)	X: CU# YY: LDEV#
	MCU changed volume pair status. (Operation from an SVP/remote console or a host processor)	D0	3X	YY	FE	Service	No	X: CU# YY: LDEV#
	Status of the R-VOL is changed.	D1	ZX	YY	FE	Service	Yes (*17)	X: CU# YY: LDEV# Z: (*16)
	RCU changed status of R-VOL to suspend. (Operation from an SVP/remote console or a host processor.)	D2	0X	YY	FE	Service	No	X: CU# YY: LDEV#
	Status of the R-VOL was changed from suspend to simplex. (Operation from an SVP/remote console or a host processor.)	D2	1X	YY	FE	Service	No	X: CU# YY: LDEV#
	Status of R-VOL was changed from duplex to simplex. (Operation from an SVP/remote console or a host processor.)	D2	2X	YY	FE	Service	No	X: CU# YY: LDEV#
	Status of the R-VOL was changed from pendingduplex to simplex. (Operation from an SVP/remote console or a host processor.)	D2	3X	YY	FE	Service	No	X: CU# YY: LDEV#
	HODM started the migration copy or out of sync for this volume.	D3	0X	YY	FE	Service	Yes (*17)	X: CU# YY: LDEV#
	HODM completed the migration copy for this volume.	D3	1X	YY	FE	Service	Yes (*17)	X: CU# YY: LDEV#
	HODM for this volume was deleted. (Operation from an SVP/remote console)	D3	2X	YY	FE	Service	Yes (*17)	X: CU# YY: LDEV#
	HODM started the erase operation for the R-VOL.	D3	AX	YY	FE	Service	No (*17)	X: CU# YY: LDEV#
	HODM completed the erase operation for the R-VOL.	D3	BX	YY	FE	Service	No (*17)	X: CU# YY: LDEV#
	HRC/HODM for this volume was suspended (Due to an unrecoverable failure on the remote copy connections.)	D4	0X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV#

Copyright ©2000,2001, Hitachi, Ltd.

SIM Reference Codes Detected by the Processor for HRC/HODM (2/2)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		36	37	2D	3C			
Pair volume status error	HRC/HODM for this volume was suspended (Due to an unrecoverable failure on the M-VOL or the remote copy connections)	D4	1X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV#
	HRC/HODM for this volume was suspended (Due to an unrecoverable failure on the R-VOL)	D4	2X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV#
	HRC for this volume was suspended (Caused by DFW to the R-VOL was prohibited)	D4	3X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV#
	HRC for this volume was suspended (Due to an internal error condition detected by the RCU)	D4	4X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV#
	HRC for this volume was suspended (Caused by Delete pair operation was issued to the R-VOL)	D4	5X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV#
	Erase operation for this volume was not completed. (Due to anerror conditions)	D4	8X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV#
	MCU detected a Moderate Level SIM for RCU.	D4	DX	YY	FE	Moderate	Yes (*18)	X: CU# YY: LDEV#
	MCU detected an Acute or Serious Level SIM for RCU.	D4	EX	YY	FE	Serious	Yes (*18)	X: CU# YY: LDEV#
	Status of the M-VOL was not consistent with the R-VOL.	D4	FX	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV#

Copyright ©2000, Hitachi, Ltd.

Blank Sheet

Copyright ©2000, Hitachi, Ltd.

Blank Sheet

Copyright ©2000, Hitachi, Ltd.

SIM Reference Codes Detected by the Processor for HRC (Asynchronous) (1/2)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		36	37	2D	3C			
Pair volume status error	HRC started the initial copy or out of sync for this volume.	D5	0X	YY	FE	Service	Yes (*17)	X: CU# YY: LDEV#
	HRC completed the initial copy for this volume.	D5	1X	YY	FE	Service	Yes (*17)	X: CU# YY: LDEV#
	HRC for this volume was accepted delete pair operation. (Operation from an SVP/remote console or a host processor)	D5	2X	YY	FE	Service	Yes (*17)	X: CU# YY: LDEV#
	HRC for this volume was accepted suspend pair operation. (Operation from an SVP/remote console or a host processor)	D5	3X	YY	FE	Service	Yes (*17)	X: CU# YY: LDEV#
	Delete pair operation for this HRC volume has completed.	D5	4X	YY	FE	Service	Yes (*17)	X: CU# YY: LDEV#
	Suspend pair operation for this HRC volume has completed.	D5	5X	YY	FE	Service	Yes (*17)	X: CU# YY: LDEV#
	The R-VOL status has changed as requested by MCU.	D6	ZX	YY	FE	Service	Yes (*17)	X: CU# YY: LDEV# Z: (*16)
	The R-VOL has accepted/completed state change as requested by operation. (Operation from an SVP/remote console or a host processor.)	D7	ZX	YY	FE	Service	No	X: CU# YY: LDEV# Z: (*26)
	The M-VOL has suspended. (Due to an unrecoverable failure on the remote copy connections.)	DB	0X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV#
	The M-VOL has suspended. (Due to an unrecoverable failure on the M-VOL or the remote copy connections)	DB	1X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV#
	The M-VOL has suspended. (Due to an unrecoverable failure on the R-VOL)	DB	2X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV#
	The M-VOL has suspended. (Caused by DFW to the R-VOL was prohibited)	DB	3X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV#
	The M-VOL has suspended. (Caused by Suspend pair operation was issued to the R-VOL)	DB	4X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV#

Copyright ©2000, Hitachi, Ltd.

SIM Reference Codes Detected by the Processor for HRC (Asynchronous) (2/2)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		36	37	2D	3C			
Pair volume status error	The M-VOL has suspended. (Caused by Delete pair operation was issued to the R-VOL)	DB	5X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV#
	The R-VOL has suspended. (Due to an unrecoverable failure on the remote copy connections)	DB	6X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV#
	The R-VOL has suspended. (Due to an unrecoverable failure on the R-VOL)	DB	7X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV#
	The R-VOL has suspended. (Due to an MCU power-off event)	DB	8X	YY	FE	Service	No	X: CU# YY: LDEV#
	MCU detected a Service Level SIM for RCU.	DB	CX	YY	FE	Service	Yes	X: CU# YY: LDEV#
	MCU detected a Moderate Level SIM for RCU.	DB	DX	YY	FE	Moderate	Yes	X: CU# YY: LDEV#
	MCU detected an Acute or Serious Level SIM for RCU.	DB	EX	YY	FE	Serious	Yes	X: CU# YY: LDEV#
	Status of the M-VOL was not consistent with the R-VOL.	DB	FX	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV#

Notice : SIM which REF.CODE is DB7XXX may be reported in the following case.

- When the Suspend Pair operation with the Drain option is accepted by the MCU/RCU under the host I/O.
- When the Delete Pair operation with the Group option is accepted by the RCU under the host I/O.

Copyright ©2000, Hitachi, Ltd.

SIM Reference Codes Detected by the Processor for HMRCF/HOMRCF/HIHSM/HXRC (1/1)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		36	37	2D	3C			
HMRCF error or HOMRCF error	Copy warning end	47	AY	XX	FE	Moderate	No	XX:T-Vol# Y: CU#
	Copy abnormal end (S-Vol blocked)	47	BY	XX	FE	Moderate	No	XX:T-Vol# Y: CU#
	Copy abnormal end (T-Vol blocked)	47	CY	XX	FE	Moderate	No	XX:T-Vol# Y: CU#
	Copy abnormal end (others)	47	DY	XX	FE	Moderate	Yes	XX:T-Vol# Y: CU#
HIHSM error	HIHSM Volume Migration Abnormal End	47	FY	XX	FE	Moderate	No	XX:T-Vol# Y: CU#
HXRC error	Sidefile 40% over	49	0X	YY	FE	Service	Yes ***	X: CU# YY: LDEV#

Copyright ©2000,2003, Hitachi, Ltd.

(*1)

Separate Model

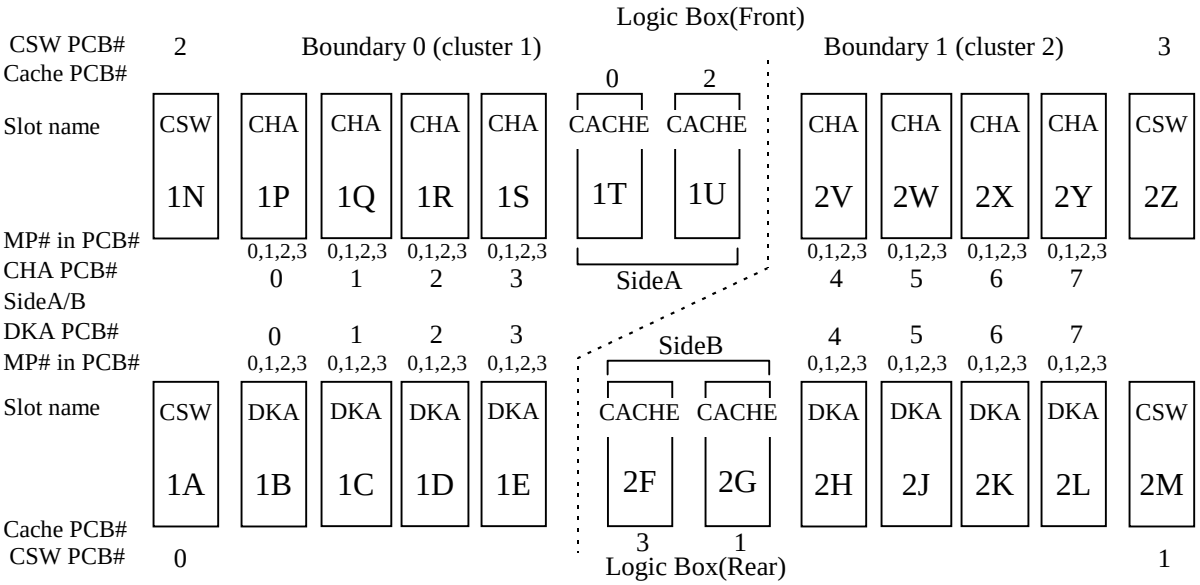
CHA PCB#: x‘0’ to x‘7’ indicates the CHA PCB number. See the figure below.
DKA PCB#: x‘0’ to x‘7’ indicates the DKA PCB number. See the figure below.
CSW PCB#: x‘0’ to x‘3’ indicates the CSW PCB number. See the figure below.
Cache PCB#: x‘0’ to x‘3’ indicates the Cache PCB number. See the figure below.

Single Cabinet Model

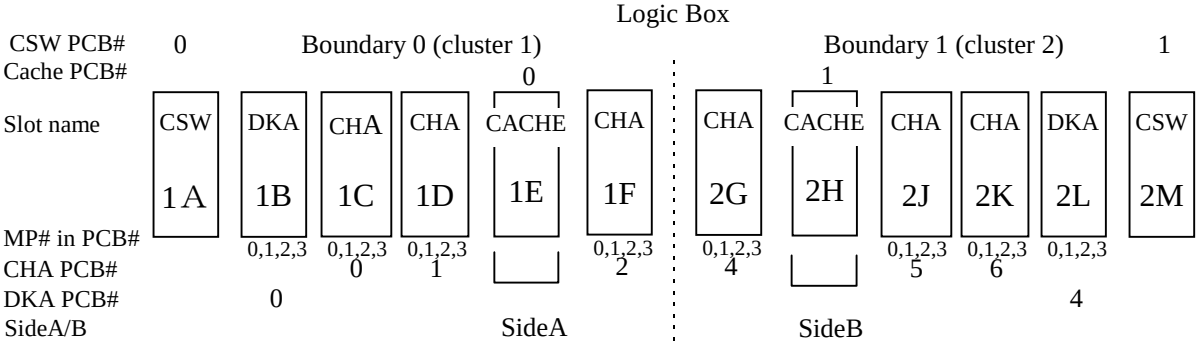
CHA PCB#: x‘0’ to x‘6’ indicates the CHA PCB number. See the figure below.
DKA PCB#: x‘0’ to x‘4’ indicates the DKA PCB number. See the figure below.
CSW PCB#: x‘0’ to x‘1’ indicates the CSW PCB number. See the figure below.
Cache PCB#: x‘0’ to x‘1’ indicates the Cache PCB number. See the figure below.

(*2) Side A/B: Indicates the side of cache/shared memory. See the figure below.

Separate Model



Single Cabinet Model



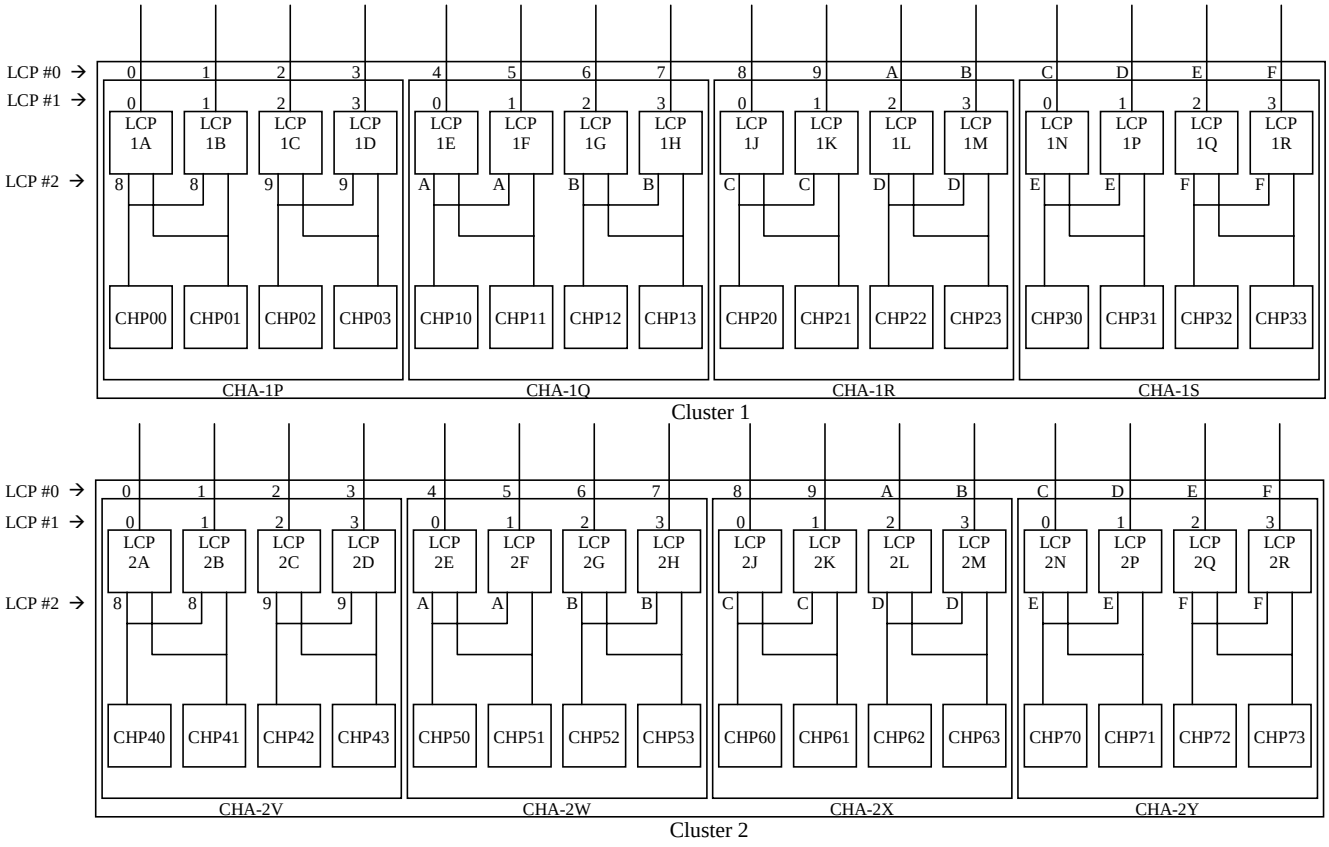
Copyright ©2000, Hitachi, Ltd.

(*3)

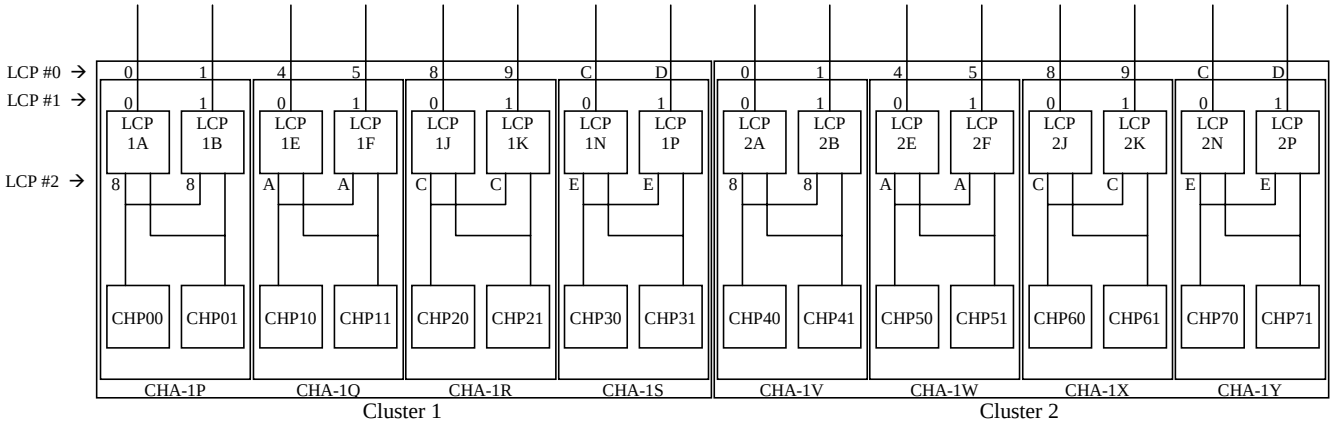
Separate Model

LCP #0: x‘0’ to x‘F’ indicates the LCP number.
LCP #1: x‘0’ to x‘3’ indicates the LCP number.
LCP #2: x‘8’ to x‘F’ indicates the LCP number.

-DKC-F410I-8S-



-DKC-F410I-4S-

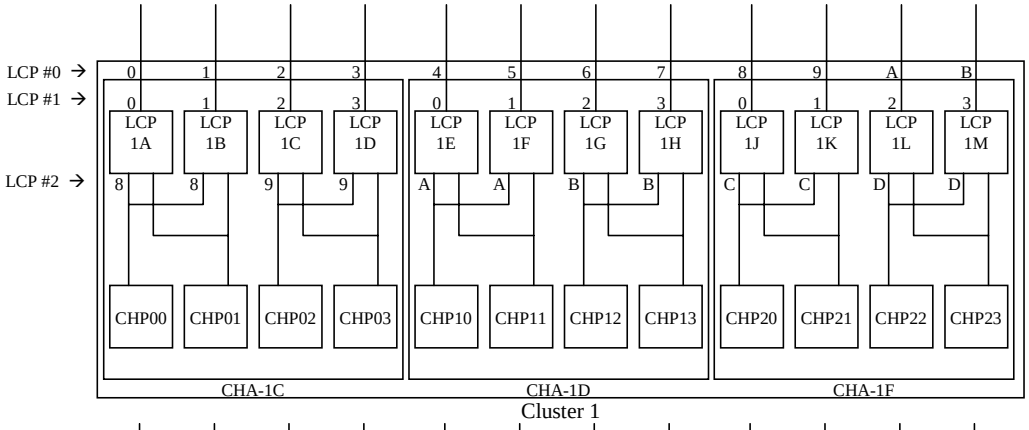


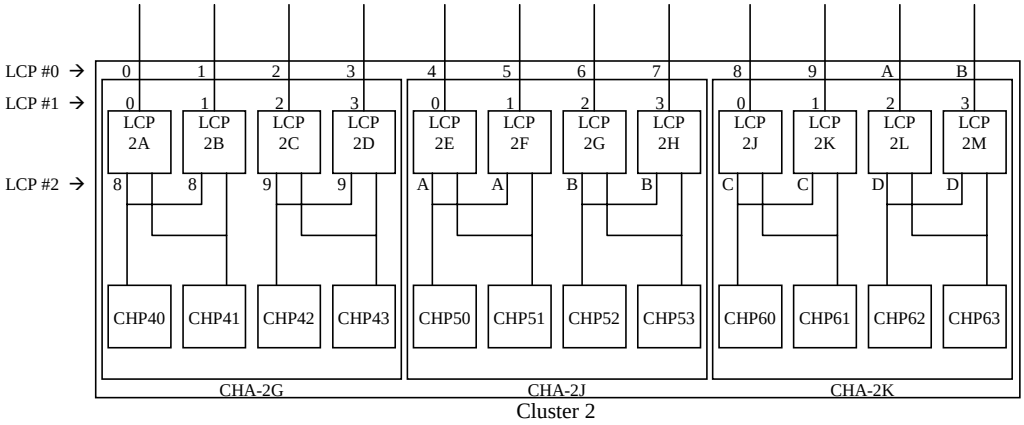
Copyright ©2000, Hitachi, Ltd.

Single Cabinet Model

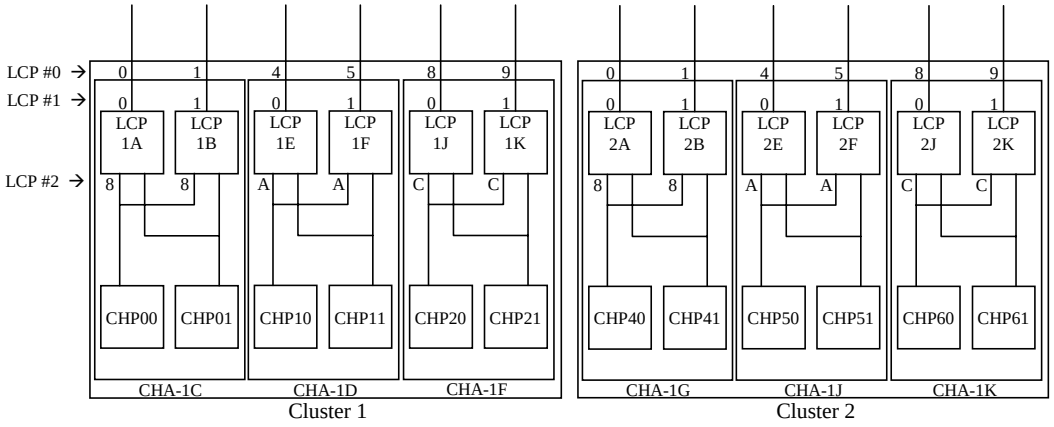
LCP #0: x‘0’ to x‘D’ indicates the LCP number.
LCP #1: x‘0’ to x‘3’ indicates the LCP number.
LCP #2: x‘8’ to x‘D’ indicates the LCP number.

-DKC-F410I-8S-



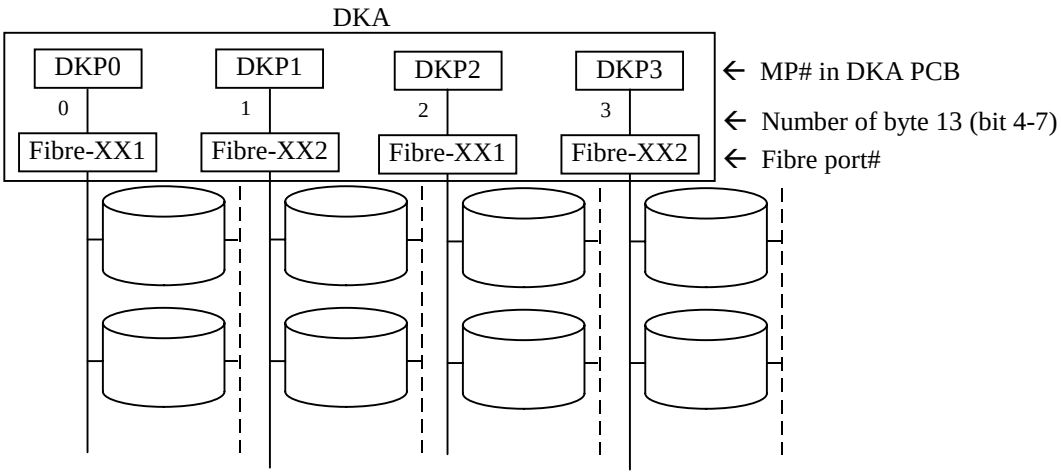


-DKC-F410I-4S-



Copyright ©2000, Hitachi, Ltd.

(*4) Port #: x‘0’ to x‘3’ indicates the FIBRE port number. See the figure below.



(*5) The package that is not defined in the configuration information exists.
If it is prepared for new installation, it is necessary to do the new installation procedure.
Otherwise it should be pulled out by executing P/S off.

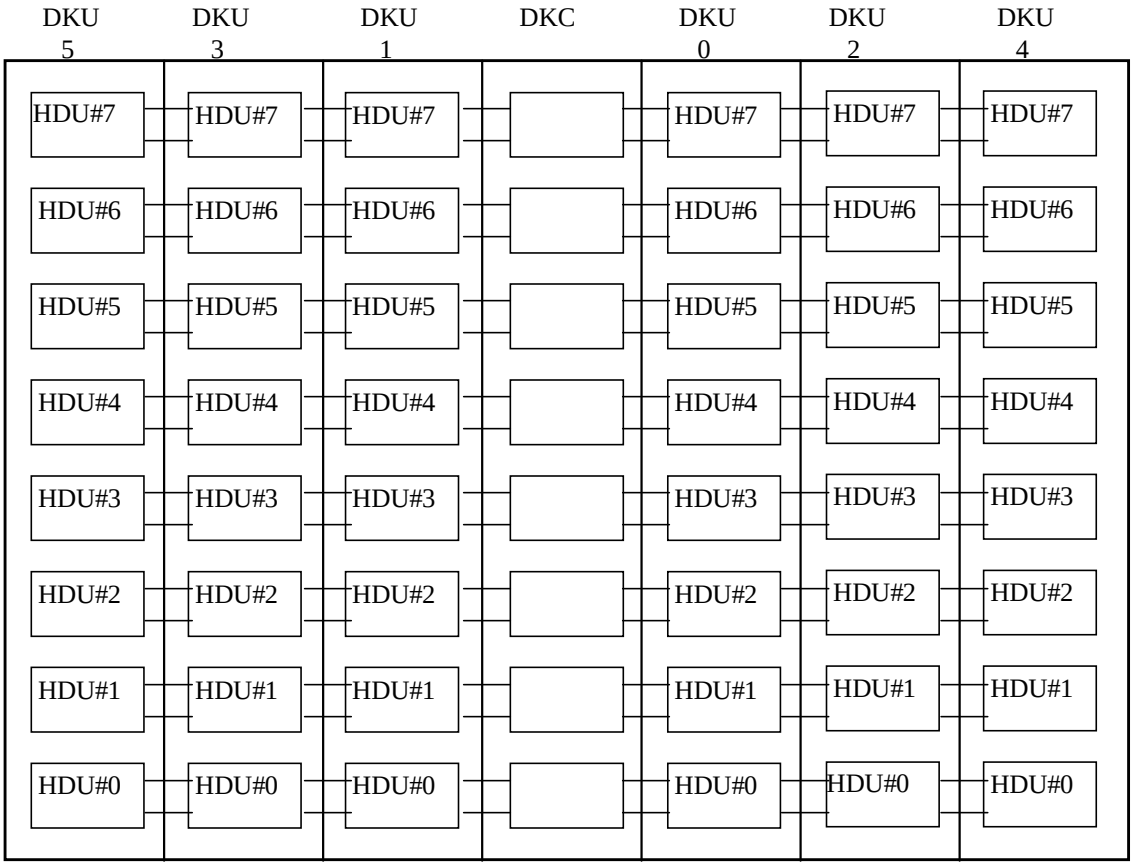
(*7) Isolate the error according to the procedure shown in TRBL05-170.

(*8) Recover the error according to the procedure shown in TRBL05-270.

(*10) Perform error isolation according to the procedure given in the two separate pages attached to TRBL05-300.

Copyright ©2000, Hitachi, Ltd.

(*12) DKU#: x‘0’ to x‘3’ indicates DKU number. See the figure below.
HDU#: x‘0’ to x‘7’ indicates HDU number. See the figure below.



(*13) reason code
x‘0’ : Pinned data exist
x‘1’ : The shutdown of the power supply was occurred
x‘2’ : Invalid Version/Revision exists

(*15) Recover LDEVs according to the procedure shown in TRBL05-330.

(*16) Change pair status number
x‘0’: From simplex to duplex pending
x‘1’: From simplex to duplex
x‘2’: From pending duplex to duplex
x‘3’: From pending duplex to suspend
x‘4’: From duplex to suspend
x‘5’: From duplex to simplex
x‘6’: From pending duplex to simplex
x‘7’: From suspend to simplex
x‘8’: From suspend to duplex pending

Copyright ©2000, Hitachi, Ltd.

(*17) You can suppress reporting the HRC/HODM Service SIM to the HOST by RCU Option operation (PPRC support by HOST and Service SIM of HRC/HODM).

- Service level SIM -

PPRC support by HOST	Service SIM or HRC/HODM	level of error	HRC	HODM
Yes	Report	DKC_SIM	Host Report	Host Report
		DEV_SIM	Not Host Report	Host Report
	Not Report	DKC_SIM	Not Host Report	Not Host Report
		DEV_SIM	Not Host Report	Not Host Report
No	Report	DKC_SIM	Host Report	Host Report
		DEV_SIM	Host Report	Host Report
	Not Report	DKC_SIM	Not Host Report	Not Host Report
		DEV_SIM	Not Host Report	Not Host Report

- Moderate or Serious level SIM -

PPRC support by HOST	level of error	HRC	HODM
Yes	DKC_SIM	Host Report	Host Report
	DEV_SIM	Not Host Report	Host Report
No	DKC_SIM	Host Report	Host Report
	DEV_SIM	Host Report	Host Report

(*18) SIMs which REF.CODE are D4DX, D4EX are reported in case of HODM.
In case of HRC, SIMs reported from RCU are reported to the host by MCU.

Severity Level	RC of reported SIM for HRC	RC of reported SIM for HODM
Acute or Serious	No modification	D4EX
Moderate	No modification	D4DX
Service (Not HRC SIM)	No modification	Not reported
Service (HRC SIM)	Not reported	Not reported

(*19) This temporary blocking is to recover the logical table on SM and be automatically recovered.

(*20) In case of the replacement of the cache memory PCB on the side having blocked SM (see REP01-160 work ID = RCA1), insert the removed cache memory PCB again.

(*21) Isolate the error according to the procedure shown in TRBL05-200.

(*22) The LDEV is blocked because of an error (inconsistency between data on the A and B sides) of configuration information stored in the SM. Recover the error following the instruction of the Technical Support Center.

(*23) X represents the X in a program version “? X-? ? -? ? /? ? ”.

(*24) Cache SIMM sizes of sides A and B are different because the replacement of the cache memory has been performed on one side only. Perform the replacement left referring to the description in the remark column.

(*25) Type of the lost information is reported according to the bit position. (There may be the case that two or more bits are set.)

Copyright ©2000, Hitachi, Ltd.

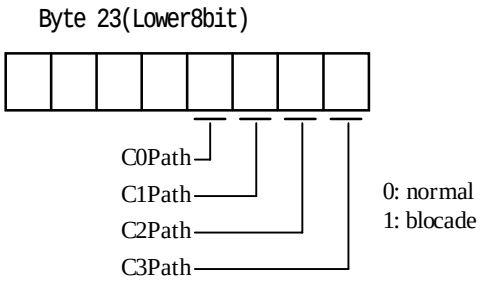
(*26) Change pair status number
- x‘0’: Accepted Suspend Pair operation
- x‘1’: Accepted Delete Pair operation (The R-VOL is in suspended status)
- x‘2’: Accepted Delete Pair operation (The R-VOL is in duplex status)
- x‘3’: Accepted Delete Pair operation (The R-VOL is in pending duplex status)
- x‘4’: Completed Suspend Pair operation
- x‘5’: Completed Delete Pair operation

(*27) In the case that the error is detected in the area of ROM, the level of error is “Moderate” in other case “Service”.

(*28) Recover the error according to the procedure shown in TRBL11-10.

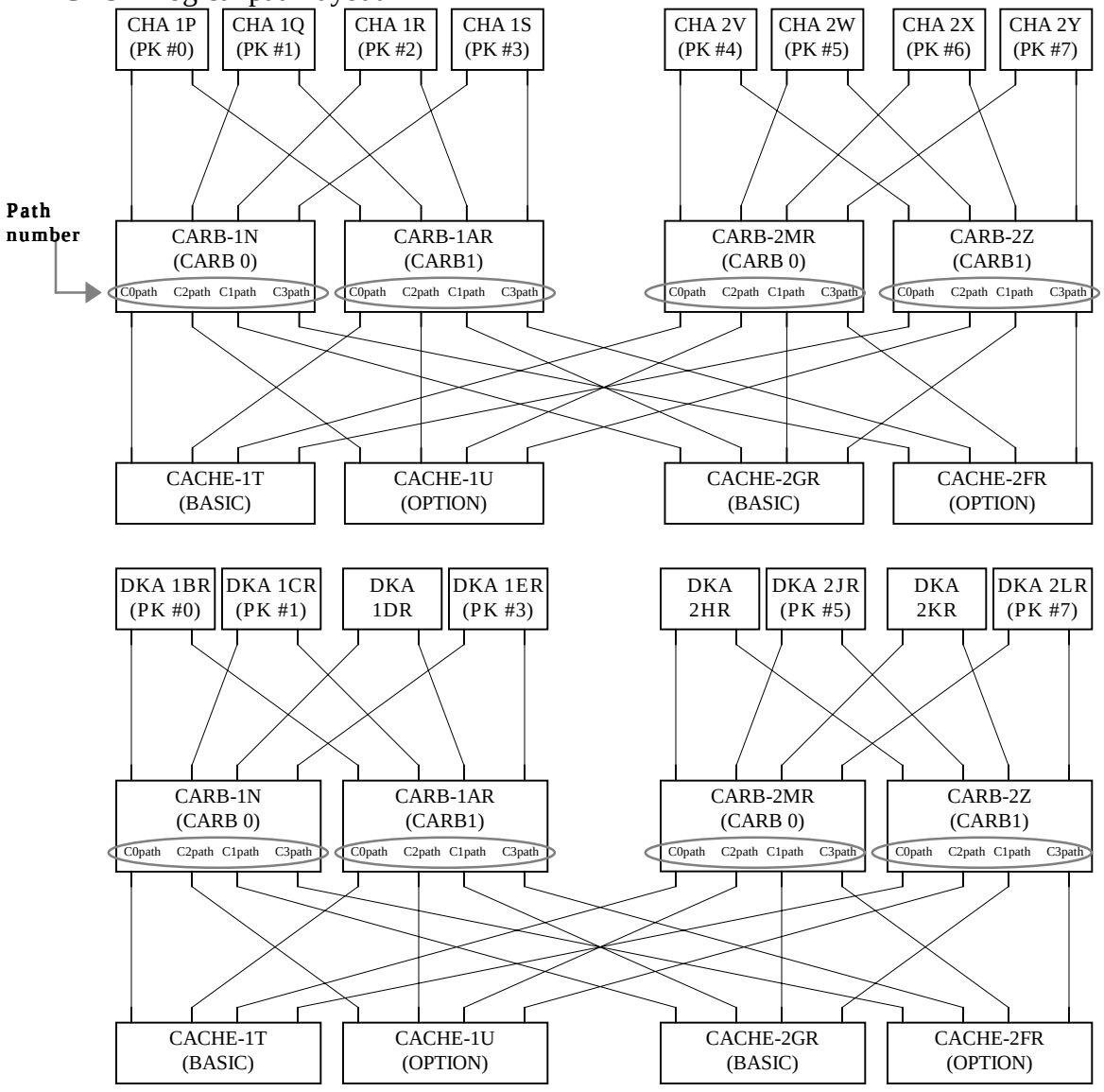
Copyright ©2000, Hitachi, Ltd.

(*29) C path bitmap indicates status of C path. See the figure below.



Separate Model

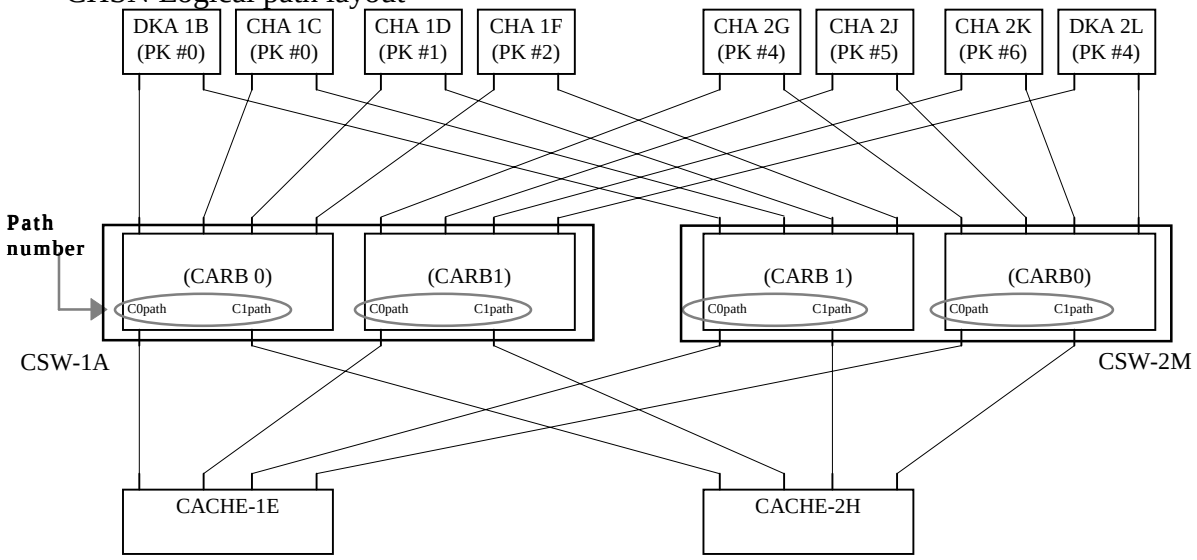
CHSN Logical path layout



Copyright ©2000, Hitachi, Ltd.

Single Cabinet Model

CHSN Logical path layout

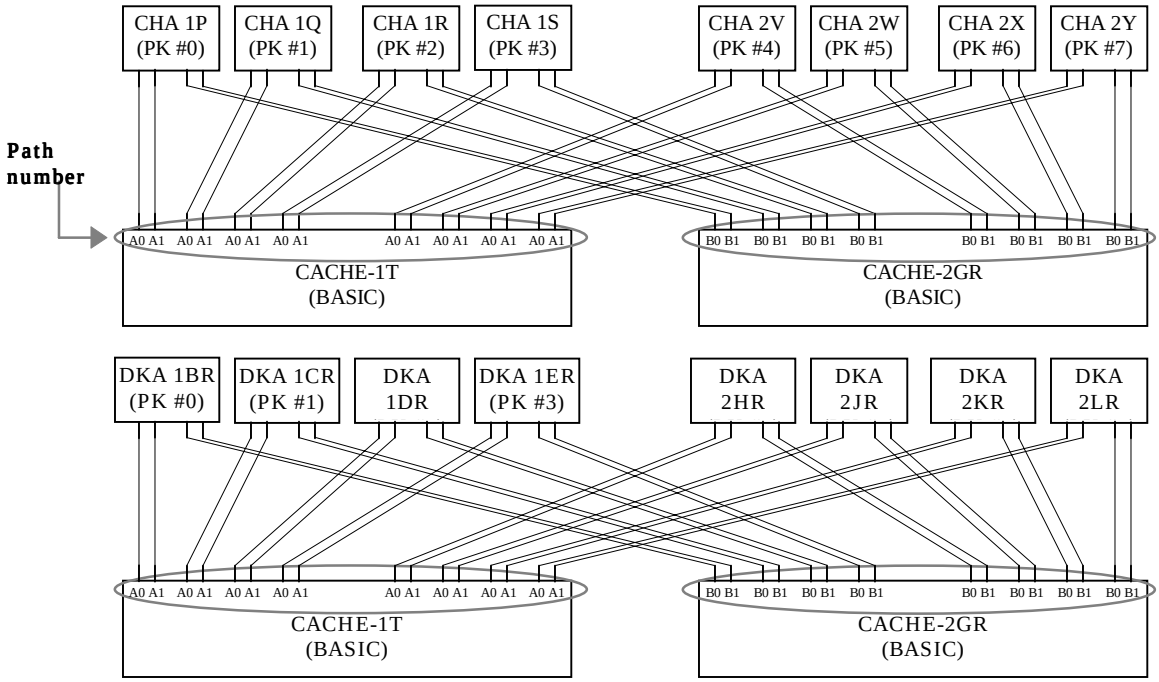


(*30) If this reference code is reported, execute the micro-program exchange procedure (On-line) of the micro type “DKCMAIN”. (MICRO-FC04-10 to 04-120)

(*31) PATH# A0, A1, B0, B1 indicates the SHSN Logical path number. See the figure below.

Separate Model

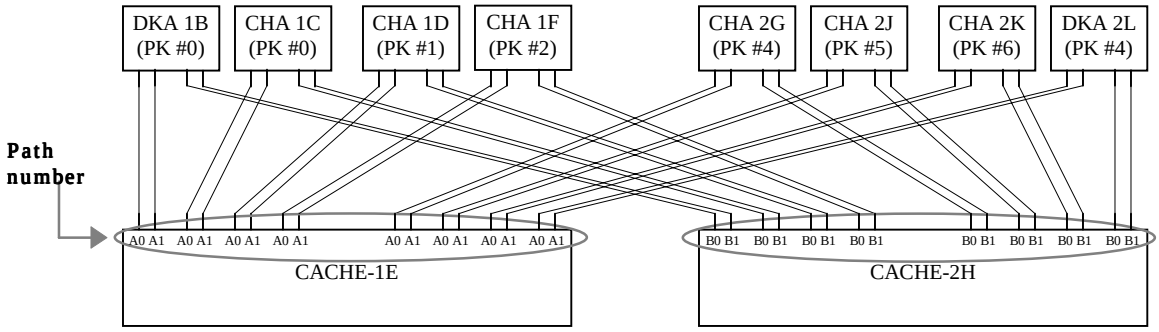
SHSN Logical path layout



Copyright ©2000, Hitachi, Ltd.

Single Cabinet Model

SHSN Logical path layout



(*32) In the case that there are no redundance of drive the level of error is “Serious”.

Copyright ©2000, Hitachi, Ltd.

SIM Reference Codes Detected by the SVP

Error		REF code			SIM	Level of	Host	Remarks
		22	23	13	28	error	report	
Environmental error	Temperature abnormal	BF	1X *1	XX *13	F1	Moderate	Yes	
	Voltage alarm	BF	2X *2	XX *13	F1	Moderate	Yes	
	Voltage warning	BF	3X *3	XX *13	F1	Moderate	Yes	
	P/S warning	BF	4X *4	XX *13	F1	Moderate	Yes	
	Battery warning	BF	5X *5	XX *13	F1	Moderate	Yes	
	AC warning	BF	6X *6	XX *13	F1	Moderate	Yes	
	Fan abnormality : CL1 logic	BF	7X *7	10	F1	Moderate	Yes	
	Fan abnormality : CL2 logic	BF	7X *8	20	F1	Moderate	Yes	
	Fan abnormality : HDU-R1X	BF	7X *9	3X *13	F1	Moderate	Yes	
	Fan abnormality : HDU-L1X	BF	7X *9	4X *13	F1	Moderate	Yes	
	Fan abnormality : HDU-R2X	BF	7X *9	5X *13	F1	Moderate	Yes	
	Fan abnormality : HDU-L2X	BF	7X *9	6X *13	F1	Moderate	Yes	
	JP remains	BF	8X *10	XX *13	F1	Moderate	Yes	
	Environment monitor error	BF	9X *11	XX *13	F1	Service	No	
	Environment monitor disagreement	BF	AX *12	XX *13	F1	Moderate	No	
	SVP P/S abnormal	BF	C0	XX *13	F1	Moderate	Yes	
SVP error	Logical inconsistency	70	XX *14	00	F1	Moderate	No	
	HEEP error	71	XX *14	00	F1	Moderate	No	
	File error	72	XX *14	00	F1	Moderate	No	
	LAN error	73	XX *14	00	F1	Moderate	No	
	S-SVP error	74	XX *14	XX *15	F1	Moderate	No	
	Windows error	75	XX *14	00	F1	Moderate	No	
	CUDG3 detected error	76	01	XX *16	F1	Moderate	No	
	LCDG3 detected error	76	10	XX *16	F1	Moderate	No	
	BOOT detected error (CHA)	79	00	XY *18	F1	Moderate	No	
	BOOT detected error (DKA)	79	01	XY *19	F1	Moderate	No	
End status of remote microprogram exchange	Normal end	7A	00	00	F1	Service	No	
	Abnormal end (SVP)	7A	01	00	F1	Service	No	
	Abnormal end (MP)	7A	02	XX *21	F1	Service	No	
	Version check error	7A	03	XX *17	F1	Service	No	
	Sum check error	7A	04	XX *17	F1	Service	No	
	LCP patch error	7A	05	XX *20	F1	Service	No	
	Warning (Configuration nconsistency)	7A	10	00	F1	Service	No	
	Warning (S-SVP busy)	7A	11	00	F1	Service	No	
	Warning (LCP busy)	7A	12	XX *20	F1	Service	No	
Dump received	WCHK1 dump(CHA)	30	80	XY *18	F1	Moderate	No	
	WCHK1 dump(DKA)	31	80	XY *19	F1	Moderate	No	
	ABEND dump(CHA)	30	81	XY *18	F1	Moderate	No	
	ABEND dump(DKA)	31	81	XY *19	F1	Moderate	No	
Backup Server	Backup Server Failure detected by SVP	BE	00	00	F1	Moderate	No	
	ATL Failure	BE	01	00	F1	Moderate	No	
	MT Failure	BE	02	00	F1	Moderate	No	
	OS Failure	BE	03	00	F1	Moderate	No	
	NetWorker Error	BE	04	00	F1	Moderate	No	
	Application Error	BE	05	00	F1	Moderate	No	

Copyright ©2000, Hitachi, Ltd.

*1 Contents of byte 23 when a temperature abnormality occurred

Byte 23	Error
10	Abnormal temperature (over 60 ºC) is detected in the front side .
11	Abnormal temperature (over 60 ºC) is detected in the back side.
12	Abnormal temperature (over 45 ºC) is detected in the front side .
13	Abnormal temperature (over 45 ºC) is detected in the back side.

*2 Contents of byte 23 when a voltage alarm was given

Byte 23	Error
20	5V voltage has dropped below 80%.
21	3V voltage has dropped below 80%.
22	12V voltage has dropped below 80%.

*3 Contents of byte 23 when a voltage warning was given

Byte 23	Error
30	Voltage for shared memory has dropped below 80 %.
31	Voltage for cache memory periphery has dropped below 80 %.
33	12V voltage has dropped below 80 %.

*4 Contents of byte 23 when a P/S warning was given

Byte 23	Error
40	5V PS 0 box abnormality has been detected.
41	5V PS 1 box abnormality has been detected.
42	5V PS 2 box abnormality has been detected.
43	5V PS 3 box abnormality has been detected.
44	3V PS 0 box abnormality has been detected.
45	3V PS 1 box abnormality has been detected.
46	3V PS 2 box abnormality has been detected.
47	3V PS 3 box abnormality has been detected.
48	Multi PS 0 box abnormality has been detected.
49	Multi PS 1 box abnormality has been detected.
4A	HDD P/L Multi PS 1 box abnormality has been detected.
4B	HDD P/L Multi PS 0 box abnormality has been detected.

*5 Contents of byte 23 when a battery warning was given

Byte 23	Error
50	Battery0 or BATT-CTR0 abnormality has been detected..
52	Battery1 or BATT-CTR1 abnormality has been detected.
53	Battery2 or BATT-CTR2 abnormality has been detected.
5A	Battery0 abnormality has been detected.(DIAG)
5B	Battery1 abnormality has been detected.(DIAG)
5C	Battery2 abnormality has been detected.(DIAG)

Copyright ©2000, Hitachi, Ltd.

*6 Contents of byte 23 when an AC warning was given

Byte 23	Error
60	AC power off/interruption of the breaker box occurred.

*7 Contents of byte 23 when a fan lock in a CL1 Logic Box occurred.

Byte 23	Error
70	Low rotation speed of FPSFAN12A has been detected.
71	Low rotation speed of FPSFAN12B has been detected.
72	Low rotation speed of FPSFAN11A has been detected.
73	Low rotation speed of FPSFAN11B has been detected.
74	Low rotation speed of RPSFAN11A has been detected.
75	Low rotation speed of RPSFAN11B has been detected.
76	Low rotation speed of RPSFAN12A has been detected.
77	Low rotation speed of RPSFAN12B has been detected.
78	Low rotation speed of FLGFAN12A has been detected.
79	Low rotation speed of FLGFAN12B has been detected.
7A	Low rotation speed of FLGFAN11A has been detected.
7B	Low rotation speed of FLGFAN11B has been detected.
7C	Low rotation speed of RLGFAN11A has been detected.
7D	Low rotation speed of RLGFAN11B has been detected.
7E	Low rotation speed of RLGFAN12A has been detected.
7F	Low rotation speed of RLGFAN12B has been detected.

*8 Contents of byte 23 when a fan lock in a CL2 Logic Box occurred.

Byte 23	Error
70	Low rotation speed of FPSFAN21A has been detected.
71	Low rotation speed of FPSFAN21B has been detected.
72	Low rotation speed of FPSFAN22A has been detected.
73	Low rotation speed of FPSFAN22B has been detected.
74	Low rotation speed of RPSFAN21A has been detected.
75	Low rotation speed of RPSFAN21B has been detected.
76	Low rotation speed of RPSFAN22A has been detected.
77	Low rotation speed of RPSFAN22B has been detected.
78	Low rotation speed of FLGFAN22A has been detected.
79	Low rotation speed of FLGFAN22B has been detected.
7A	Low rotation speed of FLGFAN21A has been detected.
7B	Low rotation speed of FLGFAN21B has been detected.
7C	Low rotation speed of RLGFAN21A has been detected.
7D	Low rotation speed of RLGFAN21B has been detected.
7E	Low rotation speed of RLGFAN22A has been detected.
7F	Low rotation speed of RLGFAN22B has been detected.

Copyright ©2000, Hitachi, Ltd.

*9 Contens of byte 23 when a fan lock in a HDU occurred.

Byte 23	Error
70	Low rotation speen of FAN-XXX2A-ASSY has been detected. (FAN-XXX:the part shown in byte 13)
71	Low rotation speen of FAN-XXX1A-ASSY has been detected. (FAN-XXX:the part shown in byte 13)
72	Low rotation speen of FAN-XXX0A-ASSY has been detected. (FAN-XXX:the part shown in byte 13)
73	Low rotation speen of FAN-XXX2B-ASSY has been detected. (FAN-XXX:the part shown in byte 13)
74	Low rotation speen of FAN-XXX1B-ASSY has been detected. (FAN-XXX:the part shown in byte 13)
75	Low rotation speen of FAN-XXX0B-ASSY has been detected. (FAN-XXX:the part shown in byte 13)

*10 Contents of byte 23 when warning of JP (Jumper plug) remains was given

Byte 23	Error
81	JP for LOGIC 1 remains.
82	JP for LOGIC 2 remains.
85	JP for HDU-XX0~HDU-XX3 remains.
86	JP for HDU-XX4~HDU-XX7 remains.

*11 Contents of byte 23 when an environment monitor error occurred

Byte 23	Error
90	Environment monitor register access error
91	Basic clock error of the environment monitor PCB occurred.
92	Parity error of the environment monitor PCB occurred.
93	Battery diagnostic mode setting failure.

*12 Contents of byte 23 when an environment monitors disagreement error occurred

Byte 23	Error
A0	An environment monitors disagreement error occurred.
A1	An environment monitors disagreement error of P/S occurred

Copyright ©2000, Hitachi, Ltd.

*13 Contents of byte 13 when an environmental abnormality error occurred

Byte 13	Error section	Byte 13	Error section
10	Logic 1	55	HDU-R25
20	Logic 2	56	HDU-R26
30	HDU-R10	57	HDU-R27
31	HDU-R11	60	HDU-L20
32	HDU-R12	61	HDU-L21
33	HDU-R13	62	HDU-L22
34	HDU-R14	63	HDU-L23
35	HDU-R15	64	HDU-L24
36	HDU-R16	65	HDU-L25
37	HDU-R17	66	HDU-L26
40	HDU-L10	67	HDU-L27
41	HDU-L11	70	DKUMN-R1F
42	HDU-L12	71	DKUMN-R1R
43	HDU-L13	72	DKUMN-L1F
44	HDU-L14	73	DKUMN-L1R
45	HDU-L15	74	DKUMN-R2F
46	HDU-L16	75	DKUMN-R2R
47	HDU-L17	76	DKUMN-L2F
50	HDU-R20	77	DKUMN-L2R
51	HDU-R21	80	PWRCTL-1
52	HDU-R22	81	PWRCTL-2
53	HDU-R23	90	AC BOX-R10
54	HDU-R24	91	AC BOX-R11

*14 Contents of byte 23 when a logical error, a HEEP error, a file error, a LAN ereor or Windows error occurred

Byte 23

Byte 23	Error
0x00	Dump task
0x01	DKU inline
0x02	Microprogram change (online)
0x03	Information
0x04	LOGOUT
0x05	PATH inline
0x06	Back Ground
0x07	DIAG
0x08	Install
0x09	Online
0x0A	Microprogram change (offline)
0x0B	Special PCB maintenance
0x0C	Common communication function
0xEF	Other AP

Copyright ©2000, Hitachi, Ltd.

*15 Contents of byte 23 and byte 13 when a S-SVP logical error occurred

Byte 23
S-SVP error code (High byte)
Byte 13
S-SVP error code (Low byte)

*16 Contents of byte 13 when a CUDG detection error occurred

Byte13(bit0-bit5)

Byte 13 (bit 0 - bit 5)	MPID	Byte 13 (bit 0 - bit 5)	MPID
000000	CHP00-1P	011000	CHP24-2X
000001	CHP01-1P	011001	CHP25-2X
000010	CHP10-1P	011010	CHP34-2X
000011	CHP11-1P	011011	CHP35-2X
000100	CHP02-1Q	011100	CHP26-2Y
000101	CHP03-1Q	011101	CHP27-2Y
000110	CHP12-1Q	011110	CHP36-2Y
000111	CHP13-1Q	011111	CHP37-2Y
001000	CHP04-1R	100000	DKP08-1B
001001	CHP05-1R	100001	DKP18-1B
001010	CHP14-1R	100010	DKP09-1C
001011	CHP15-1R	100011	DKP19-1C
001100	CHP06-1S	100100	DKP0A-1D
001101	CHP07-1S	100101	DKP1A-1D
001110	CHP16-1S	100110	DKP0B-1E
001111	CHP17-1S	100111	DKP1B-1E
010000	CHP20-2V	101000	DKP28-2H
010001	CHP21-2V	101001	DKP38-2H
010010	CHP30-2V	101010	DKP29-2J
010011	CHP31-2V	101011	DKP39-2J
010100	CHP22-2W	101100	DKP2A-2K
010101	CHP23-2W	101101	DKP3A-2K
010110	CHP32-2W	101110	DKP2B-2L
010111	CHP33-2W	101111	DKP3B-2L

Byte13(bit6-bit7)

Byte 13 (bit 6 - bit 7)	Section
00	CHA/DKA
01	CACHE+Shared Memory
10	CACHE PORT+Shared Memory
11	CACHE

Copyright ©2000, Hitachi, Ltd.

*17 Contents of byte 13 when a version check error or sum check error occurred

Byte 13	Micro-program type
00	RAM BOOT
01	DKC MANI
02	LCP
03	MCP
04	LCDG
05	DKU
06	SVP
07	S-SVP

*18 Contents of byte 13 when a CHP error occurred.

Contents of high byte of Byte13(X).

High byte of Byte 13	Contents
0	1st. CHA of cluster 1
1	2nd. CHA of cluster 1
2	3rd. CHA of cluster 1
3	4th. CHA of cluster 1
4	1st. CHA of cluster 2
5	2nd. CHA of cluster 2
6	3rd. CHA of cluster 2
7	4th. CHA of cluster 2

Contents of low byte of Byte13(Y).

High byte of Byte 13	Contents
0	1st. CHP of the CHA
1	2nd. CHP of the CHA
2	3rd. CHP of the CHA
3	4th. CHP of the CHA

In WCHK1 dump and ABEND dump received SIM = 3080XX, 3081XX, the system error code is indicated on the SIM log detail screen in the format [YYYY] as in Reference Code 3080X0[YYYY].

*19 Contents of byte 13 when a DKP error occurred.

Contents of high byte of Byte13(X).

High byte of Byte 13	Contents
0	1st. DKA of cluster 1
1	2nd. DKA of cluster 1
2	3rd. DKA of cluster 1
3	4th. DKA of cluster 1
4	1st. DKA of cluster 2
5	2nd. DKA of cluster 2
6	3rd. DKA of cluster 2
7	4th. DKA of cluster 2

Copyright ©2000, Hitachi, Ltd.

Contents of low byte of Byte13(Y).

High byte of Byte 13	Contents
0	1st. DKP of the DKA
1	2nd. DKP of the DKA

In WCHK1 dump and ABEND dump received SIM = 3180XX, 3181XX, the system error code is indicated on the SIM log detail screen in the format [YYYY] as in Reference Code 3180X0[YYYY].

*20 Contents of byte 13

Contents of high byte of Byte13(X).

High byte of Byte 13	Contents
0	1st. CHA of cluster 1
1	2nd. CHA of cluster 1
2	3rd. CHA of cluster 1
3	4th. CHA of cluster 1
4	1st. CHA of cluster 2
5	2nd. CHA of cluster 2
6	3rd. CHA of cluster 2
7	4th. CHA of cluster 2

Contents of low byte of Byte13(Y).

High byte of Byte 13	Contents
0	1st. LCP of the CHA
1	2nd. LCP of the CHA
2	3rd. LCP of the CHA
3	4th. LCP of the CHA

Copyright ©2000, Hitachi, Ltd.